Silicon Deformable Mirrors and CMOS-based Wavefront Sensors

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ABSTRACT

Inexpensive wavefront sensors and deformable mirrors are essential for addressing potential commercial applications for adaptive optics like laser beam control and ophthalmology. Silicon micromachined deformable mirrors offer the potential for low cost and high actuator density, but there are some problems with the architectures currently available like low mirror quality and high actuator crosstalk. Shack-Hartmann wavefront sensors are still based on traditional charge coupled device (CCD) arrays making them very expensive at high frame rates. To address the need for low cost deformable mirrors, we have implemented a new architecture of silicon deformable mirror designed to be low cost, have low actuator crosstalk, and still maintain good mirror quality. Furthermore, we built and tested a CMOS Shack-Hartmann wavefront sensor to address the needs of the adaptive optics community for high speed wavefront sensing.

INTRODUCTION

Adaptive optics has been applied with great success to atmospheric aberration compensation for astronomy and satellite imaging[1] and to biological aberration compensation for retinal imaging.[2] Adaptive optics techniques are already being considered for aberration compensation in projection lithography systems, high-power lasers systems, and free-space telecommunication systems. Although many of the important applications of adaptive optics have yet to be identified, improving existing adaptive optics technology by reducing cost and improving system performance will only further foster and broaden its application.

With this in mind, many researchers have looked to silicon to solve the problems of adaptive optics systems because of the large industrial investment in developing silicon technology. Silicon technology is used today to produce the charge-coupled devices (CCDs) that are the basis of the modern Shack-Hartmann wavefront sensor. Silicon integrated circuits are used for the processing of signals from the wavefront sensors and the drive electronics for the deformable mirrors. Over the last decade there has been a considerable effort in applying silicon micromachining technology to develop a higher quality lower cost deformable mirror.

We present here the application of bulk micromachining to the development of silicon deformable mirrors and the application of CMOS imagers to the fabrication of Shack-Hartmann wavefront sensors. We demonstrate both of these technologies and further discuss their advantages over the competing technologies.

STANFORD'S SILICON DEFORMABLE MIRROR

Over the last several years, we have applied bulk silicon micromachining to the development of an inexpensive deformable mirror. The motivation behind our work is laser beam quality control, specifically for the Laser Interferometer Gravitational-wave Observatory (LIGO). LIGO is a large Michelson interferometer with Fabry-Perot cavities in each of its 4km long orthogonal arms. Because the resonance cavities of the LIGO interferometer will be tuned to the TEM_{00} spatial mode, most of the laser power must be in this mode. As the future generations of LIGO scale to higher laser power, aberrations in the laser and those induced in slightly absorbing transparent optics will couple more light from the TEM_{00} Hermite-Gaussian mode, resulting in less light in the interferometer. We are examining adaptive optics as an avenue for laser wavefront control to maintain the laser beam quality.

Ideal Deformable Mirror Characteristics

Ideal characteristics for deformable mirrors were established in the literature during the development of adaptive optics systems for astronomy in the 1970s.[3] Some of the characteristics stemmed from a basic understanding of optics. The mirror surface should have high reflectivity and low optical loss, thus necessitating a polished and coated mirror surface. Aberrations that developed during fabrication of the mirror should be able to be compensated with the mirror actuators.

More detailed mirror characteristics were derived from an understanding of the atmosphere presented by Kolmogorov.[4] Based on Kolmogorov's model of the atmosphere, the adaptive optics community developed a characteristic size given by Fried's coherence length (r_0),[5] typically around 10cm, and a characteristic time constant given by the reciprocal of the Greenwood frequency,[6] which is typically around 50Hz. Control theory says that the the first mechanical resonance of the

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mirror should be about one order of magnitude above the Greenwood frequency for sufficient control of the system. Furthermore, there should be roughly one actuator corresponding to each patch of sky equal in size to Fried's coherence length. Continuing the use of the Kolomogorov atmospheric turbulence model, Hudgin studied the optimal actuator influence function, which is the shape of the distortion an individual mirror actuator creates on the mirror surface.[7] Hudgin reported that to achieve equivalent residual wavefront error, almost 8 times more actuators were required if their influence functions were piston-only instead of gaussian in shape. Further work in the literature has shown a variety of different results in this regard, but there is always a significant improvement in modeled systems when a continuous influence function is used.[3] Tyson studied the ideal amount of crosstalk between adjacent actuators and found an optimum around 15%.[8]

With the success of adaptive optics in recent years, adaptive optics systems have found wider applicability and thus deformable mirror specifications have evolved. The design and fabrication of large-aperture terrestrial telescopes has added scalability to the list of deformable mirror characteristics. Designers want to use systems with not just one thousand actuators, but between ten thousand and one million actuators. Laser wavefront control is becoming more important as average output power levels increase due to thermal effects.[9] Applying deformable mirror technology to high power lasers means that the mirrors must at least be coated for high reflectivity with low absorption coatings. Finally, to widen the applicability of adaptive optics systems, the deformable mirror component must be inexpensive. All of these characteristics point away from hand assembly of mirrors and towards a mass-fabrication compatible construction like is offered with silicon micromachining.

Approach: Surface vs. Bulk Micromachining

Silicon micromachining can be divided into surface micromachining techniques and bulk micromachining techniques. Surface micromachining involves adding layers of different materials to a wafer surface and then using a wet etchant to remove one type of layer and release the structure. In the typical case where these layers are polysilicon and silicon dioxide, the wet etchant is hydrofluoric acid. Bulk micromachining always involves deep etches into the wafer, often completely through the wafer. Typically long etches in tetra-methyl ammonium hydroxide (TMAH) or potassium hydroxide (KOH) are used for removing large amounts of silicon with silicon nitride or silicon dioxide as an etch mask. In this section we will discuss the advantages and disadvantages of each of the fabrication methods as they apply to making deformable mirrors.

Silicon micromachining has been applied by several researchers to make silicon deformable mirrors because it offers several key advantages over bulk micromachining.[10,11] The major advantage is that there are several foundries available for fabrication of surface-micromachined devices.[12] This fact reduces the amount of time necessary for a given researcher's fabrication and reduces the financial burden of setting up a silicon fabrication facility. Furthermore, surface micromachining, like the CMOS process, offers enough flexibility for the designer to create fairly complex structures.

Although surface micromachining offers a very quick way to test architectures, sometimes the limitations of the process are critical to the success of a device. Making continuous surface mirrors with surface micromachining is not easy because the release step requires that there be an array of holes in the mirror's surface. There have been some backside release procedures proposed to avoid this problem, but they involve moving to a hybrid surface-bulk micromachining fabrication procedure, thus necessitating a clean room for fabrication and eliminating the major benefits of a foundry-based fabrication. Another limitation is the inability so far to easily integrate complex silicon circuitry with surface micromachined devices. This leads to large numbers of densely packed wires on a wafer, which could provide a fundamental limit to the scaling of these mirrors to large sizes. In addition to the large numbers of wires on a surface micromachined wafer without any circuitry, there is the further problem of getting connections to these wires off the chip. Finally, accumulated routhness and stresses induced during deposition of the layers make it difficult to achieve high quality mirror surfaces, even if the wafer is polished before the wet etch release step.[11]

Bulk micromachining, which has investigated by a few researchers for making deformable mirrors,[13] offers several advantages over surface micromachining. The biggest advantage of bulk micromachining is design freedom. Mirrors with continuous surfaces have been created for several years using this technique. Also, bulk micromachining offers avenues for integrate circuit with structures via wafer bonding, thus reducing the problems with wiring and contacts. Using silicon circuitry, large arrays of actuators can be addressed like random-access memory (RAM).

The major disadvantage of bulk micromachining is that it necessitates a clean-room for processing. Fortunately, there are several avenues for low-cost research and development using bulk micromachining. First, the National Science Foundation has established silicon fabrication facilities all over the United States called the National Nanofabrication Users Network (NNUN). These facilities have all the necessary silicon processing devices to a wide range of bulk micromachining and are

open to the public for a reasonable monthly fee. Similar facilities exist internationally as well. There are also many commercial facilities that will perform foundry work on wafers. This reduces the complexity of the clean room facility required for research and development substantially.

Deformable Mirror Architecture

For the deformable mirror device, we chose bulk micromachining over surface micromachining because it allowed us to create a continuous polished mirror surface that could be eventually able to be integrated with silicon circuitry. After selecting bulk micromachining, we then chose an architecture that would give us the most control of the mirror performance. We initially built a modified membrane mirror, but found that the architecture did not offer enough scalability or low enough crosstalk.[14] To address these problems, we added a third layer, called the intersitital or "bridge" layer, between the upper mirror membrane and the lower electrodes. The resulting architecture is shown in Figure 1. The interstitial layer provides a way to generate a local mechanical force upwards on each actuator to act against the electrostatic attraction force.

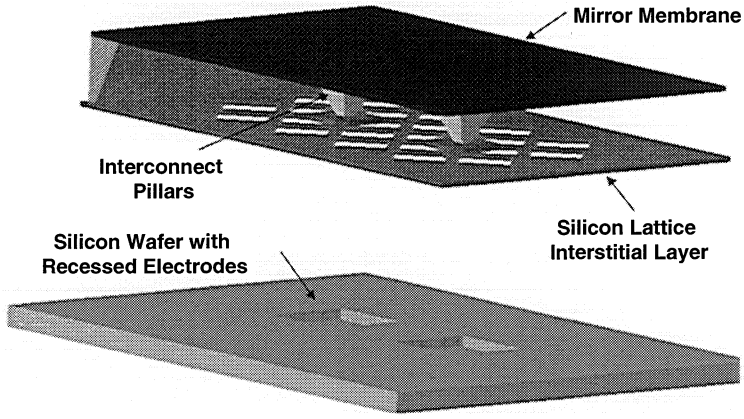

Figure 1 - Three dimensional rendering of the Stanford silicon deformable mirror architecture. The upper wafer, comprised entirely of single crystal silicon, is bonded to the lower silicon wafer, which has recessed electrodes.

Figure 2 shows a cross-sectional view of the deformable mirror operation. Each pillar attached to the upper mirror surface is also attached to the interstitial layer. The attachment of the lower interstitial layer to the recessed electrodes creates a small stiff plate. As a potential difference is established between the intersitital layer and one of the recessed electrodes, the electrostatic force attracts the interstitial layer and moves the upper mirror surface. The motion of the upper mirror surface pulls down on the pillars surrounding the actuated pillar. The surrounding plates formed by the intersection of the interstitial layer attached to the base of the pillars and the recessed electrodes provides a mechanical force upwards, thus localizing the deformation.

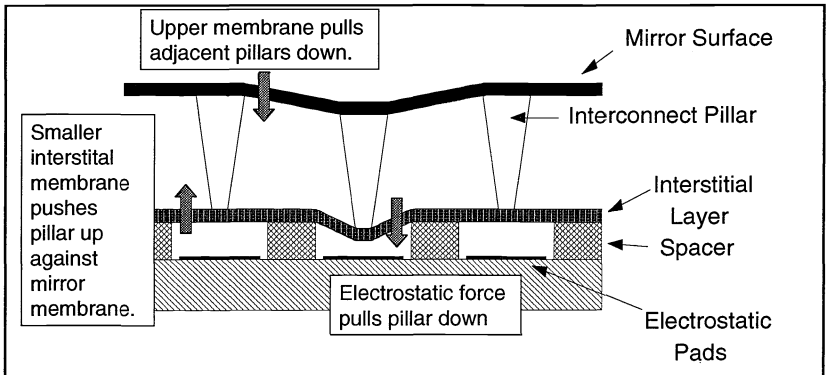

Figure 2 - Diagram of the operation of the deformable mirror.

Analytical Scaling Rules

Detailed numerical modeling of the performance of micromachined structures is difficult due to inaccuracies in the measurements of the dimensions and because small pieces of materials do not behave like bulk material due to surface effects. It is possible, however, to apply scaling law arguments based on mechanical analysis. We applied analytical mechanical analysis to the mirror to obtain scaling laws for the deflection, resonance frequency , and crosstalk.

We modeled the upper mirror layer and the lower interstitial layer as plates.[15] We first began by assuming that the lower plate formed by the intersection of the interstitial layer and the recessed electrode is much stiffer than the mirror plate, so the mirror plate could be ignored for deflection analysis. Using this approximation, we examined the maximum deflection of the interstitial layer and found that for a wide variety of edge conditions, the maximum deflection of a plate is governed by the relationship given by,

$$z_{\max} \propto F \cdot w^2 \frac{(1-\nu^2)}{E \cdot t^3} \quad (1)$$

where F is the applied force, w is the size of the suspended interstitial plate, E is Young's modulus, ν is Poisson's ratio, and h is the interstitial layer thickness. Adding in the scaling parameters for the electrostatic force, we obtain the relationship,

$$z_{\max} \propto \frac{w^4}{t^3 d^2} V^2 \quad (2)$$

where V is the applied voltage and d is the separation between the interstitial layer and the electrode. This relationship allows us to engineer the interstitial layer deflection.

Furthermore, this proportion allows us to define an effective spring constant for a plate, given by the ratio of the applied force, F, to the maximum deflection, z_{max}. The resonance frequency of a mechanical structure, determined by solving the differential equation resulting from equating Newton's second law and Hooke's law, is given by the square-root of the ratio of the spring constant to the mass. We can approximate the mass of a piece of the mirror as the product of the density, the thickness, and the area. Assuming the lowest frequency resonace is from the upper mirror membrane and using the variables defined in Figure 3, the lowest resonance frequency is proportional to the thickness of the mirror membrane divided by the actuator spacing squared, or t/s^2.

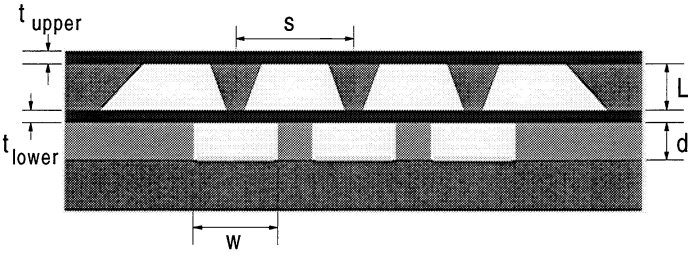

Figure 3 - Definition of the variables used in the mechanical analysis of the deformable mirror.

Finally, we were interested in determining a relationship for the inter-actuator coupling or crosstalk. We modeled the upper and lower membranes as coupled plates. A force applied down in the center of the mirror plate has to be counteracted by forces from the adjacent pillars upwards, each with magnitude equal to the force down divided by the number of neighboring actuators sharing the force. This restoring force must be obtained mechanically through the deflection of the adjacent actuators, and thus creating crosstalk. We can write the coupling as a ratio of the motion of the adjacent actuators relative to the central actuator. In reality, we are applying a deflection to the upper mirror layer via the pillar. Using the relationship given above in Equation (1) relating deflection and force to the upper mirror layer and the variables as defined in Figure 3, we can derive the a scaling relationship for the inter-actuator coupling,η, given by,

$$\eta = \frac{z_{adjacent}}{z_{central}} = \frac{F/k_i/N}{F/k_m + F/k_i/N} = \frac{k_m}{k_m + N \cdot k_i} \propto \frac{t_{upper}^3/s^2}{t_{upper}^3/s^2 + N \cdot t_{lower}^3/w^2} \quad (3)$$

where $z_{adjacent}$ is the deflection of the adjacent interstitial layer, $z_{central}$ is the deflection of the upper mirror layer, F is the force required to deflect the mirror layer, k_i is the effective spring constant of the interstitial membranes, k_m is the effective spring constant of the upper mirror layer, N is the number of neighboring actuators, w is the size of the interstitial membrane, s is the spacing between actuators, t_{lower} is the thickness of the interstitial layer, and t_{upper} is the thickness of the mirror layer.

Fabrication

The fabrication of the silicon deformable mirror presented above requires three mask steps and only one alignment. The upper piece in Figure 1, henceforth called the mirror wafer, consists of the mirror surface on one side and the latticed interstitial membrane. The bottom piece in Figure 1, henceforth called the electrode wafer, contains metal electrode pads

recessed slightly below the wafer's surface and is made separately from the mirror wafer. In this section we will describe the fabrication procedure we used and then discuss some possible variations on the procedure.

The mirror wafer fabrication begins by coating the front and back surface of a double-side polished silicon wafer with 10 microns of epitaxial silicon that has been doped heavily with boron (~10^{20}/cm^3) and counter doped with germanium for stress reduction. Then the wafer is coated with a layer of silicon nitride at least 50nm thick for protection in the subsequent wet etches. The silicon nitride is patterned with the lattice pattern shown in Figure 1 using photolithography and a CF_4/O_2 plasma etch. After removing the photoresist in acetone, the wafer is placed in a mixture of hydrofluoric acid, nitric acid, and water (5:200:100), to transfer the pattern into the heavily doped silicon layer. Then the wafer is rinsed and placed into a bath of 20wt% potassium hydroxide (KOH) saturated with isopropanol at 75°C until the desired structure is achieved. This typically takes 28 hours for a 500 microns thick wafer. By properly patterning the heavily doped silicon, the KOH etches the silicon underneath it, but leaves pillars interconnecting the layers.

The anisotropic nature of the KOH was studied carefully before selecting this mixture of KOH. Although it is well known that adding isopropanol and lowering the concentration of KOH reduces the etch rate of the solution on heavily doped silicon,[16] we could not find information on how the anisotropy changes while changing KOH concentration with and without the presence of isopropanol. Figure 4 shows the etch rates we measured with respect to angle from the <110> crystallographic plane for various concentrations of aqueous KOH saturated with isopropanol. We decided upon using 20 wt% KOH by using this anisotropy data in conjunction with the known enhanced selectivity to heavily boron doped silicon in the presence of isopropanol. This etch stops undercutting on <111> planes instead of <411> planes, thus forcing our spacing between actuators to be about 3mm for a 500 micron thick wafer. We would ideally like to have used KOH without isopropanol because its enhanced <411> etch rates would produce steeper sidewalls, but we could not afford to lose too much of the heavily doped silicon since it is exposed to the KOH during the entire etch.

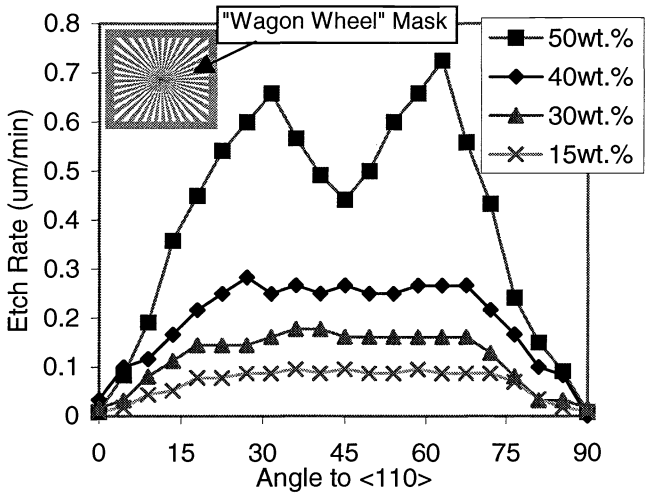

Figure 4 - Anisotropy of potassium hydroxide etchant relative for various concentrations of aqueous solution saturated with isporopanol. The data was taken from the undercutting of the spokes of the "wagon wheel" mask pattern shown in the upper left.

Upon completion of the KOH etch, we rinse the wafer and dried it in an oven at 120°C. We found that it is essential to thoroughly rinse the wafer because the KOH solution tends to stick well to the silicon and produce crystals that stress the membrane during drying. We found that employing a piranha etch (4:1 sulfuric acid to hydrogen peroxide) further cleaned the wafer. We then removed the nitride layer with a long 160°C phosphoric acid bath and coated the mirror surface with a 200nm layer of chrome/gold for both reflectivity and conductivity. We initially were coating the backside as well, but found that uneven stresses induced by evaporating the gold coating through the lattice interstitial layer warped the mirror surface.

To fabricate the electrodes wafer, we begin by spinning a thick layer of AZ4620 photoresist onto the rough back surface of a single-side polished silicon wafer. We then pattern the photoresist and etch the underlying silicon in a CF_4/O_2 plasma to create the recesses. After removing the photoresist, the wafer is placed into a 900°C oven in room air for 10 hours to grow 100nm of silicon dioxide as an insulation layer. Finally, gold electrodes and wires are placed in the recesses using a lift-off process.

The final deformable mirror device is formed by combining the mirror and electrode pieces. We have thus far used epoxy on the edge of the mirror to bond the pieces together. We are now also assembling some mirrors by putting epoxy in holes made through the electrode wafer to prevent edge stresses from buckling the structure. Conductive epoxy is used to make the electrical connection to the mirror. An array small spring-loaded copper pins is used in our experimental setup for making all the mirror connections at once.

Although we decided to use silicon in the mirrors we fabricated, there are many different material variations which may offer significant advantages. For example, for high power laser work, a transparent mirror membrane may allow light that is not reflected by a multi-layer dielectric (MLD) to transmit through the mirror without being absorbed and causing distortions. Although silicon is transparent beyond about 1.3 microns, other materials may be better for visible or near infrared light. Furthermore, there are other ways to fabricate this type of structure using bulk micromachining, which we are currently investigating.

Deformable Mirror Characterization

Figure 5 shows a typical optical setup used to characterize our deformable mirrors. The setup allows interferometry, wavefront sensing, and examination of the point-spread function (PSF). A helium-neon laser is split into two beams with a 50% reflectivity beam splitter. One beam propagates through a telescope that has been setup to reimage the beam splitter without adding curvature onto the deformable mirror. When doing interferometry on the mirror surface, the other beam reflects off a flat static mirror and interferes with the beam from the mirror on a CCD.

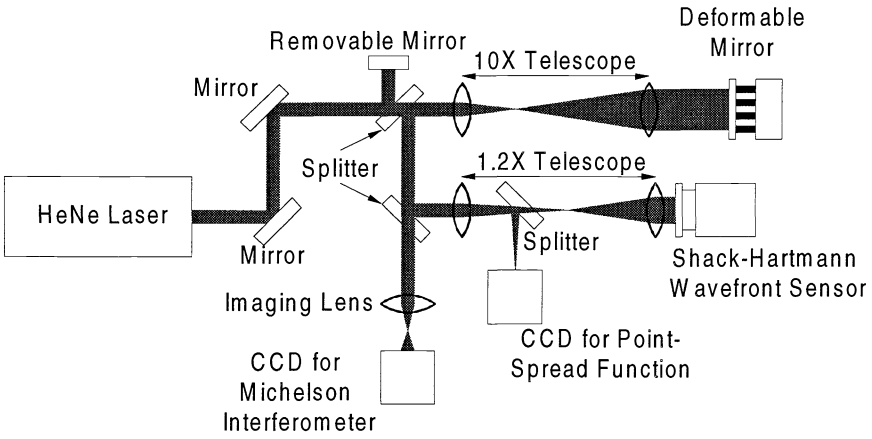

Figure 5 - Experimental setup for testing silicon deformable mirrors that allows for Michelson interferometry, Shack-Hartmann wavefront sensing, and the examination of the point-spread function (PSF).

When doing wavefront sensing or PSF measurements, the second arm is blocked to avoid interference. For these measurements, the light from the deformable mirror is reimaged onto the Shack-Hartmann wavefront sensor with a telescope designed to magnify the image, but not to add curvature to the wavefront. A beam splitter inside the telescope sends the focus in the telescope to a CCD for evaluation of the point spread function.

We have tested several different deformable mirrors. We first used a network analyzer and a photodiode to measure a mechanical resonance frequency of about 2kHz. Using the setup in Figure 5, we measured the actuator's influence functions on the Shack-Hartmann wavefront sensor and found about 30% crosstalk between adjacent actuators. The amplitude of the deformation was about one micron for 200V of applied potential difference. The gold-coated silicon mirror surface demonstrated the capability of sustaining more than 250kW/cm^2 of CW 1064nm laser light. The surface micro-roughness of the mirror is effectively that of the initial silicon wafer because the mirror surface is sealed in silicon nitride before the processing begins so the surface is sealed from the etch.

The mirror flatness was measured first using a Michelson interferometer and then for more quantitative results using a Shack-Hartmann wavefront sensor. The all-silicon mirror wafers suffered from print-through of the lattice structure of the interstital layer due to insufficient etch selectivity of the heavily doped silicon and the low doped silicon. Furthermore, there was some low-spatial frequency aberrations in the mirror. We built a mirror wafer with a tensile silicon nitride mirror to try to pull the mirror surface flat. The silicon nitride mirror surface had no observable print-through of the lattice pattern and had noticeably less aberration when measured by the interferometer. The primary aberrations in the silicon nitride mirror surface were caused by an imbalance in the film stress between the mirror and intersitital layers of the mirror wafer due to patterning of the interstitial layer. We believe that actuating the mirror surface could compensate the other low spatial frequency aberrations in the surface.

CMOS-BASED SHACK-HARTMANN WAVEFRONT SENSORS

CMOS imaging sensors are becoming more prevalent in industry because they are inexpensive and allow signal-processing circuitry to be incorporated onto the sensor chip. Yang demonstrated an 8-bit digital 640 by 512 digital pixel sensor (DPS)

CMOS imager with a 250 Hz frame rate.[17] This imager was the first to dedicate a non-sigma-delta analog-to-digital converter (ADC) to every pixel improving measurement repeatability and eliminating timing issues from the digitization process. While past CMOS imagers have typically been too noisy for scientific applications, the high digitization accuracy and high frame rate of this CMOS imager lends itself well to some scientific applications, like measuring the spatial phase of light by using the imager to build a Shack-Hartmann wavefront sensor.

The Shack-Hartmann wavefront sensor is being used more frequently for measuring the spatial phase of light.[18] These wavefront sensors are built by placing an imaging sensor, which we will henceforth call an imager, at the focus of an array of micro-optic lenses. The average slope of the wavefront is measured over each lens by determining the change in the position of the focal spots relative to a reference position and dividing this spot displacement by the separation between the imager and the lens array. The wavefront is then determined by integrating the array of measured wavefront slopes.

Recently, other researchers have proposed using CMOS chips as the detector arrays for the Shack-Hartmann wavefront sensor. They proposed using a single position sensitive detector behind each lens of a Shack-Hartmann wavefront sensor.[19] For some applications this offers a distinct advantage, like the high spatial resolution application,[20] but for general purpose wavefront sensing as is used in adaptive optics, we believe that it will be less expensive to leverage off the growing CMOS imager market.

Advantages of CMOS imagers over CCD imagers

CMOS imagers have the potential to be cheaper, faster, and more accurate than CCD arrays because they use conventional technology under continual development by integrated circuit manufacturers. Although CCD imagers are fabricated using silicon-processing technology similar to CMOS chips, CCD arrays cannot be made using the conventional CMOS process. Therefore CCD arrays have not been able to integrate much signal-processing electronics onto the same chip or benefit from CMOS speed increases. Furthermore, there are many more CMOS foundries internationally than there are CCD array foundries because of the larger need for standard CMOS integrated circuits. All of these reasons will make CMOS based devices more attractive in the next decade.

The integration of electronics onto a CMOS chip is especially important for scientific applications like adaptive optics and wavefront sensing since it allows data reduction to happen on the chip thereby reducing the amount of data needed to be transmitted off the chip and increasing system speed. Furthermore, the integration of photodiodes and CMOS circuitry with MEMS technology offer the potential for constructing complex optical systems, like those used for adaptive optics, onto a single CMOS chip.

The CMOS Imager

The CMOS imager used in these experiments integrates an array of photodiode pixels and the associated signal conditioning and readout electronics on a single silicon chip. The 640 by 512 pixel CMOS imager features a Nyquist rate pixel-level ADC.[17] Each 2 by 2 pixel cell shares a single ADC circuit comprising a comparator and a one-bit latch. The readout is done one pixel quadrant at a time. The sensor is fabricated using a standard 0.35 micron, 4-layer metal, 1-layer poly, n-well digital CMOS process. The pixel consists of a nwell/psub photodiode and 5.5 transistors. It uses three layers of metal for interconnects and the 4th metal layer as a light shield. The pixel area is 10.5 by 10.5 microns, of which 29% is exposed to light. The fill factor, which is the fraction of pixel area occupied by the photodiode, is 8%. The external quantum efficiency of the photodiodes measured at 610nm is 42%. The internal quantum efficiency taking into account the approximately 30% Fresnel reflection off the chip surface at 610nm is roughly 55%.

Measurements made on the imager after fabrication show that each of the four photodiodes in a cell had different fixed pattern noise manifesting itself as a gain offset between photodiodes varying by about 10 percent. Corresponding photodiode pixel in the other cells on the chip had the same response within a fraction of a percent. To eliminate the effect of the relatively large gain variation between pixels in a cell on our measurement, images were taken from the CMOS imager using only one of the four pixels from each cell unless otherwise noted. The major limiting factor in the speed of this device is the ability to transfer data off of the chip. By adding processing circuitry to the chip to reduce the measured intensity data into focal spot positions, it may be possible to achieve even faster frame rates for Shack-Hartmann wavefront sensing.

Imager Noise

A wide variety of noise sources encountered in the acquisition of an image affect the accuracy of a Shack-Hartmann wavefront sensor. We will divide the noise sources into temporal intensity noise and spatial or fixed-pattern noise. In both CMOS and CCD array imagers, common causes of temporal intensity noise are the amplification electronics, which can be

attributed to thermal noise, 1/f noise, and quantization noise. Analog output CCD array imagers can additionally have temporal intensity noise due to timing fluctuations of the synchronization pulse. In both CMOS and CCD array imagers, pixel-to-pixel gain variations and chip fabrication errors can cause fixed pattern noise.

To separate the effects of two different types of noise sources, we devised two tests for Shack-Hartmann wavefront sensors. The first test, which we will call the temporal noise test, is designed to determine the effect of the temporal intensity noise on the performance of the Shack-Hartmann wavefront sensor. The temporal noise test is designed to determine the behavior of the Shack-Hartmann wavefront sensor when measuring fairly small aberrations from a flat reference. The performance of the wavefront sensor in this regime is important for adaptive optics applications, which are constantly driving the wavefront back towards a reference position. The second test, which we will call the spatial noise test, is designed to measure the effects of fixed-pattern noise on the wavefront sensor performance. The spatial noise test is important for applications like optical metrology where the Shack-Hartmann wavefront sensor is measuring large variations from a planar wavefront.

Shack-Hartmann Wavefront Sensor Characterization Tests

To perform the temporal noise test, we illuminated the Shack-Hartmann wavefront sensor with a beam of fairly uniform intensity and a planar wavefront. We compared a set of ten individual frames to the average of all the frames while illuminating the sensor with a planar wavefront. During this test, the spots do not move, but apparent motion is detected by the wavefront sensor due to temporal noise in the measurement of the intensity. The RMS fluctuation of the focal spot positions determines the limit of the sensor's ability to measure wavefront slope and, therefore, the wavefront itself. Although temporal noise in the intensity measurements can be averaged out over a series of frames, use of Shack-Hartmann wavefront sensors to obtain high-speed wavefront measurements, like in adaptive optics, make such averaging impossible.

To perform the spatial noise test, a set of frames is taken while changing the radius of curvature of a fairly uniform intensity beam over the full wavefront slope range of the sensor. The maximum wavefront slope of the Shack-Hartmann wavefront sensor is reached when the focal spots move to the edge of the lens diameter. While this is not an unavoidable limit, it is a practical limit.[21] Mathematically, this means that the maximum slope that can be measured in the x direction is given by,

$$\left.\frac{\partial \phi}{\partial x}\right|_{\max} = \frac{d/2 - f\lambda/d}{f} \qquad (4)$$

where d is the lens diameter, f is the lens focal length, and λ is the wavelength of the light. For example, a Shack-Hartmann wavefront sensor built with a 23.3mm focal length lens array with 252-micron diameter lenses measuring with 633nm light has a maximum wavefront slope of 3 milliradians. Assuming that the wavefront was spherical, the minimum absolute value of the radius of curvature that can be measured by a Shack-Hartmann wavefront sensor is given by,

$$\left|R_{\min}\right| = \frac{r_{camera}}{\left.\partial \phi / \partial x\right|_{\max}} \qquad (5)$$

where r_{imager} is the farthest distance from the center of the radius of curvature seen by the imager. For the example given above with r_{imager}=5mm, the minimum radius of curvature is ±1.67 meters.

The spatial noise test is performed by acquiring a set of frames for each of a variety of different wavefront radii of curvature spanning the entire range observable by the sensor. The set of frames is then averaged together to minimize the effects of temporal intensity noise. Ideally, the reconstructed wavefront would be perfectly planar after removing the low-order Zernike terms like focus, coma, and spherical aberration, which are almost entirely unavoidable when performing the test with standard spherical optics and using a high sensitivity wavefront sensor. As the spots move off the pixels used to calculate their position in the reference and onto new pixels, variations in the response of the pixels (fixed-pattern noise) changes their calculated position. This effect causes the wavefront sensor to measure a non-zero RMS wavefront error relative to a planar wavefront after removing the lower order Zernike terms from the wavefront and performing a zonal reconstruction on the residual wavefront slopes. In addition to fixed pattern noise in the imager, another source of noise is the diffraction patterns of adjacent lens adding coherently[22]. Our modeling of coherent crosstalk from previous work[22] indicates that for our experiments we are in a regime where the effects of coherent crosstalk are much smaller than the fixed pattern noise, so they will be neglected here.

We found experimentally that the RMS wavefront deviation from a planar wavefront increases linearly with the reciprocal of the radius of curvature. Therefore, to characterize the wavefront sensor performance we fit the RMS wavefront error to the curve given by,

$$\varphi_{RMS} = \left| \frac{A}{ROC} \right| \qquad (6)$$

where ϕ_{RMS} is the RMS wavefront error relative to a planar wavefront, ROC is the radius of curvature, and A is a fit coefficient given in units of nm·m.

Although we could perform this test by varying the wavefront tilt, we have found several reasons to vary the wavefront curvature instead. From a practical standpoint, it is easier to obtain translation stages and lenses than it is to obtain a precision tilt stage. Adjusting the wavefront curvature gives a wide variety of tilt magnitudes and directions. Furthermore, an attractive feature of this test is that it is procedurally identical to the test used to extract the separation between the lens array and the imager, so taking additional data is not necessary.

Experimental Results

We compared the performance of a Shack-Hartmann wavefront sensor built with a CMOS photodiode array imager to one built with a CCD array imager. Figure 6 shows the experimental setup for testing the two different imagers as components of a Shack-Hartmann wavefront sensor. A collimated helium-neon laser illuminates two 50mm focal length lenses separated by 100mm. The collimation of the HeNe beam after the lens pair was verified using a shear plate. The lens closest to the laser is on a translation stage allowing the radius of curvature at the output to be varied. Then the beam propagates 90mm and illuminates an array of 252-micron diameter 23.3mm focal length lenses. The focal plane of the lenses is re-imaged onto the imager with a 150mm focal length lens such that the magnification of the focal plane image is 1.87. Approximately one hundred focal spots were present on the imager.

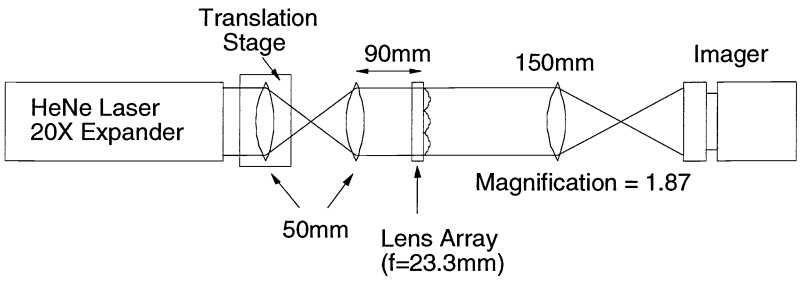

Figure 6 - Experimental setup for testing different imagers as Shack-Hartmann wavefront sensors. The pair of 50mm lenses are used to control the radius of curvature. The 150mm focal length lens is used to reimage the focal plane of the lens array onto the imager.

Two different imagers were compared in the experiments. The first imager was a Sony XC-75 charge-coupled device (CCD) array using the RS-170 communication standard and digitized with a Matrox Meteor frame grabber card. Using the RS-170 output standard limits the signal to noise ratio to about 6.5 bits. The second imager was a digital CMOS photodiode array designed and assembled at Stanford University, which achieved 8 bits of signal to noise ratio.

Calibration

Each wavefront sensor was calibrated by making a series of measurements of the HeNe laser wavefront for several different radii of curvature. Using ray optics we find that for the optical setup in Figure 6, the radius of curvature, R, of a beam at the lens array is given by,

$$\frac{1}{R} = \frac{-d}{f}\left(\frac{f^2}{f^2 + df - Ld}\right) \qquad (7)$$

where f is the lens focal length, d is the displacement of the first lens in the pair from 2f separation, and L is the distance from the second lens in the pair to the lens array. The separation between the imager and the lens array was initially assumed to be equal to the focal length of the lens array. After obtaining a series of measurements of the radius of curvature at different separations between the two leneses, we fit the data to Equation (1) and extracted the actual separation between the lens array and each imager. The CCD array to lens array separation was 22.04mm and the CMOS imager to lens array separation was 23.17mm.

Temporal Noise Test

We performed the temporal noise test on both the CCD and the CMOS Shack-Hartmann wavefront sensors. The RMS centroid error performance was almost identical for each of the cameras in the orthogonal axes, so we will only report the x-axis results. The RMS centroid error averaged over the 10 frames was 353±21 nm for the CCD imager, 130±26 nm for the quarter frame CMOS imager, and 58±5.3 nm for the full-frame CMOS imager. From these results, we can conclude that the CMOS imager has less intensity digitization noise.

Spatial Noise Test

A set of ten frames was taken at ten different radii of curvature by moving the lens on the translation stage in one-millimeter steps. The measured intensity patterns at each radii of curvature were averaged together to minimize the effects of temporal intensity noise. The wavefront slope data was then fit using a fourth-order Zernike and all these terms were subtracted from the wavefront slopes. The residual wavefront slope, now devoid of the low-order Zernike terms was reconstructed using a cubic-spline reconstructor.[23] The wavefront sensor's aperture was constrained to an array of 8 by 10 lenses centered on the wavefront radius of curvature to avoid exceeding the maximum wavefront slope measurable by the wavefront sensor. The RMS wavefront error measured relative to a planar wavefront was used to compare the different imagers. Figure 7 shows the RMS wavefront error relative to planar with respect to the separation of the lenses from a planar output. The coefficient of the fit using equation (3) above is 42.1 nm·m for the CMOS imager and 38.1 nm·m for the CCD imagers. The RMS optical path length difference for the CMOS imager and the CCD imager were similar for different input curvatures indicating that the pixel intensity measurements of the two imagers were comparable in uniformity.

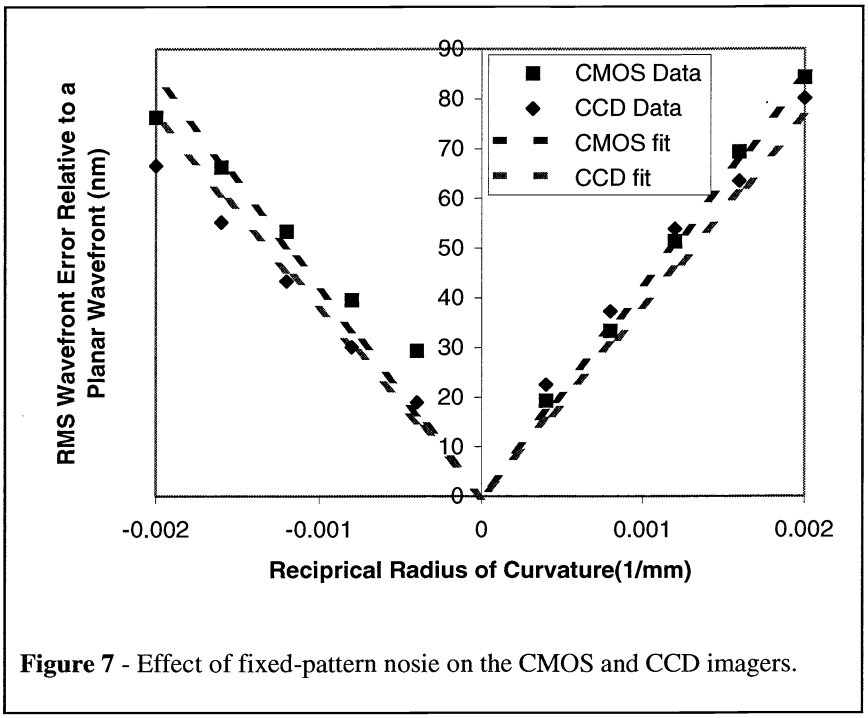

Figure 7 - Effect of fixed-pattern nosie on the CMOS and CCD imagers.

CONCLUSIONS

We have demonstrated a new type of silicon deformable mirror and a CMOS-based Shack-Hartmann wavefront sensor. The Shack-Hartmann wavefront sensor built using a CMOS imager demonstrated lower temporal noise than a CCD-based wavefront sensor, but was only comparable to the CCD in fixed-pattern noise effects. The new type of silicon deformable mirror built using bulk micromachining offers a design that is both scalable and able to be integrated with silicon circuitry, thus opening the possibility of a full adaptive optics system on a single silicon chip.

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