Lecture 6

Technology Trends and Modeling Pitfalls: Transistors in the "real world"

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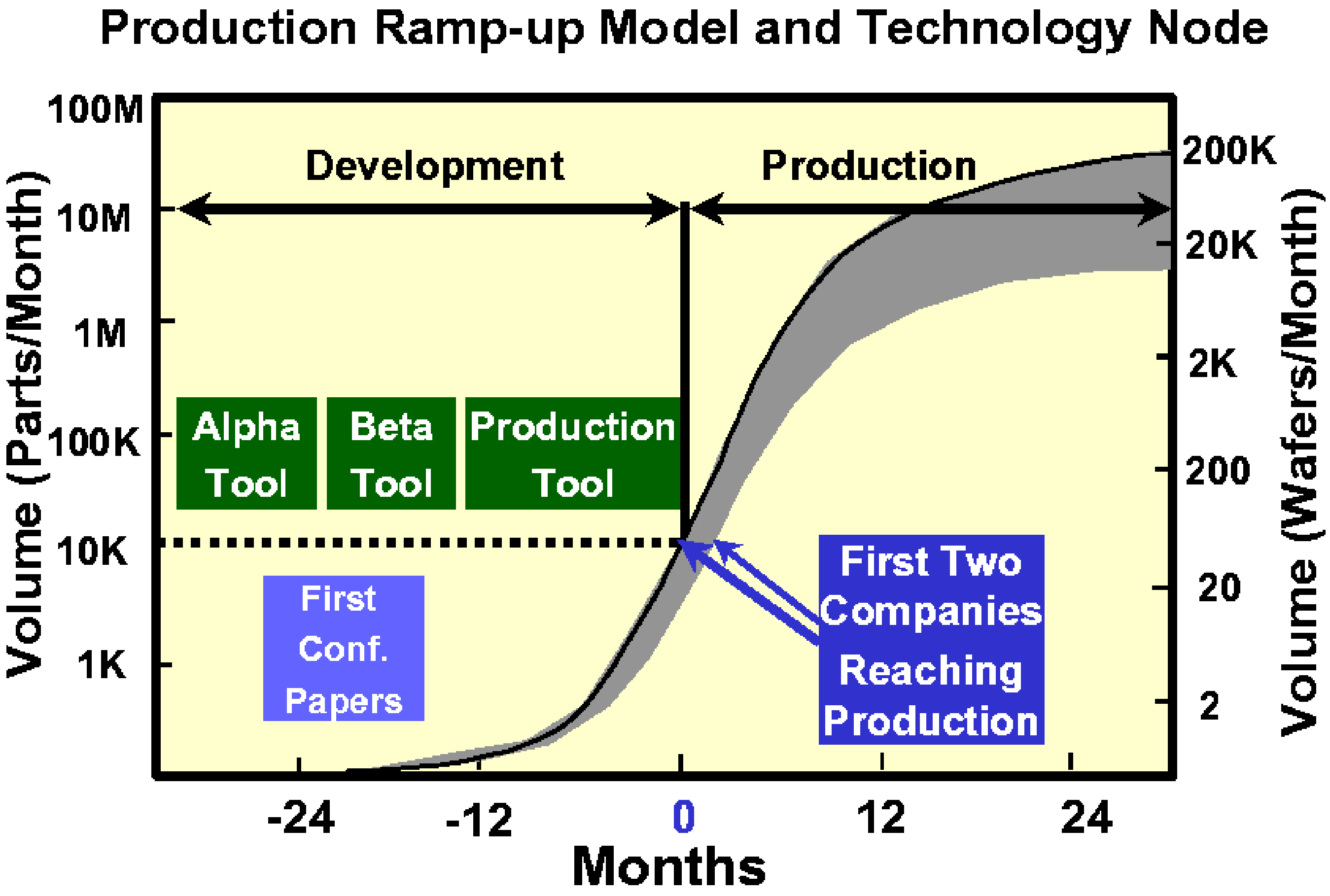
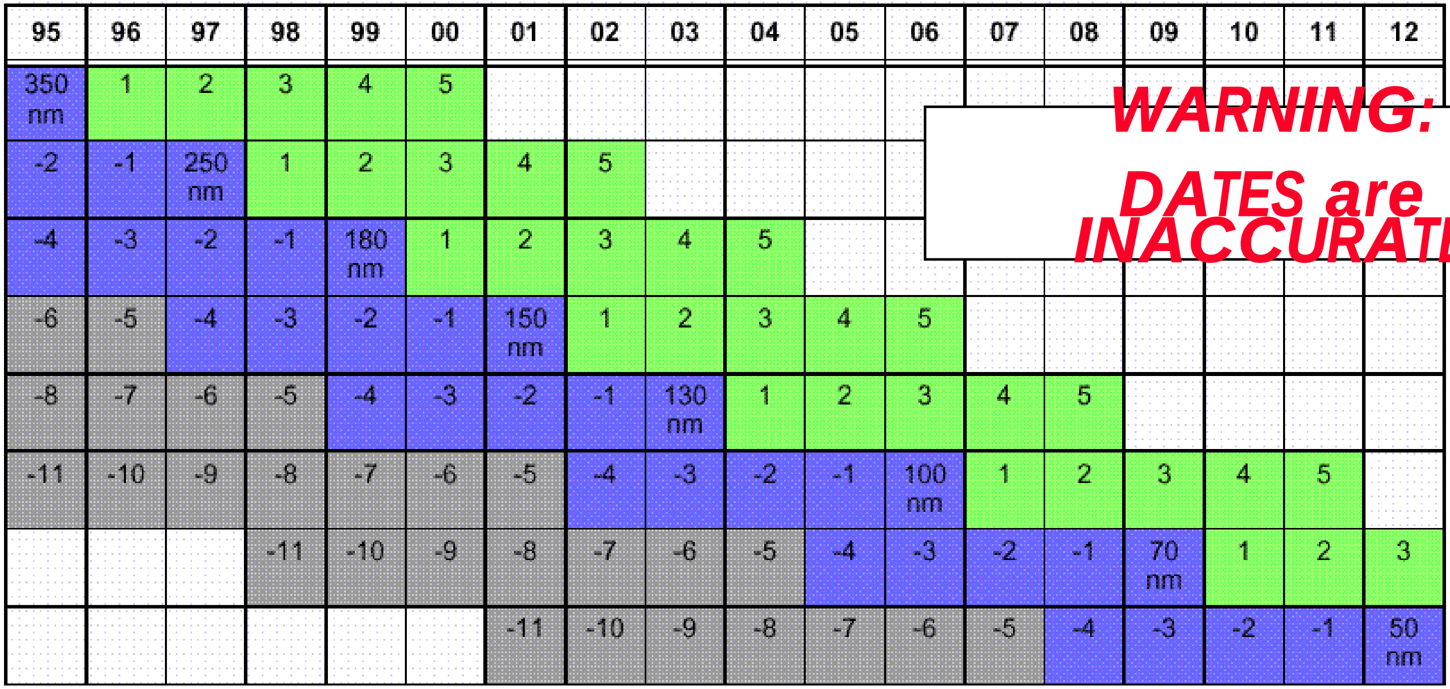
Overview

- CMOS technology trends
- MOS Modeling in industry
- EKV model
- Circuit design advice

ITRS Node production ramp



CMOS Technology generations *(OLD : ‘99NTRS)*



95	96	97	98	99	00	01	02	03	04	05	06	07	08	09	10	11	12
350 nm	1	2	3	4	5												
-2	-1	250 nm	1	2	3	4	5										
-4	-3	-2	-1	180 nm	1	2	3	4	5								
-6	-5	-4	-3	-2	-1	150 nm	1	2	3	4	5						
-8	-7	-6	-5	-4	-3	-2	-1	130 nm	1	2	3	4	5				
-11	-10	-9	-8	-7	-6	-5	-4	-3	-2	-1	100 nm	1	2	3	4	5	
			-11	-10	-9	-8	-7	-6	-5	-4	-3	-2	-1	70 nm	1	2	3
						-11	-10	-9	-8	-7	-6	-5	-4	-3	-2	-1	50 nm

WARNING: DATES are INACCURATE

- Research (7), Development (5), Manufacturing (5)
- Technologies span ~17 years: unlikely to be totally surprised
- The rate at which things change is what’s debatable

Technology Scaling & Moore's Law

- Scaling is extremely well predicted & controlled
- Driven by Moore's Law *# of DRAM bits <u>4X every 3 years</u>*

Technology (2x) X Diesize (1.4x) X Innovation (1.4x) = 4X

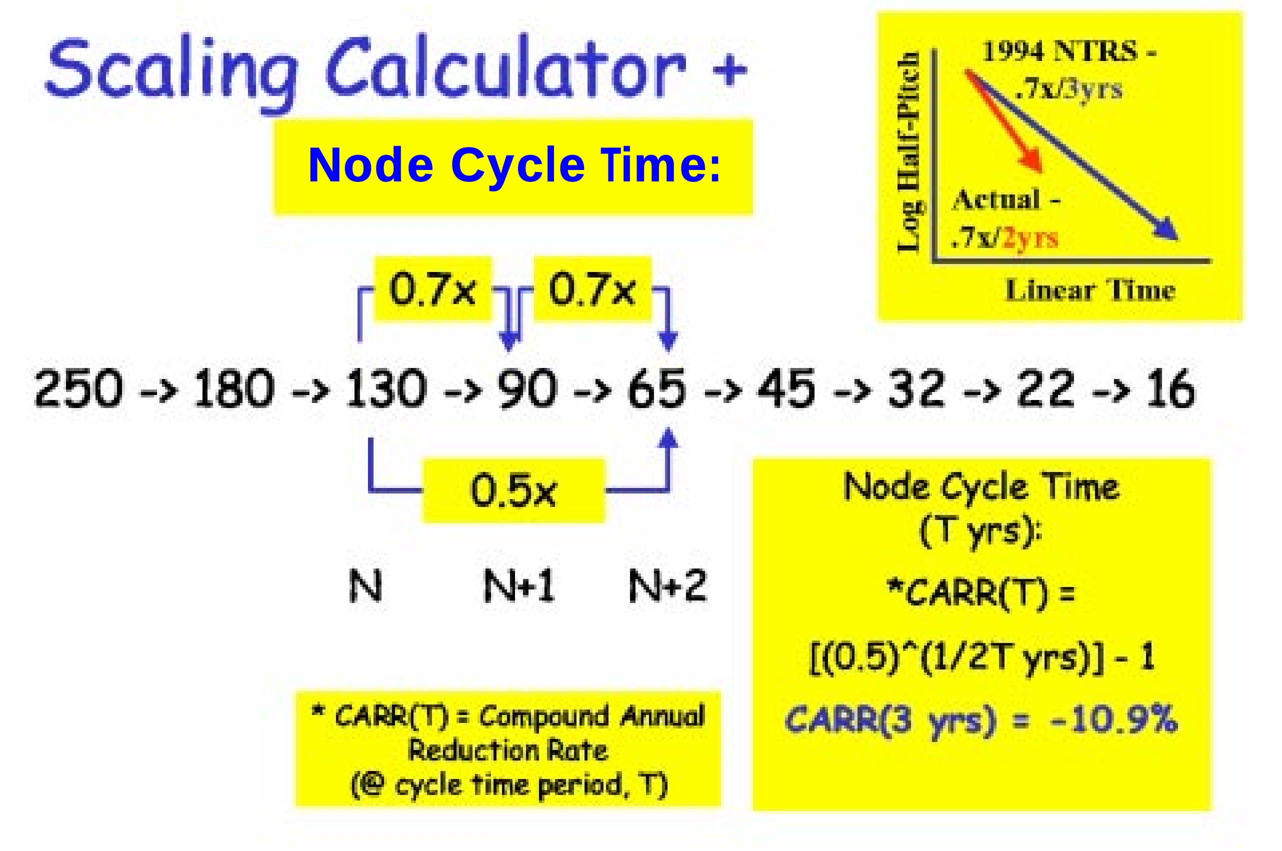
- – BUT

Technology now making up for diesize (die per wafer) limits

=> Technology has been <u>2x every two years</u> since 1995

=> Allows Diesize to remain virtually constant

Technology Scaling & CARR



Scaling Calculator +

Node Cycle Time:

0.7x 0.7x

250 -> 180 -> 130 -> 90 -> 65 -> 45 -> 32 -> 22 -> 16

0.5x

N N+1 N+2

* CARR(T) = Compound Annual Reduction Rate
(@ cycle time period, T)

Node Cycle Time
(T yrs):
*CARR(T) =
[(0.5)^(1/2T yrs)] - 1
CARR(3 yrs) = -10.9%

- This is important : lots of time & $$ spent to keep it on track!

ITRS Predicted Logic Technology Characteristics

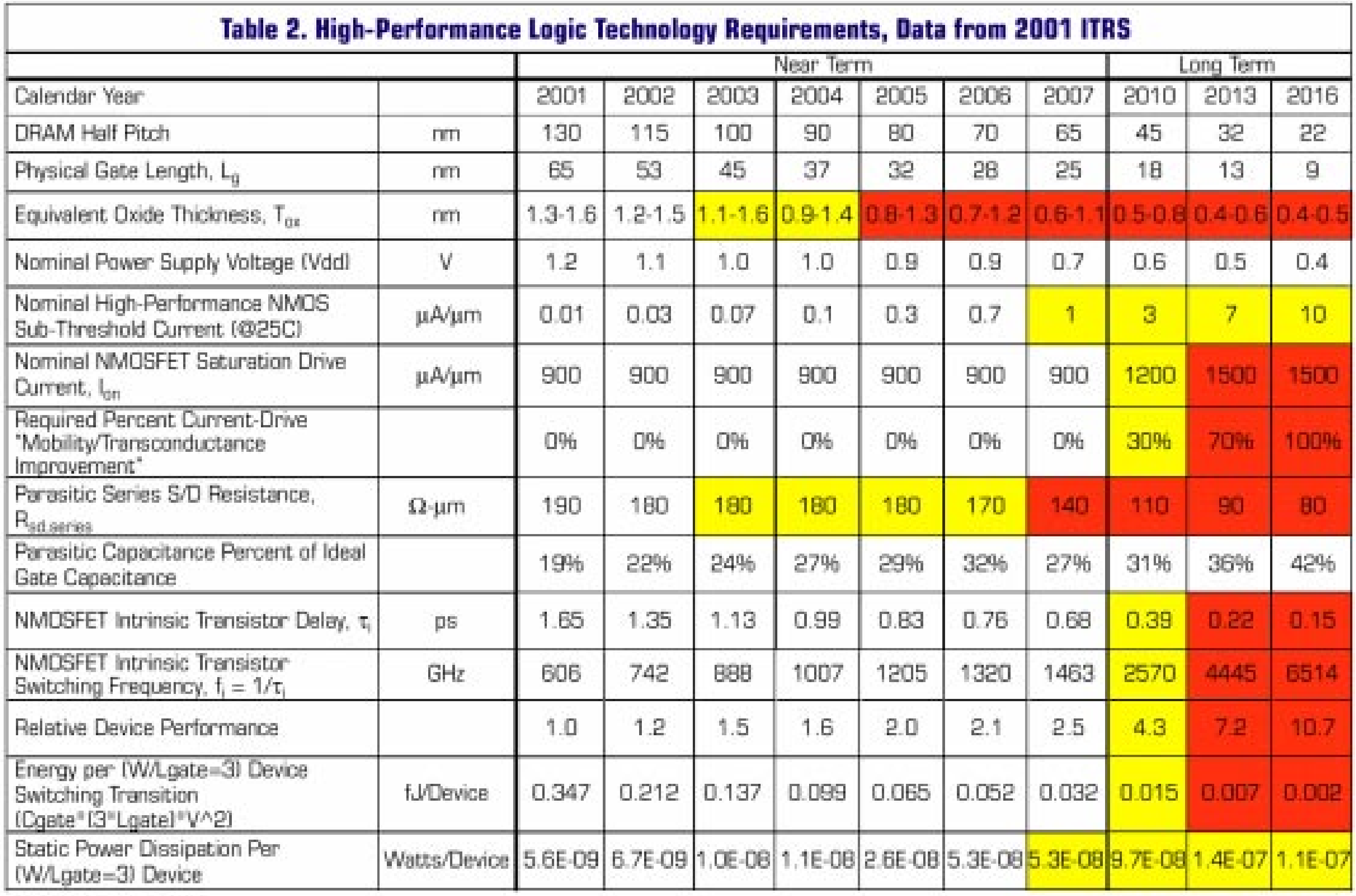
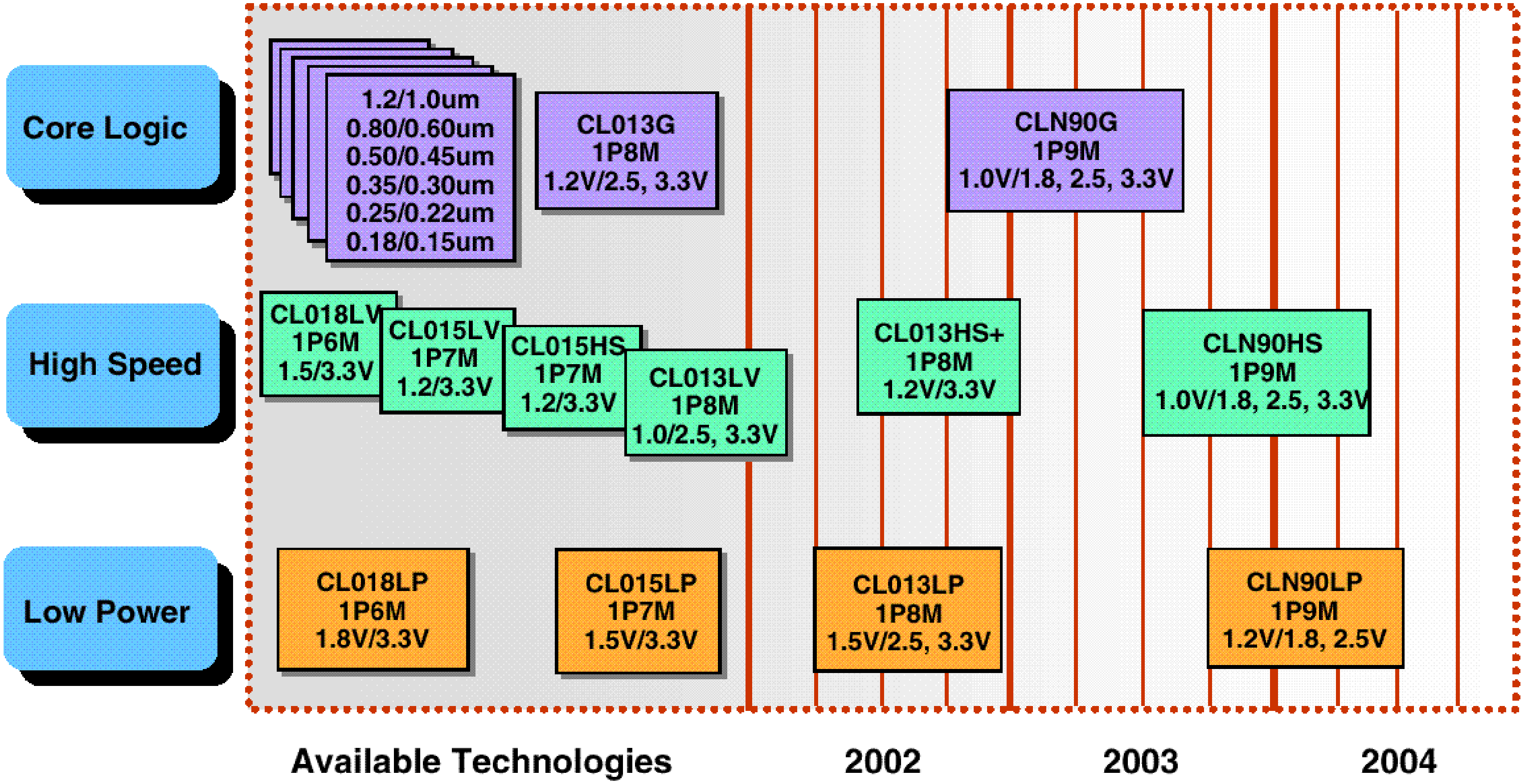


Table 2. High-Performance Logic Technology Requirements, Data from 2001 ITRS

		Near Term							Long Term		
Calendar Year		2001	2002	2003	2004	2005	2006	2007	2010	2013	2016
DRAM Half Pitch	nm	130	115	100	90	80	70	65	45	32	22
Physical Gate Length, L_g	nm	65	53	45	37	32	28	25	18	13	9
Equivalent Oxide Thickness, T_{ox}	nm	1.3-1.6	1.2-1.5	1.1-1.6	0.9-1.4	0.8-1.3	0.7-1.2	0.6-1.1	0.5-0.8	0.4-0.6	0.4-0.5
Nominal Power Supply Voltage (Vdd)	V	1.2	1.1	1.0	1.0	0.9	0.9	0.7	0.6	0.5	0.4
Nominal High-Performance NMOS Sub-Threshold Current (@25C)	µA/µm	0.01	0.03	0.07	0.1	0.3	0.7	1	3	7	10
Nominal NMOSFET Saturation Drive Current, I_{on}	µA/µm	900	900	900	900	900	900	900	1200	1500	1500
Required Percent Current-Drive "Mobility/Transconductance Improvement"		0%	0%	0%	0%	0%	0%	0%	30%	70%	100%
Parasitic Series S/D Resistance, $R_{sd,series}$	Ω-µm	190	180	180	180	180	170	140	110	90	80
Parasitic Capacitance Percent of Ideal Gate Capacitance		19%	22%	24%	27%	29%	32%	27%	31%	36%	42%
NMOSFET Intrinsic Transistor Delay, τ_i	ps	1.65	1.35	1.13	0.99	0.83	0.76	0.68	0.39	0.22	0.15
NMOSFET Intrinsic Transistor Switching Frequency, $f_i = 1/\tau_i$	GHz	606	742	888	1007	1205	1320	1463	2570	4445	6514
Relative Device Performance		1.0	1.2	1.5	1.6	2.0	2.1	2.5	4.3	7.2	10.7
Energy per (W/Lgate=3) Device Switching Transition (Cgate*(3*Lgate)*V^2)	fJ/Device	0.347	0.212	0.137	0.099	0.065	0.052	0.032	0.015	0.007	0.002
Static Power Dissipation Per (W/Lgate=3) Device	Watts/Device	5.6E-09	6.7E-09	1.0E-08	1.1E-08	2.6E-08	5.3E-08	5.3E-08	9.7E-08	1.4E-07	1.1E-07

TSMC Process Roadmap



Core Logic

1.2/1.0um
0.80/0.60um
0.50/0.45um
0.35/0.30um
0.25/0.22um
0.18/0.15um

CL013G
1P8M
1.2V/2.5, 3.3V

CLN90G
1P9M
1.0V/1.8, 2.5, 3.3V

High Speed

CL018LV
1P6M
1.5/3.3V

CL015LV
1P7M
1.2/3.3V

CL015HS
1P7M
1.2/3.3V

CL013LV
1P8M
1.0/2.5, 3.3V

CL013HS+
1P8M
1.2V/3.3V

CLN90HS
1P9M
1.0V/1.8, 2.5, 3.3V

Low Power

CL018LP
1P6M
1.8V/3.3V

CL015LP
1P7M
1.5V/3.3V

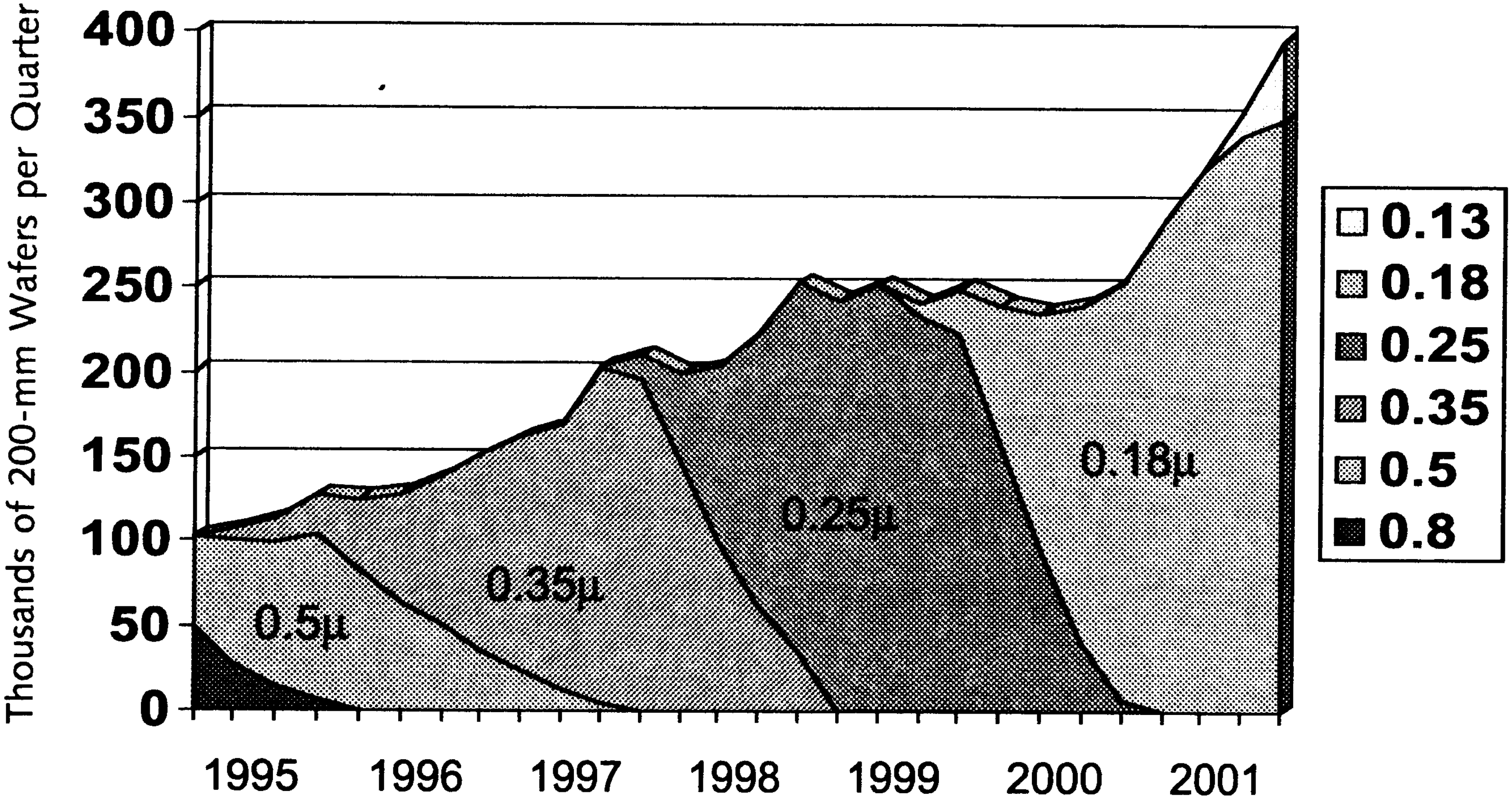
CL013LP
1P8M
1.5V/2.5, 3.3V

CLN90LP
1P9M
1.2V/1.8, 2.5V

Available Technologies **2002** **2003** **2004**

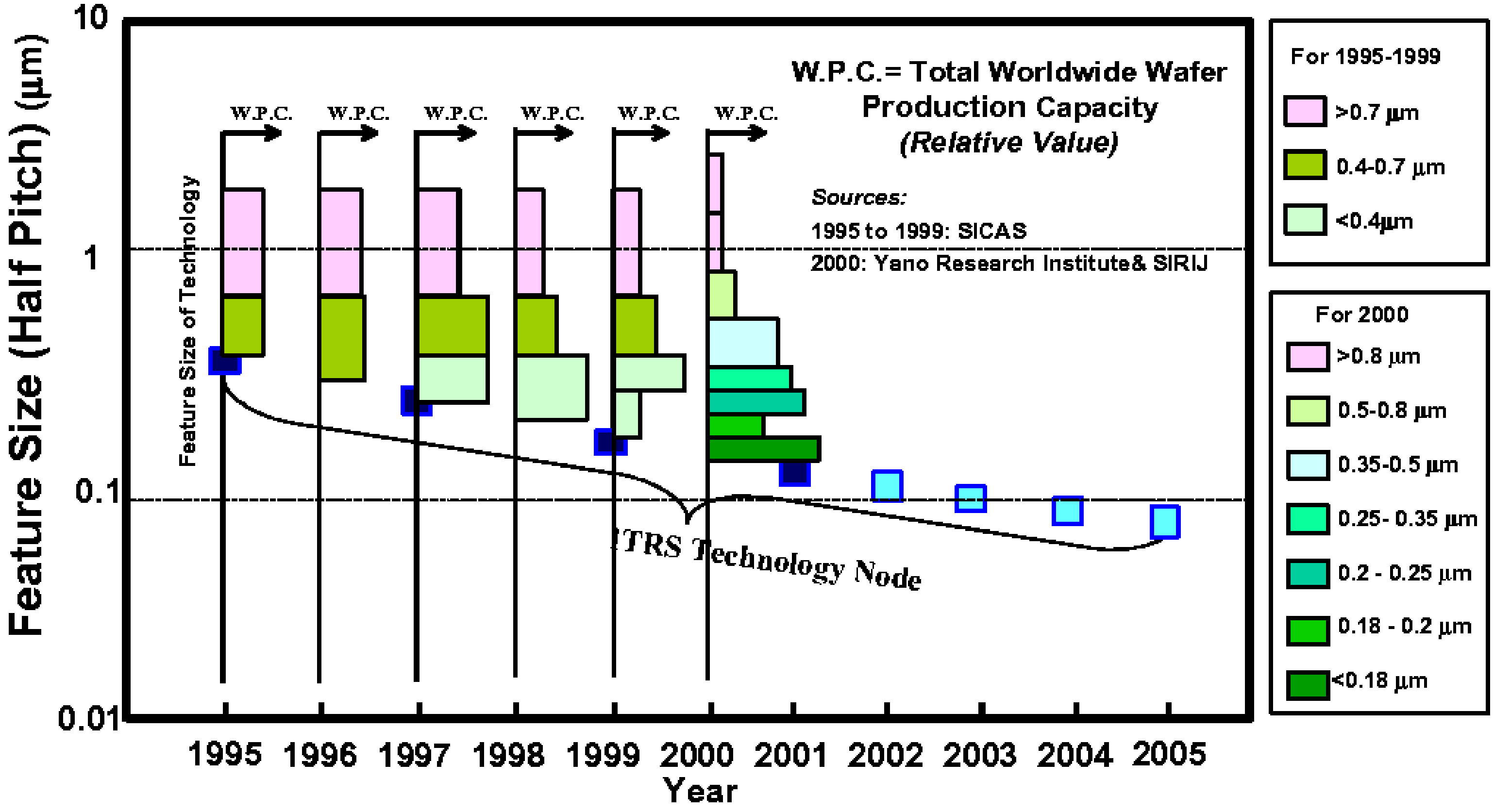
Left edge of each box represents risk production schedule

Technology & Intel wafer capacity(μP)



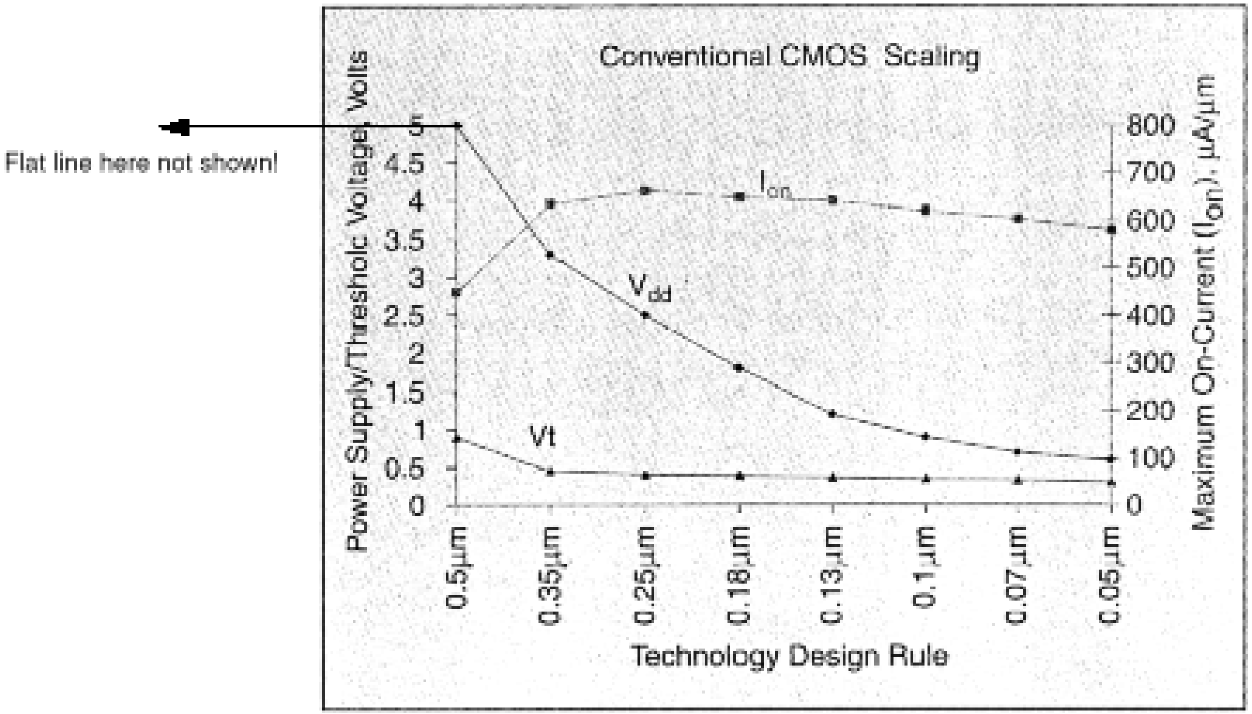
- **In uP's Useful years per technology is shrinking, but total volume same or growing!**

Technology & worldwide production



- When you’re not uP’s technologies stay around a lot longer

Technology trends: Vdd & Vt scaling



3. Power supply scaling and performance limits

- After 5V -> 3.3V the "Berlin wall" cracked & Vdd has been dropping
- Current is not increasing : speed comes from lowered capacitance

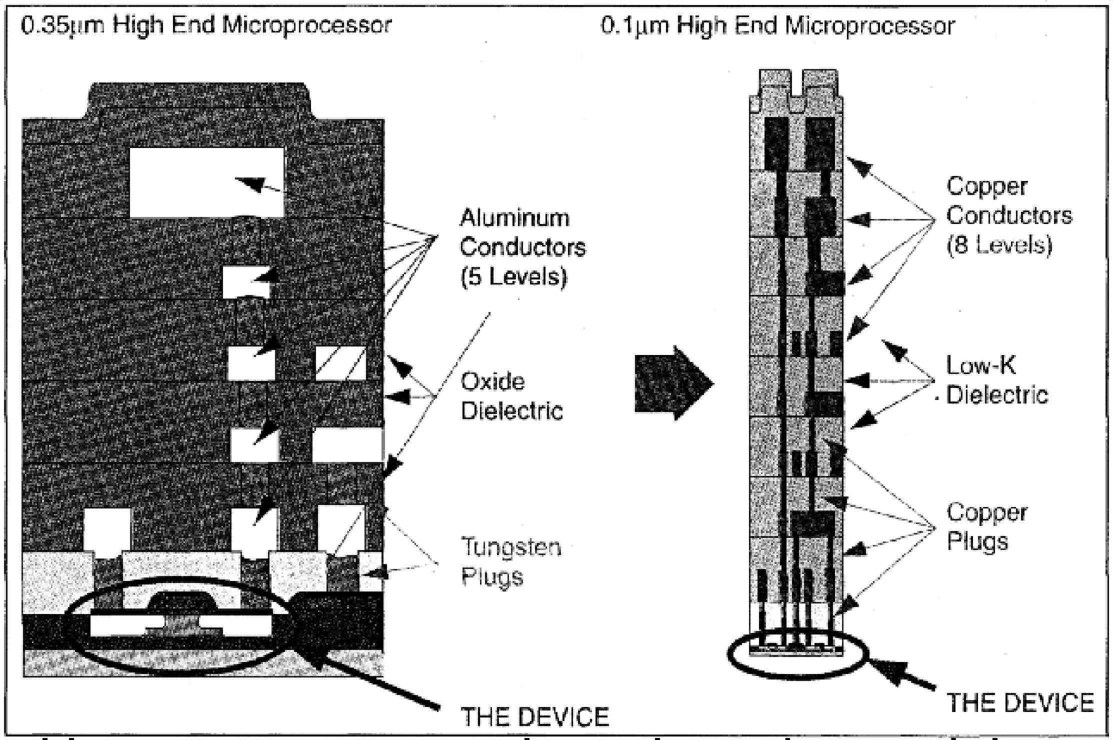
Technology trends: Vdd scaling & you

- Scaling not occurring on Vt at the same rate!
  - Device counts going up and leakage is too high to lower Vt => too much power!
  - Headroom a major issue for analog circuits -> stacked structures are tough
    - Migration of analog designs a serious headache
    - What was once “Vdd = 5 Vt’s” becomes “Vdd = 3Vt’s”
    - Budget your headroom carefully
  - Different Vt devices are coming… or already here
    - Low & High-Vt devices (separate implant = $)
    - Native device is ‘free’
    - BEWARE: Using any special device make your design less portable

Technology trends: multiple supplies

- Frequently multiple supplies on same die
  - Further reduce power or jitter (on-chip regulators)
  - Compatibility w/different devices (I/Os)
  - Further reduce leakage (DRAM)
- Be careful when crossing domains
  - Watch pass-gates & forward-biasing a diode
  - Timing issues, power consumption
  - Multiple oxides, multiple different device types

Technology trends: yes, wires are very important… and growing



- Metal layers are not equal: top layer is special
  - What layer is top today?
- Fringing much more important. $C_{fringe} > C_{area}$ below 0.25μ
- Your tools must be up to the job

Technology trends - conclusions

- Processes take a long time to develop & <u>make manufacturable</u>
  - You can make one of anything...

- Lower Vdd/Vt ratio makes analog more challenging

- Multiple supplies on-chip

- Multiple Vt's, multiple oxides

- Wires are more important than ever
  - Lots of layers, lots of fringe capacitances
  - Local vs. global clocking?
  - Tools

- Lots of room for circuit design!

MOSFET modeling : approaches

Two basic approaches over time:

- Physical
  - Parameters have physical meaning
  - Can be extracted from physical measurement (Tox, Ld, etc.)
  - Usually simple, few parameters (“one page’r”)
- Empirical
  - Use curve-fitting to match measured devices
  - Parameters hard to understand, and there are LOTS
  - Mostly mathematical approach

Reality is always a compromise

WARNING: Physical models can fit poorly
Empirical can break outside measured space

Modeling : The Big Problem

The biggest problem when it comes to MOS Modeling:

Circuit designers want a model that is 100% accurate, physically intuitive, very fast, preferably 6-months before the process is stable, and don’t want to pay for it.

Process designers want circuit designers to make their designs robust and tolerant to ‘minor variations’.

Fabs don’t get paid for having a better model…

…. but if your model is broken your circuit may be too!

MOSFET Modeling: brief history

- First generation
  - Hspice Level 1, 2, 3
  - “Physical” analytical models with geometry in model equations
  - Holding onto hand-calculation…

- Second generation
  - Hspice level 13, 28, 39: Bsim, “MetaMOS”, Bsim2
  - Shift in emphasis to circuit simulation with lots of mathematical conditioning
  - Quality of outcome is <u>highly</u> dependent on parameter extraction methodology
  - Good luck with hand-calculation
    - BUT served industry well for almost 10years!

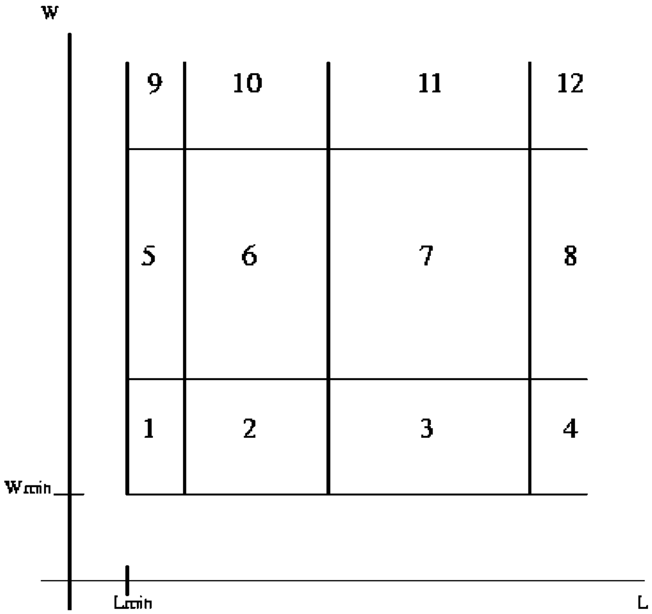
MOSFET Modeling : the present

- Third generation: Hspice level 49, 55: Bsim3v3, EKV

- Most new models are Bsim3v3
  - Bsim3 intent was return to simplicity... now >100 parameters!
  - Often start simple… and add complexity w/measured data
  - Binning still used to cover W&L space
  - Extensive mathematical conditioning
  - YOU will probably be using a Bsim3v3 model in your future

- EKV model developed by EPFL in Switzerland
  - Created for analog design
  - Excellent subthreshold behavior, mismatch, other benefits

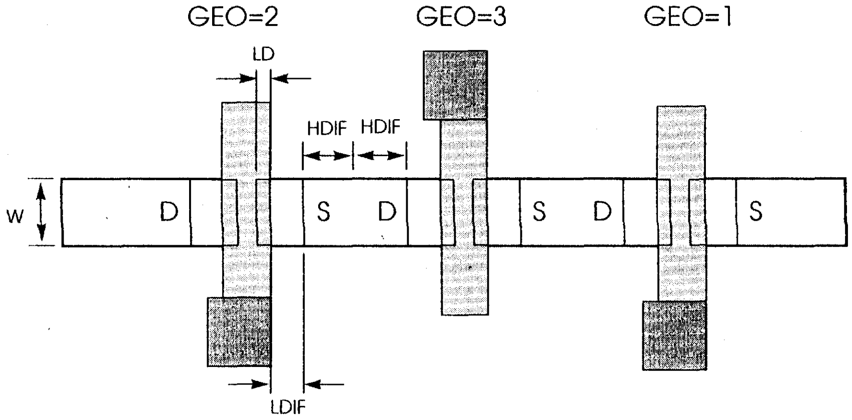
MOSFET Modeling : know your binning!



- Model binning often required for highest level of accuracy
  - Know your bin-space (remember process corners push you)
  - Beware of non-physical behavior at boundaries & beyond limits

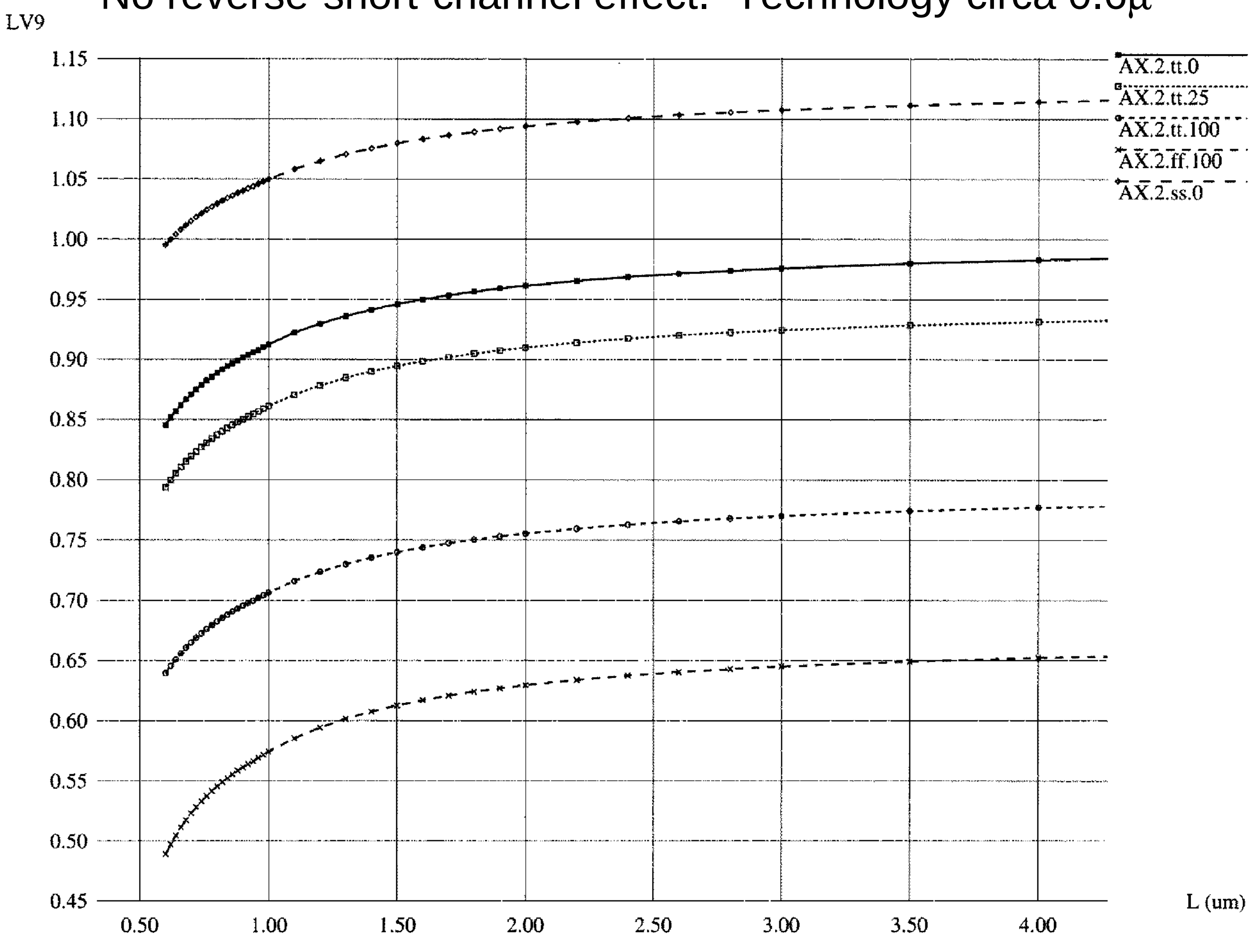
MOSFET modeling: checking the basics

- Source/drain diode capacitances are critical - don't get into a "gate cap only" mentality
  - What is the ACM method used?
    - Are all parameters (i.e. Cjgate) included in the model?
    - Do you know about GEO (HSPICE)?
  - Does your model jive with your extraction tool?
  - Does HDIF jive with your layout style?

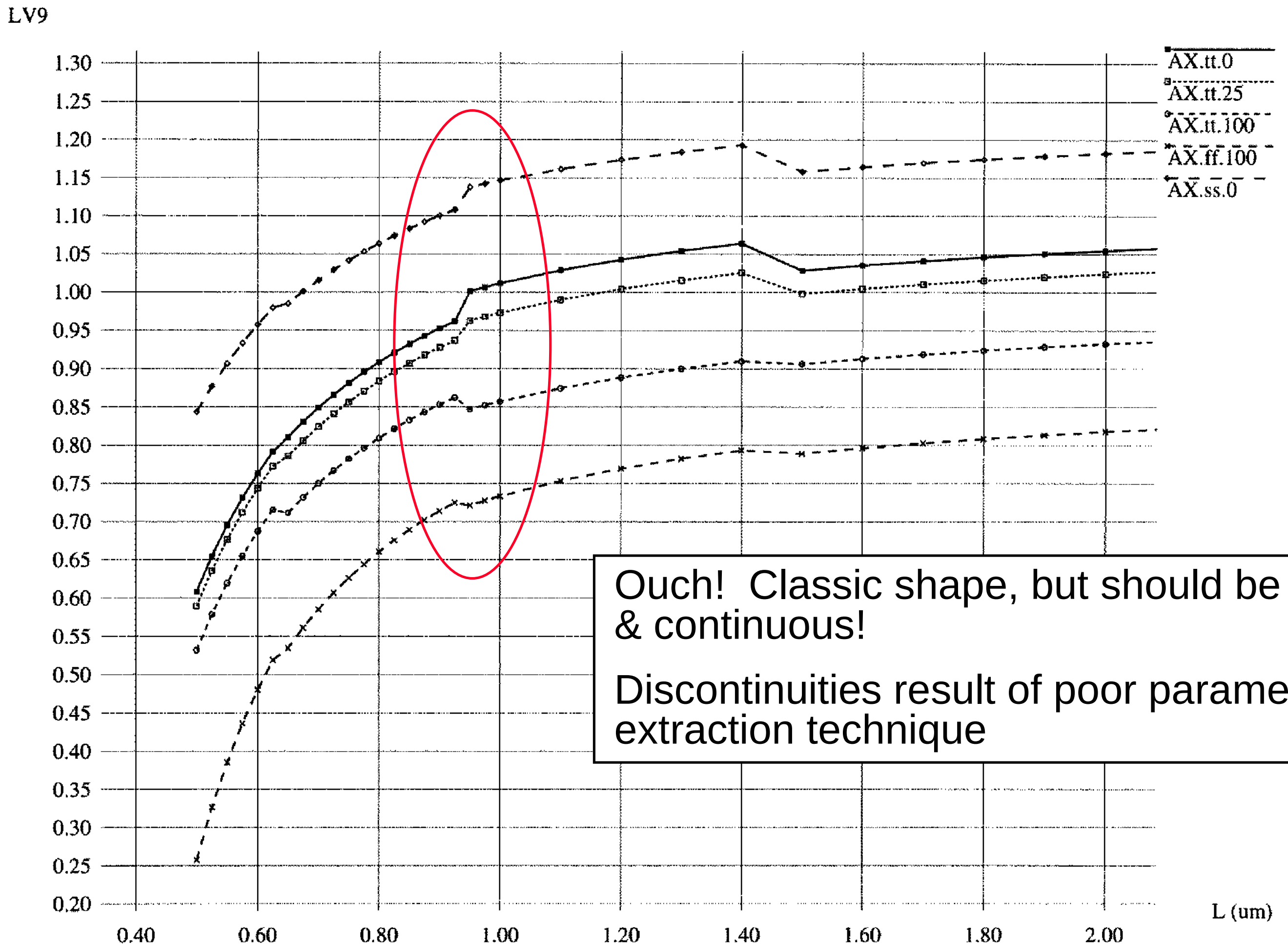


Modeling gotchas : Classic Vt vs. L

No reverse-short-channel effect. Technology circa 0.6µ



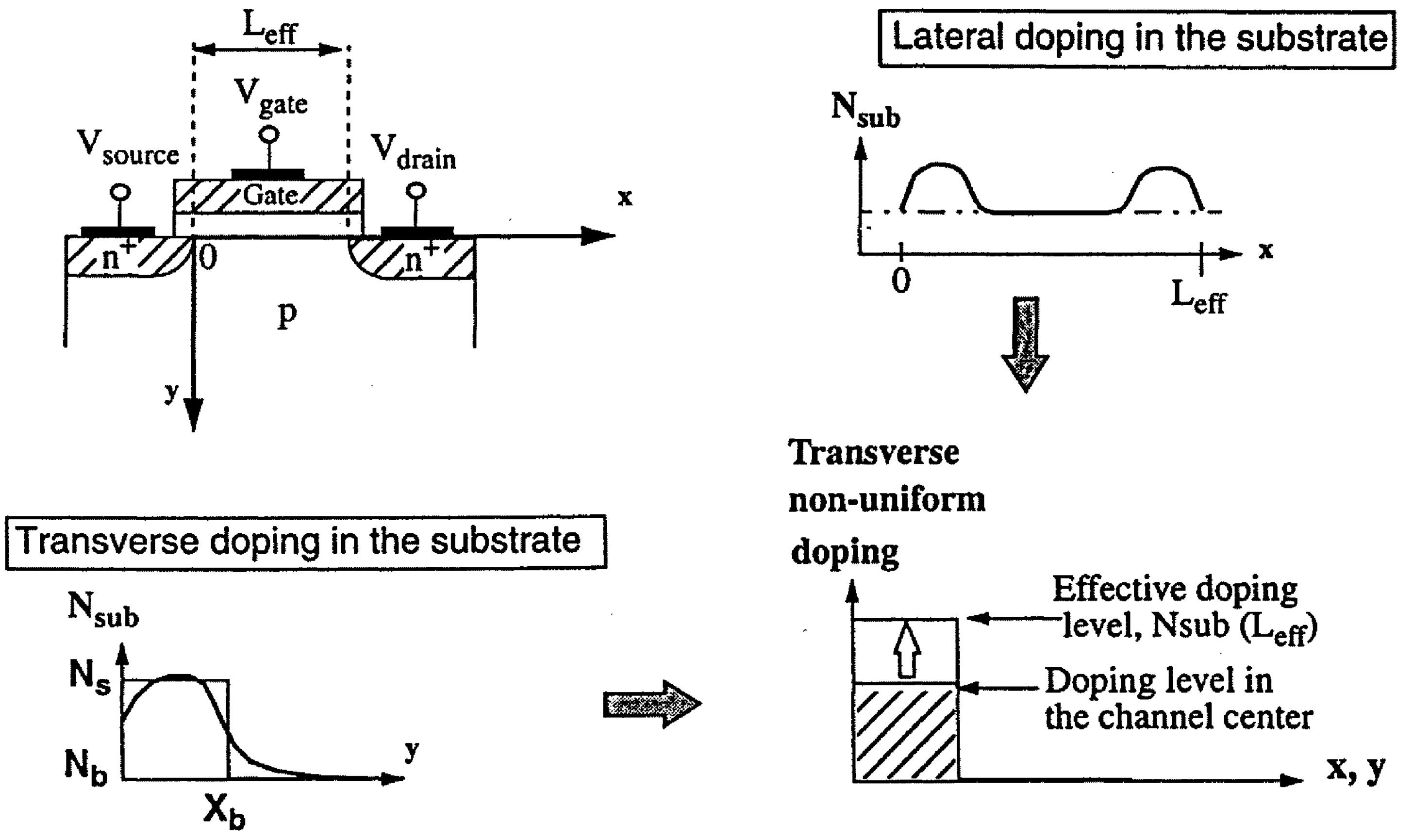
Vt vs. L : discontinuities at model boundaries



Ouch! Classic shape, but should be smooth & continuous!

Discontinuities result of poor parameter extraction technique

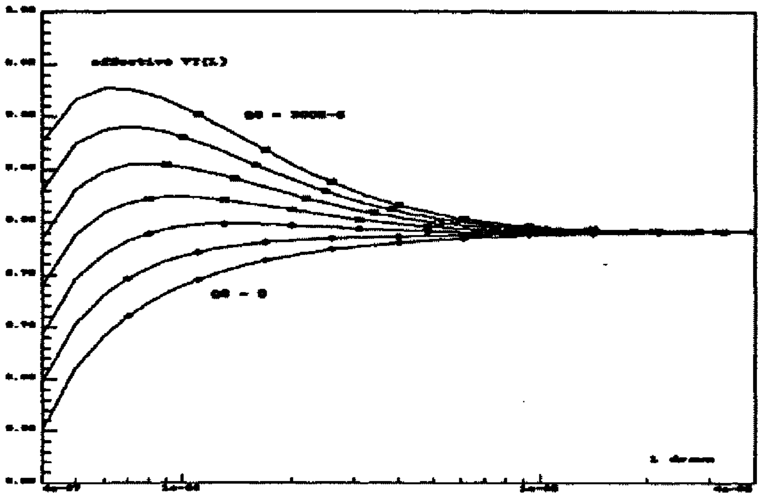
Reverse short channel effect (RSCE)



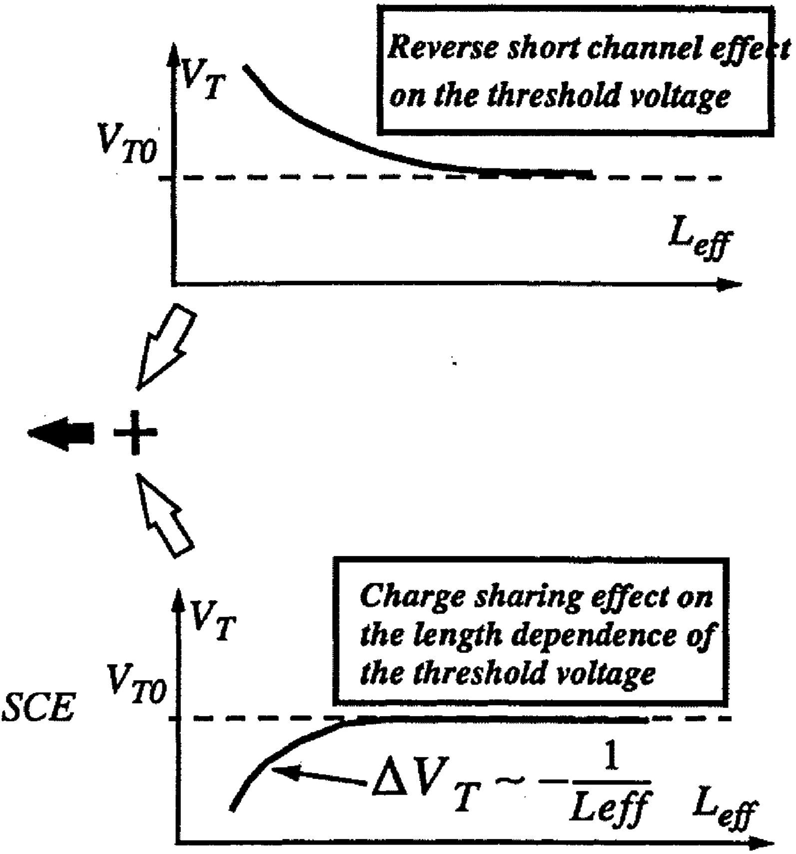
Impurities effect lattice during high-temp process steps

RSCE con't

Really a combination of two effects

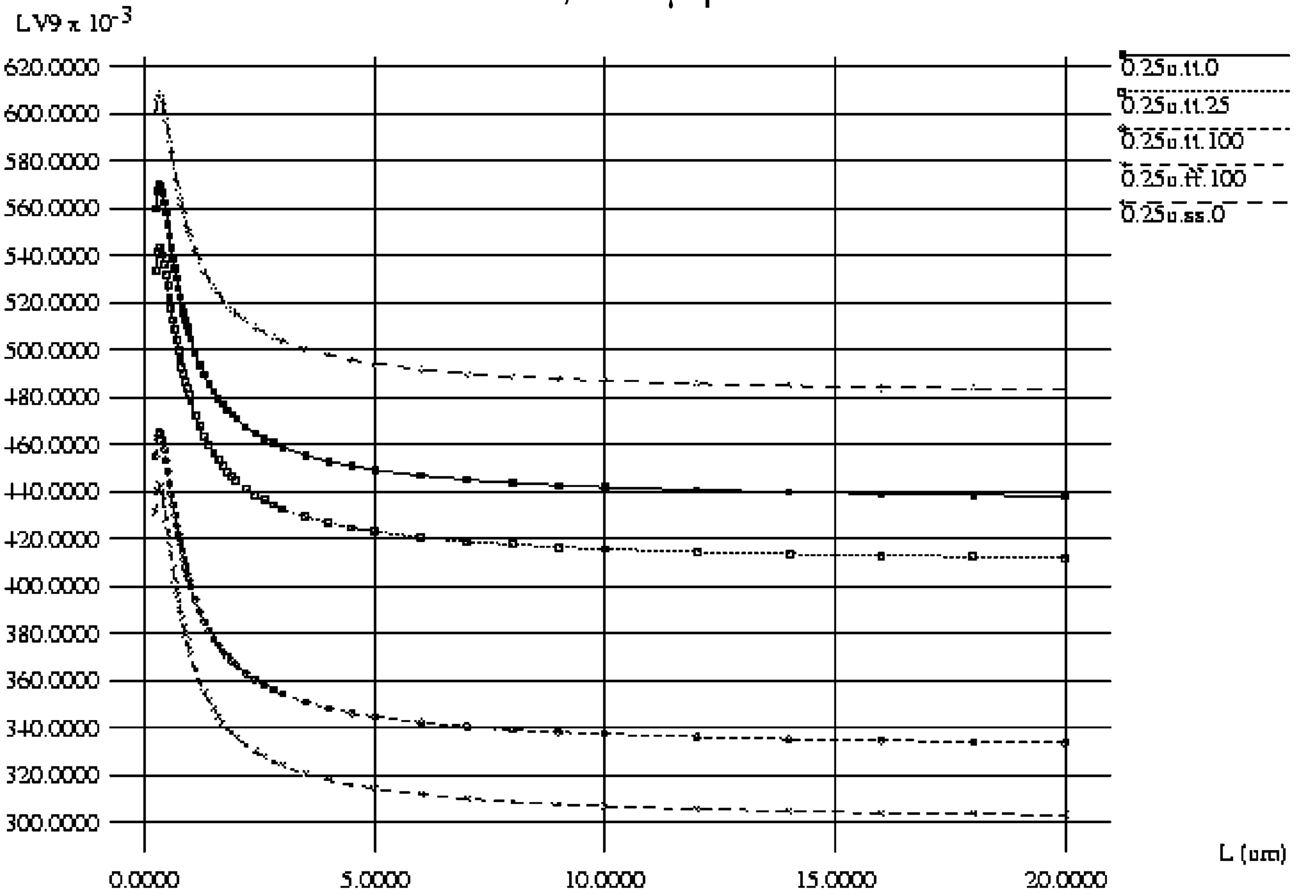


Variation of the threshold voltage due to the RSCE and charge-sharing effects with Leff



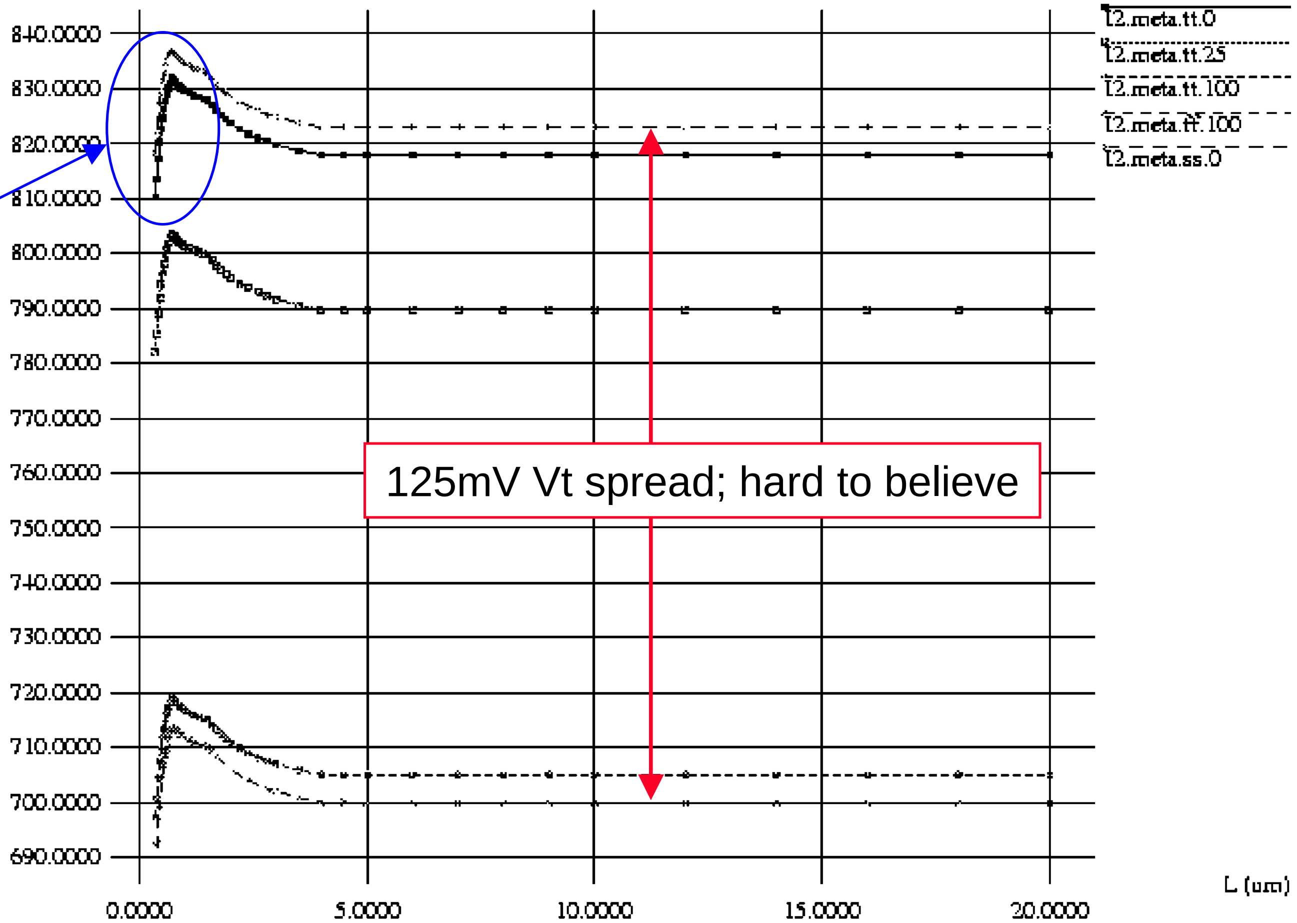
Modern Vt vs. L with RSCE

Circa 2.5V, 0.25μ process



Vt spread : process & temp

Check Vt spread between ff/100C & ss/0C

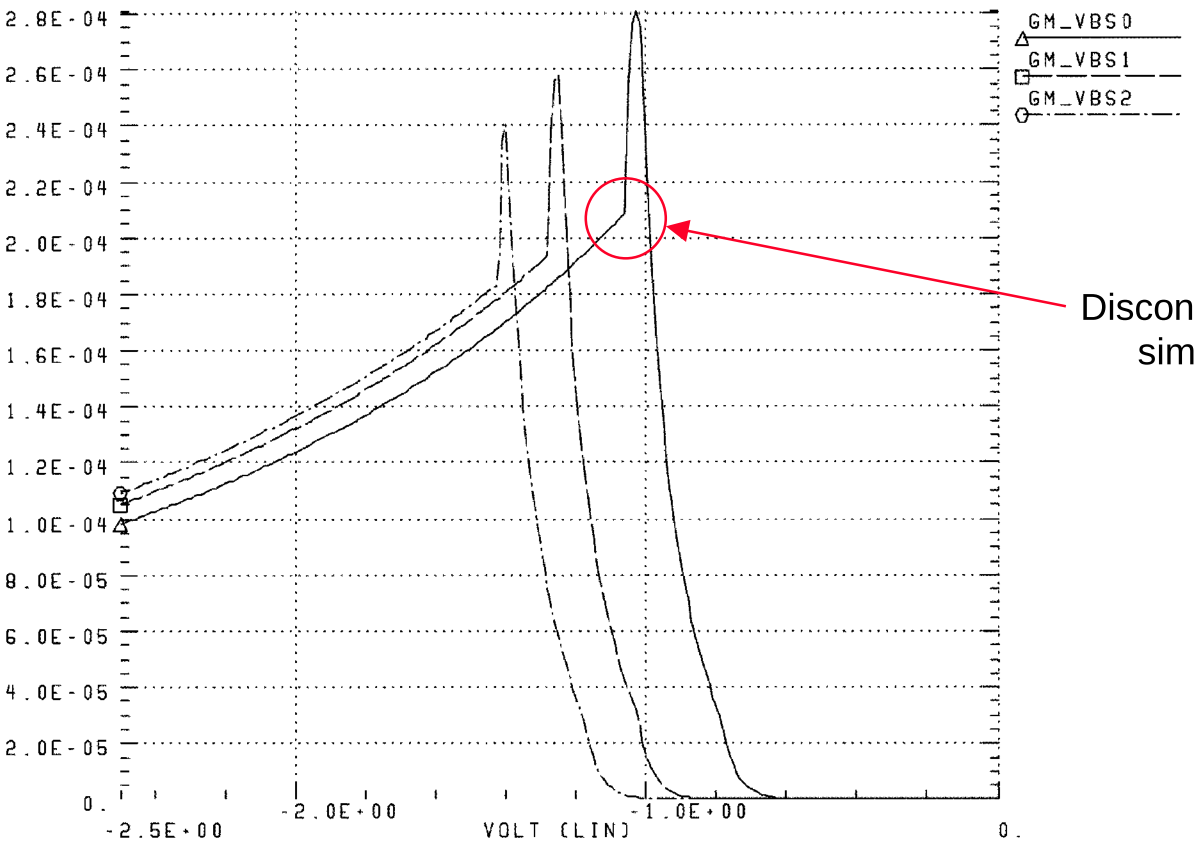


believable

125mV Vt spread; hard to believe

Modeling gotchas: g_M vs. Vgs

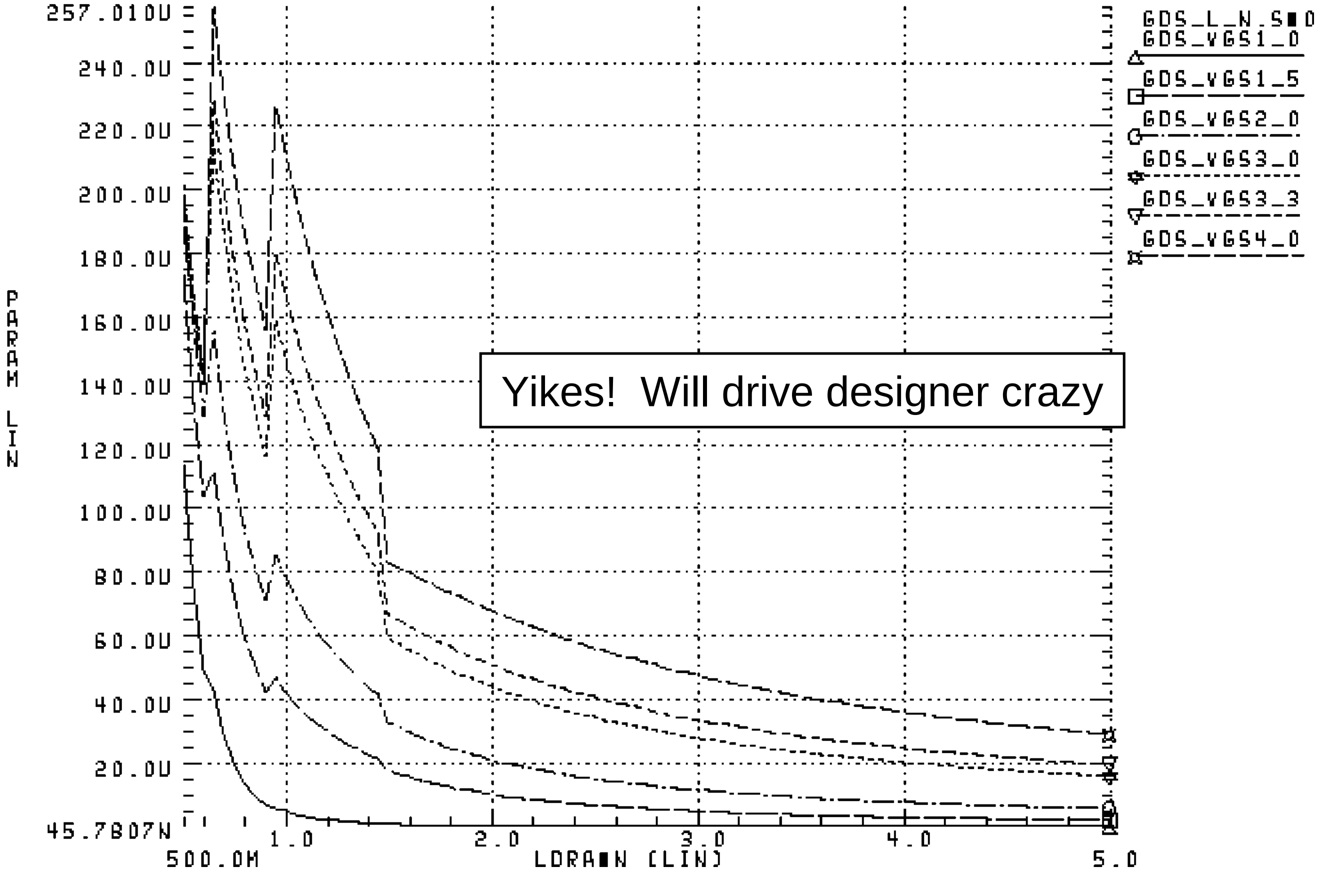
All first-derivatives should be smooth & continuous



Discontinuity will drive simulator crazy

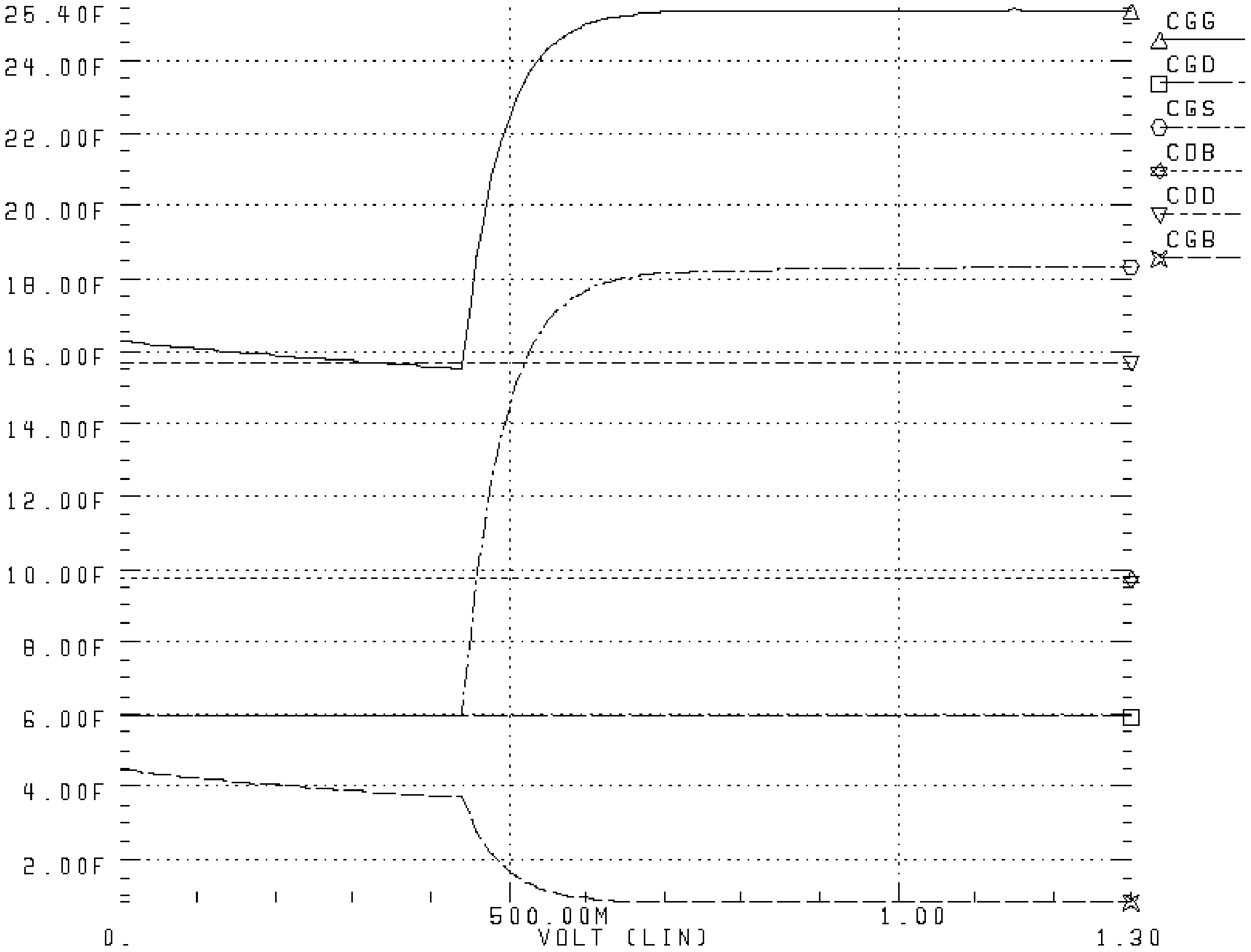
Modeling gotchas: g_{DS} vs. L

Should also be smooth and continuous

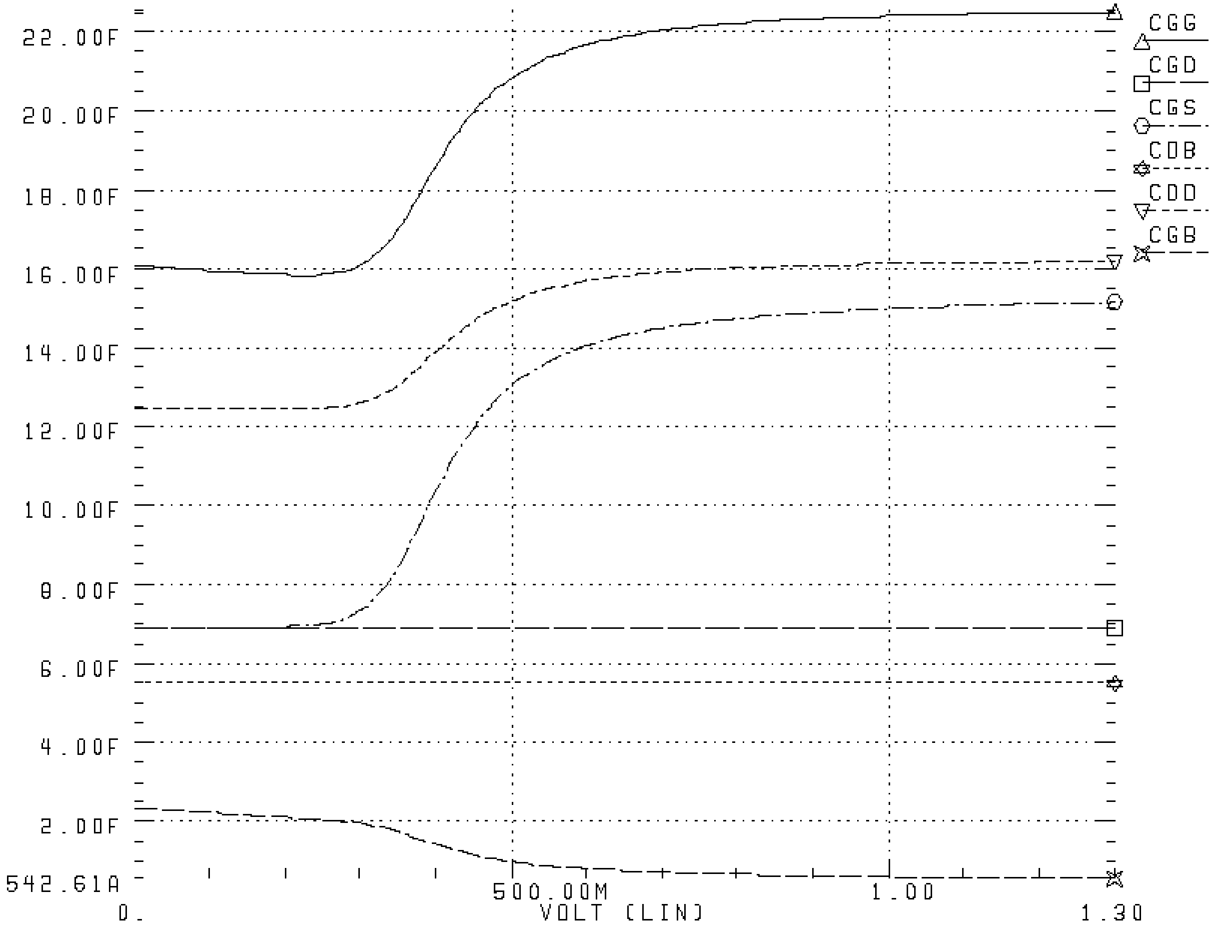


Yikes! Will drive designer crazy

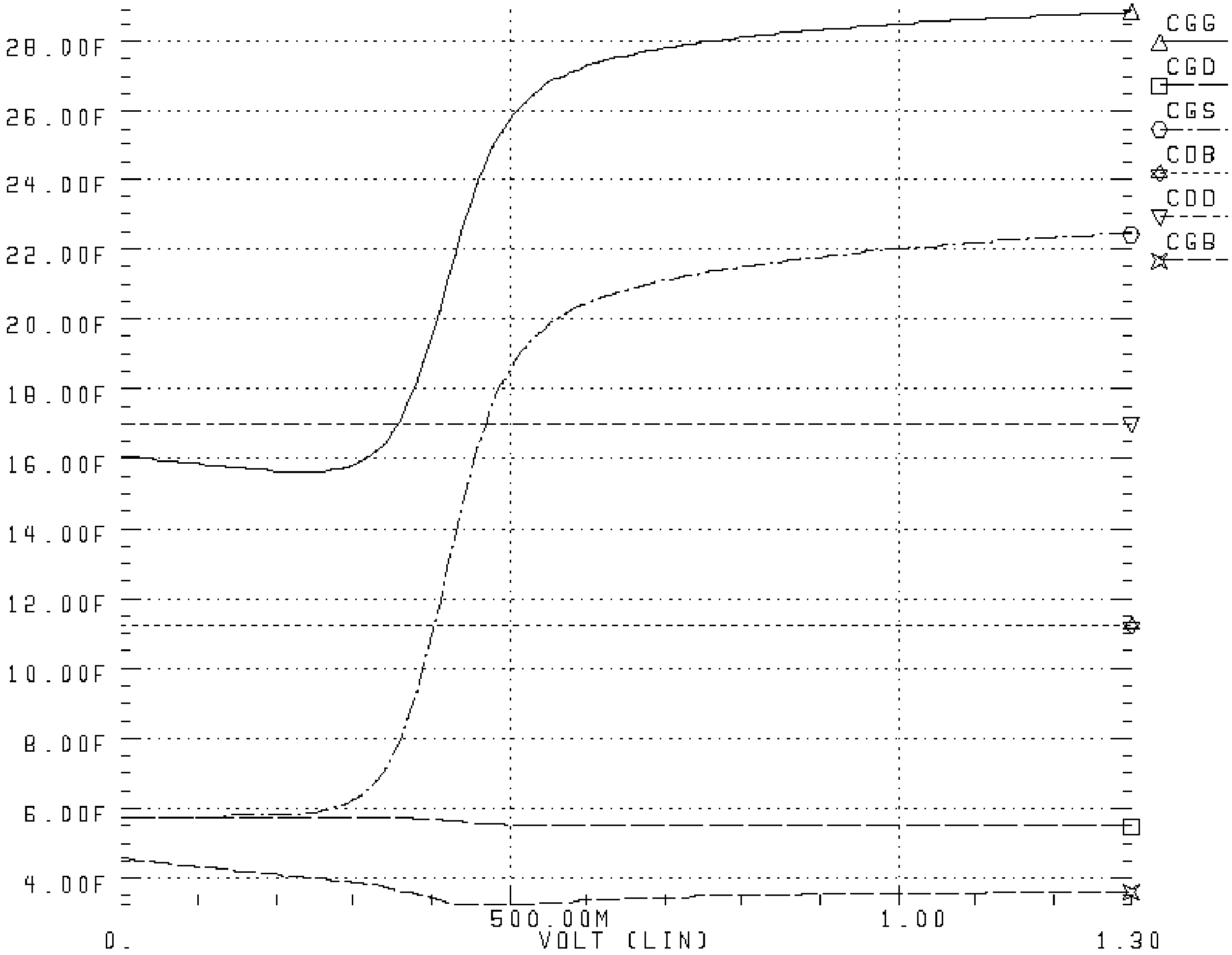
Modeling gotchas: Cgg vs. Vgs - first bsim3



Modeling gotchas: Cgg vs. Vgs - first EKV



Modeling gotchas: Cgg vs. Vgs - bsim3 at +1yr



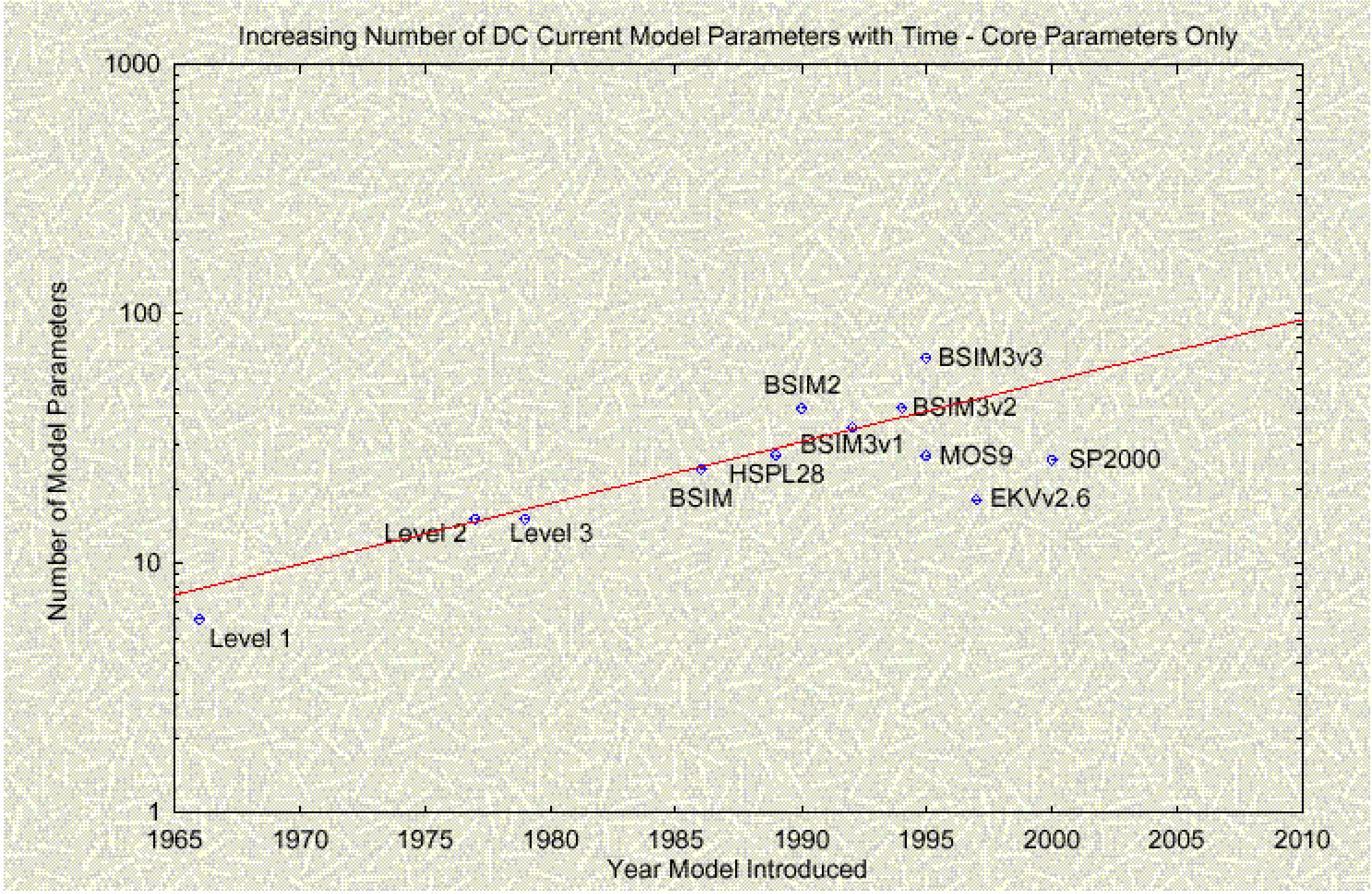
EKV model : Introduction

- EKV model developed by EPFL in 90's
  - New approach with emphasis on low-Voltage design
  - Bulk-referenced; VERY different way of thinking
  - So far has stayed mostly physical (~20 parameters, no binning)
  - Has Pelgrom-style mismatch parameters built-in (no netlist hacking)
  - Simulation speed can be ~3x Bsim3v3 (if Bsim has discontinuities)

- Availability
  - v2.6 available in Hspice 2001.4, looks good down to 0.18μ
  - v3.0 coming mid '01 - better short channel effects, poly depletion model

- Future will depend on acceptance - but has a dedicated team

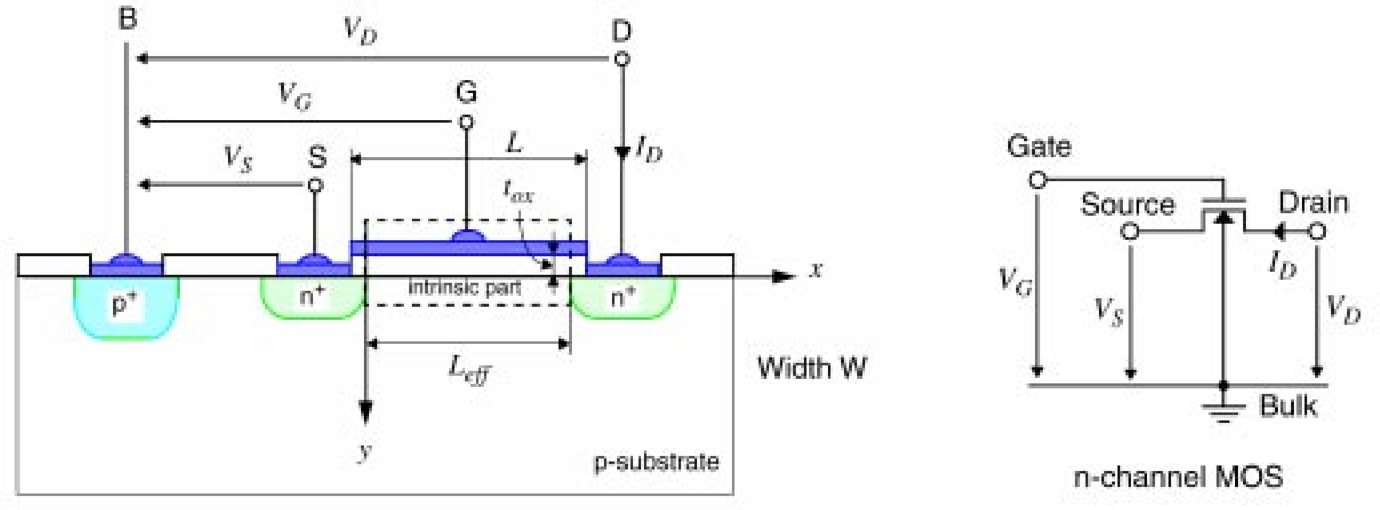
EKV Model : Fewer parameters, physically based



Courtesy D. Foty

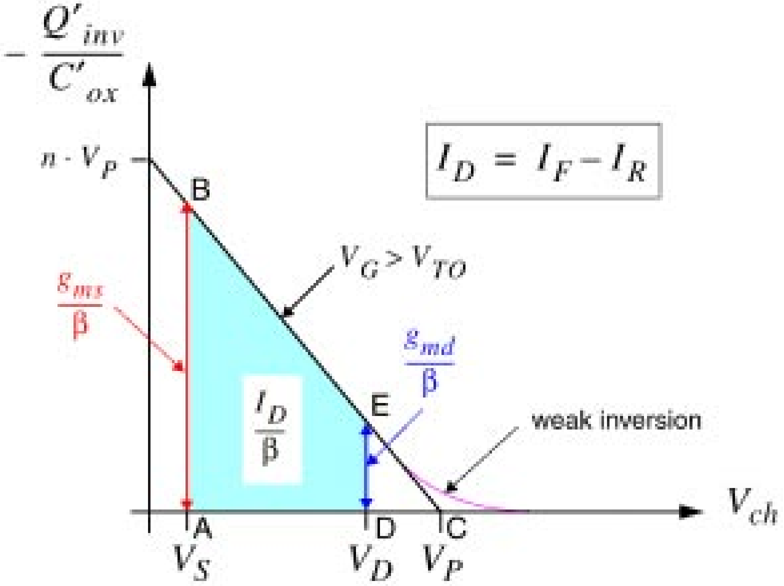
EKV model : fundamentals

- All voltages referenced to local substrate, not source
  - Takes into account natural symmetry of device



EKV model : V_P, I_F, I_R

$$I_D = \underbrace{\beta\cdot\int_{V_S}^{\infty}\left[\frac{-Q'_{inv}(V_{ch})}{C'_{ox}}\right]\cdot dV_{ch}}_{\substack{=\ \text{forward current}\, I_F \\ \text{controlled by}(V_P - V_S)}} - \underbrace{\beta\cdot\int_{V_D}^{\infty}\left[\frac{-Q'_{inv}(V_{ch})}{C'_{ox}}\right]\cdot dV_{ch}}_{\substack{=\ \text{reverse current}\, I_R \\ \text{controlled by}(V_P - V_D)}}$$



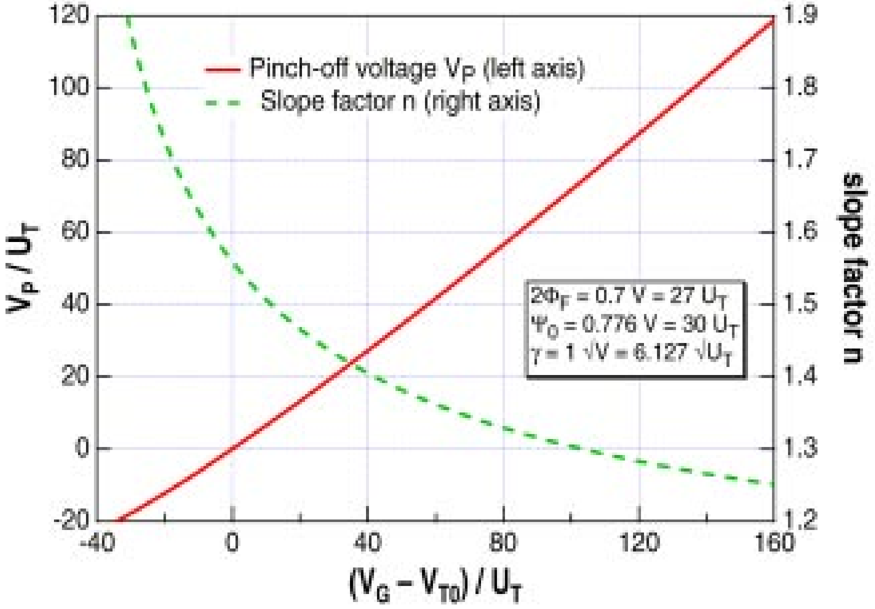
EKV model : Gate sets the pinch-off voltage

V_P represents the voltage that should be applied to the channel to cancel the effect of the gate voltage (Vg > Vt)

- It is where the inversion charge becomes zero

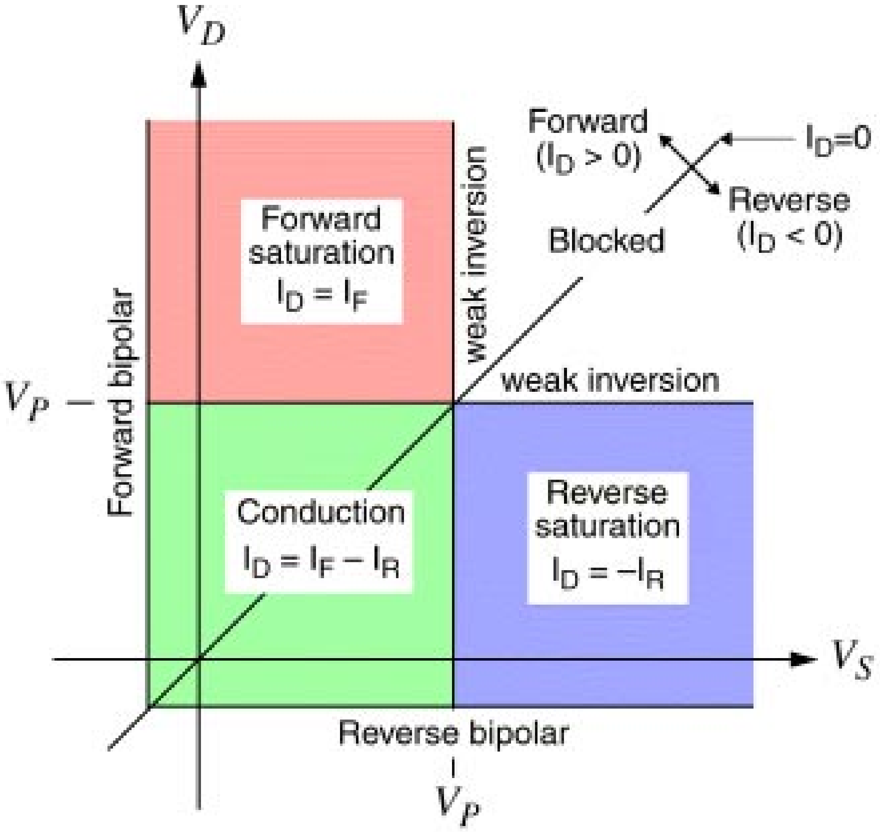
$$V_P = V_G - V_{T0} - \gamma \cdot \left[\sqrt{V_G - V_{T0} + \left(\sqrt{\Psi_0} + \frac{\gamma}{2} \right)^2} - \left(\sqrt{\Psi_0} + \frac{\gamma}{2} \right) \right]$$

$$V_P \cong \frac{V_G - V_{T0}}{n}$$

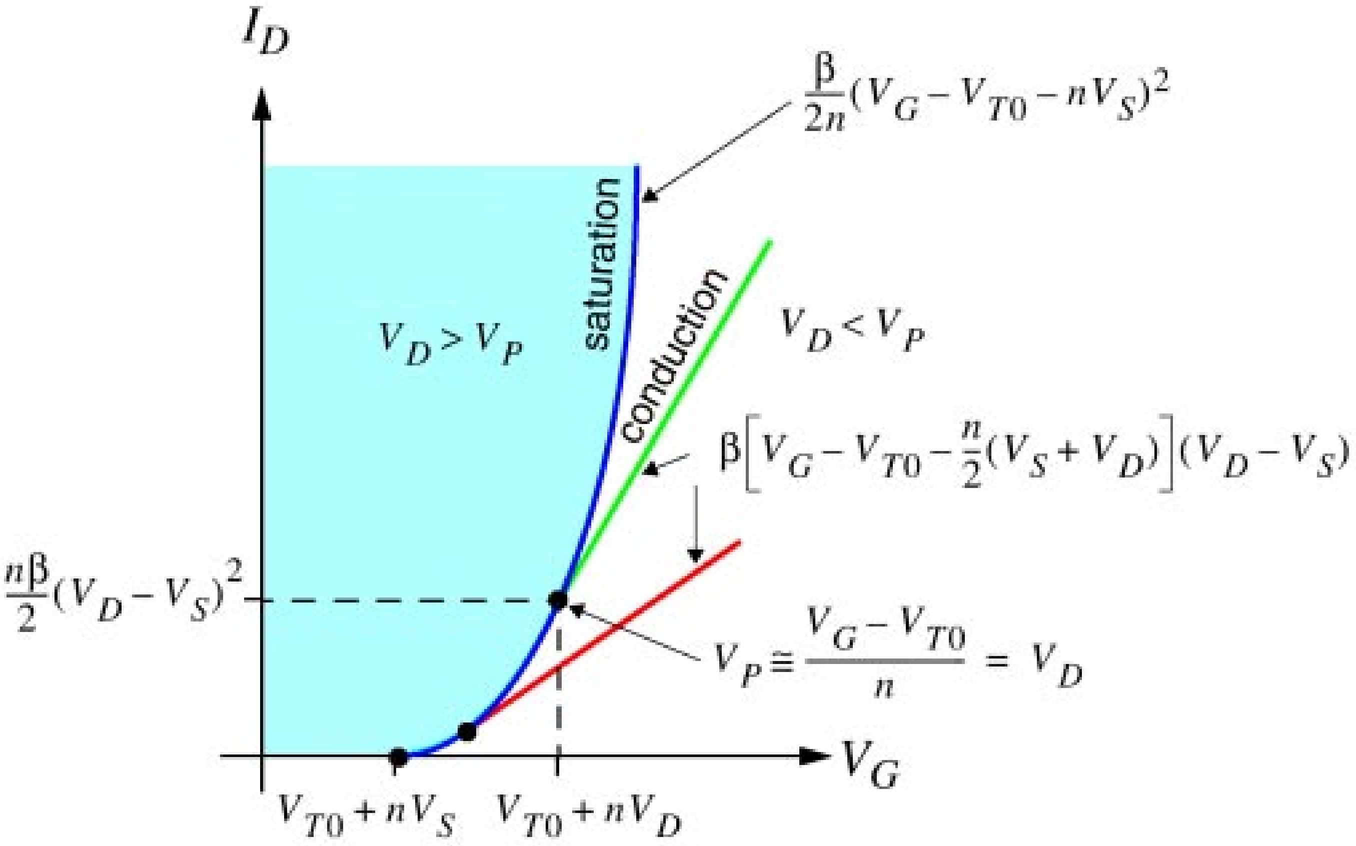


EKV model : Modes of operation

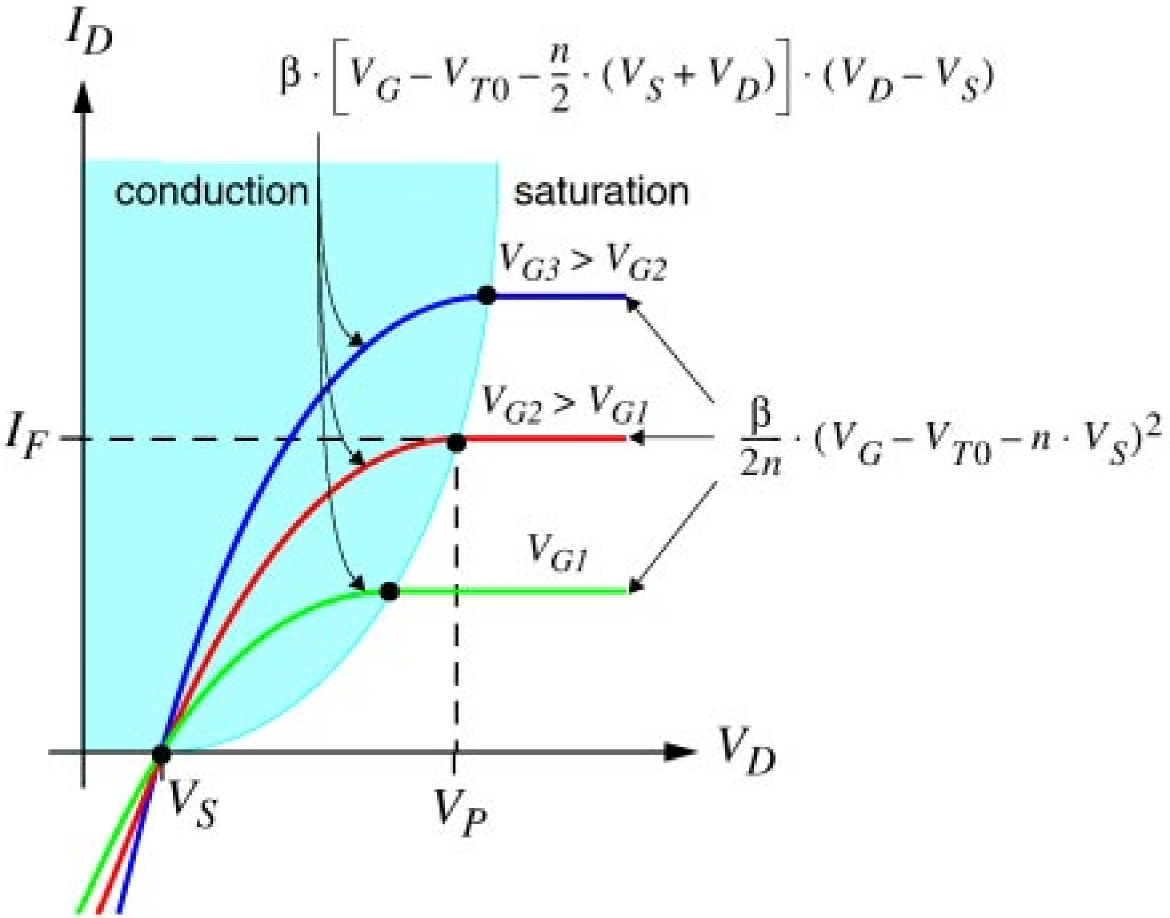
Defined by drain and source voltages w.r.t. V_P



EKV model : Id-Vg characteristics



EKV model : Id-Vd characteristics



MOSFET Modeling : Conclusions

- Big problem of modeling
  - It's in nobody's interest to make sure you have a good model and…
  - There are still disparities between fab & circuit folk
    - What you need as a circuit designer may different than digital
    - This may be uncharacterized
    - Sometimes what you want may be unrealistic!
      "Why is your circuit so sensitive…"

- Result: caveat emptor
  - Examine your models
  - Request reasonable behavior & make your circuits tolerant

Circuit design advice

- Be aware
  - Spice models are your tools : know your tools
  - You will be asked to “port” your design : think ahead

- Design clean
  - Your spice decks are software - be a good programmer
  - Device W/L’s : treat them almost as different devices
  - Do it right or do it over
    - Tapeout early, tapeout often is
      not the best method - you will get smoked

References

ITRS (International technology roadmap for semiconductors) website:

http://public.itrs.net/

MEAD Microelectronics (short courses) website:

http://www.mead.ch and http://mead.netgate.net

EKV website:

http://legwww.epfl.ch/ekv/

Dan Foty’s website:

(author MOSFET Modeling with SPICE principles and practice)

http://www.sover.net/~dfoty

FSA (Fabless semiconductor association) website:

http://www.fsa.org/

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