Lecture 8

Clock Distribution Techniques

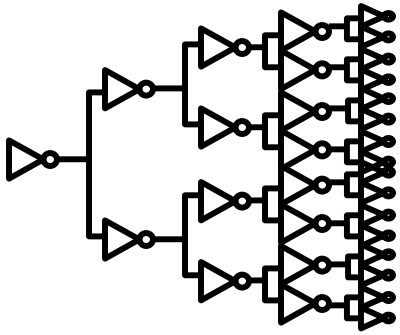
Intel Corporation
jstinson@stanford.edu

Clock Distribution Metrics

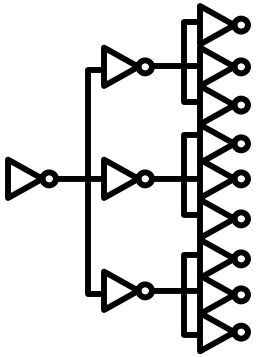
- Skew
  - Minimize “unintentional” skew between different clock taps
- Jitter
  - Minimize dynamic variation in clock arrival times
- Power
  - Minimize power consumption in the distribution network
- Duty Cycle
  - Preserve duty cycle at all clock taps

Clock Distribution Techniques

- Matching gates and wires (skew)
  - Keep transistors oriented in same direction
  - Keep transistor "environment" identical
  - Keep wire length/width/spacing identical
  - Use fully shielded wires
- Minimize clock distribution depth (skew, jitter)
  - More buffers means more chance for mismatch (P, V, or T)
  - Needs to be balanced with enough buffering to drive final load



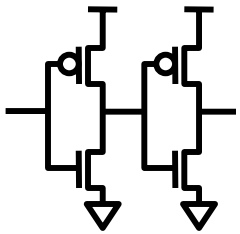
Hi Gain, Sharp Slopes



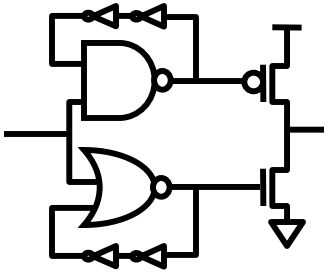
Lower Gain, but better skew?

Clock Distribution Techniques (cont'd)

- High gain buffering (skew, jitter, power)
  - Use push-pull structures vs. standard CMOS



Standard CMOS



Hi-gain CMOS

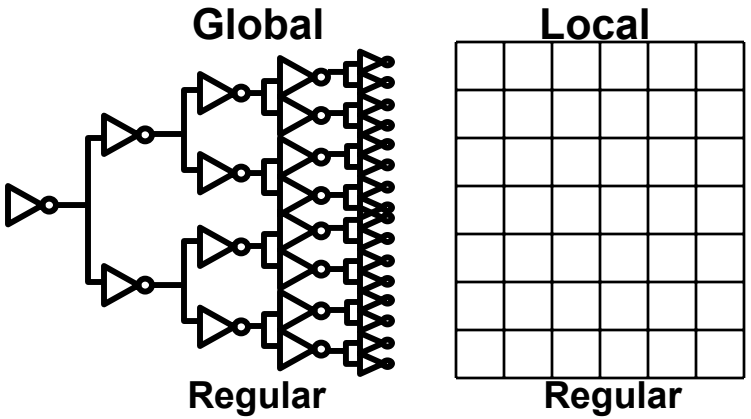
- Differential signalling (duty cycle, skew, jitter)
  - Uses more routing resources (i.e., power and area)
  - Sense amp detects "cross-over" point of differential
    - P/N ratio duty cycle issues reduced
    - Full swing signal issues reduced
  - Possible to design sense amp to provide higher gain stages

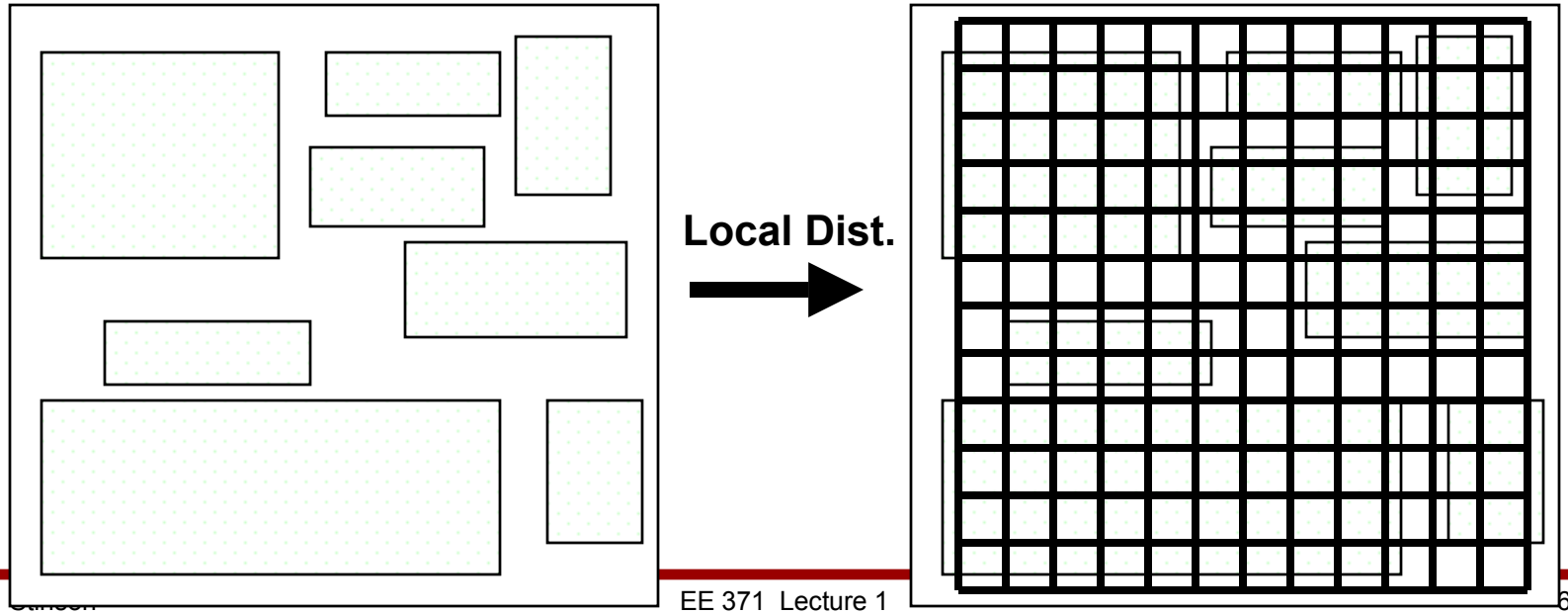
Clock Distribution Techniques (cont'd)

- Low swing signalling (power)
  - Use lower supply voltage for clock distribution
    - Could come from explicit power supply or locally generated
  - Need to transition from full swing PLL to low swing distribution
  - Need to transition from low swing distribution to full swing flops
  - Usually done in the higher level portion of distribution
    - Relatively small portion of overall clock power

Clock Distribution Examples

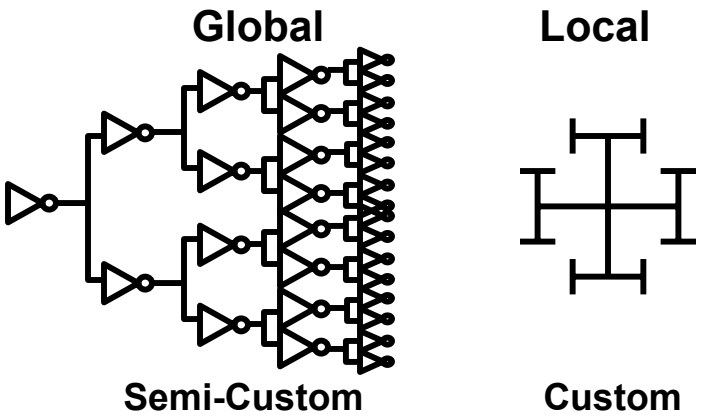
- Grid
  - “Best” skew
  - “Easy” design
  - Uses a LOT of wiring resources
    - Power and area implications

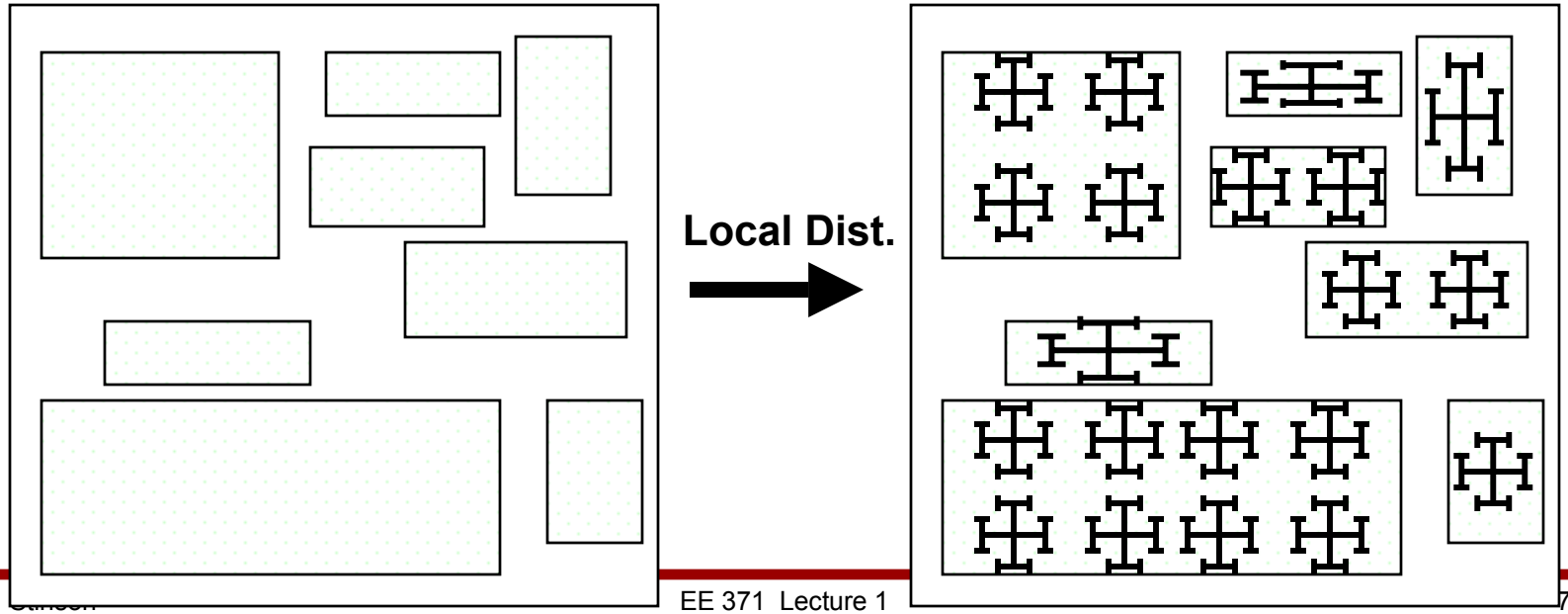




Clock Distribution Examples

- H-Tree (binary)
  - Difficult to get low skew
  - “Complex” design
  - Least number of wiring resources





Clock Distribution Examples

- Spine
  - Combines grid and binary tree
  - Put global distribution into spine
    - Makes it more regular
  - Local distribution is still custom