
VLSI Power Delivery For Core, I/O, and Analog Supplies

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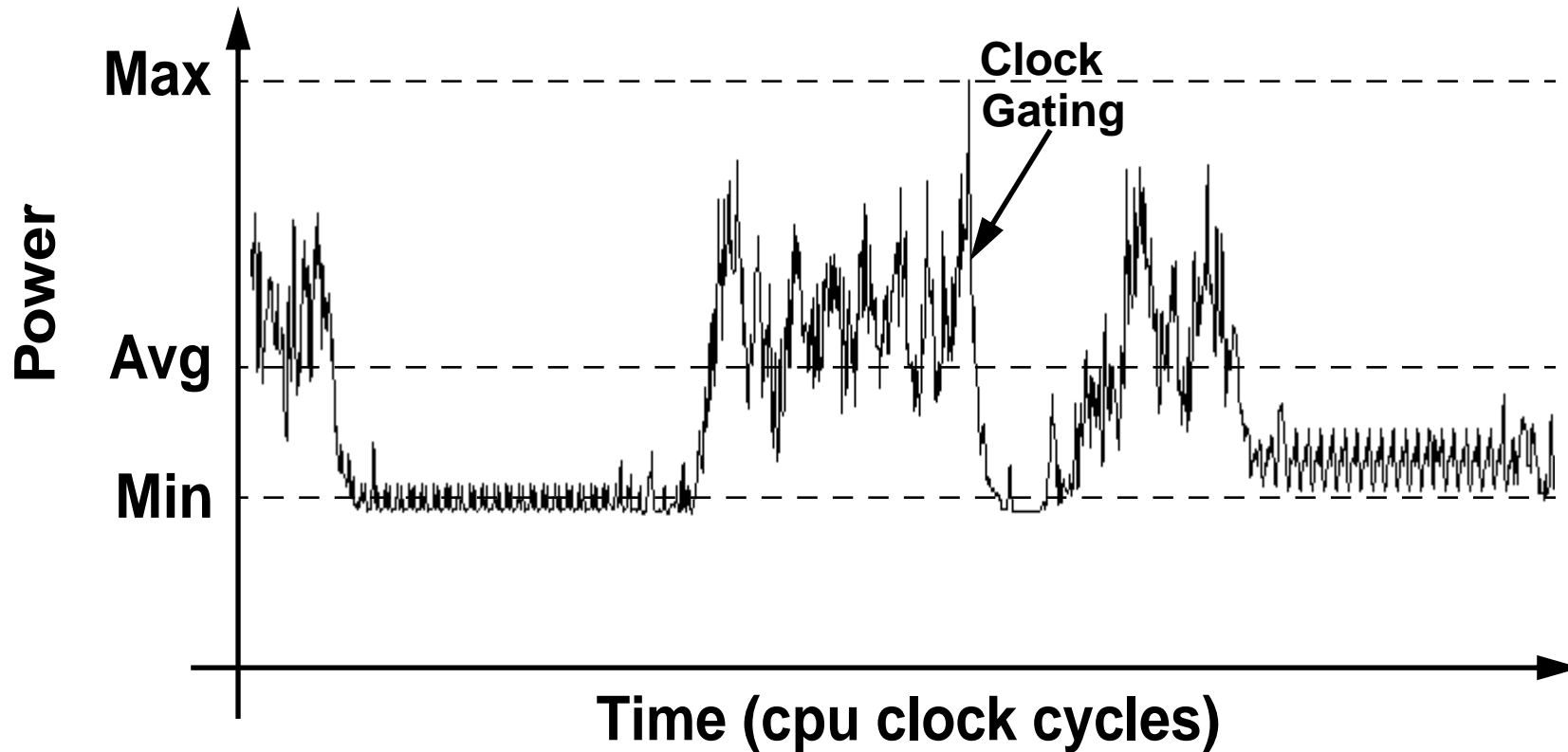
Major Electrical Interfaces

- Core Power Delivery
 - Physical and electrical view
 - Parasitic inductance estimation
 - Distribution issues, guidelines
- I/O Power Delivery and Signaling
 - Signal return current
- Analog Power Delivery
- Summary

Microprocessor Design Constraints

- Power supply impedance
 - $Z = (\Delta V_{\text{SPEC}}) / (\Delta I_{\text{ESTIMATE}})$: Ex. $1.8\text{-V} \times 5\% / 10\text{-A} = 9\text{-m}\Omega$
 - Must deliver power over a broad frequency spectrum

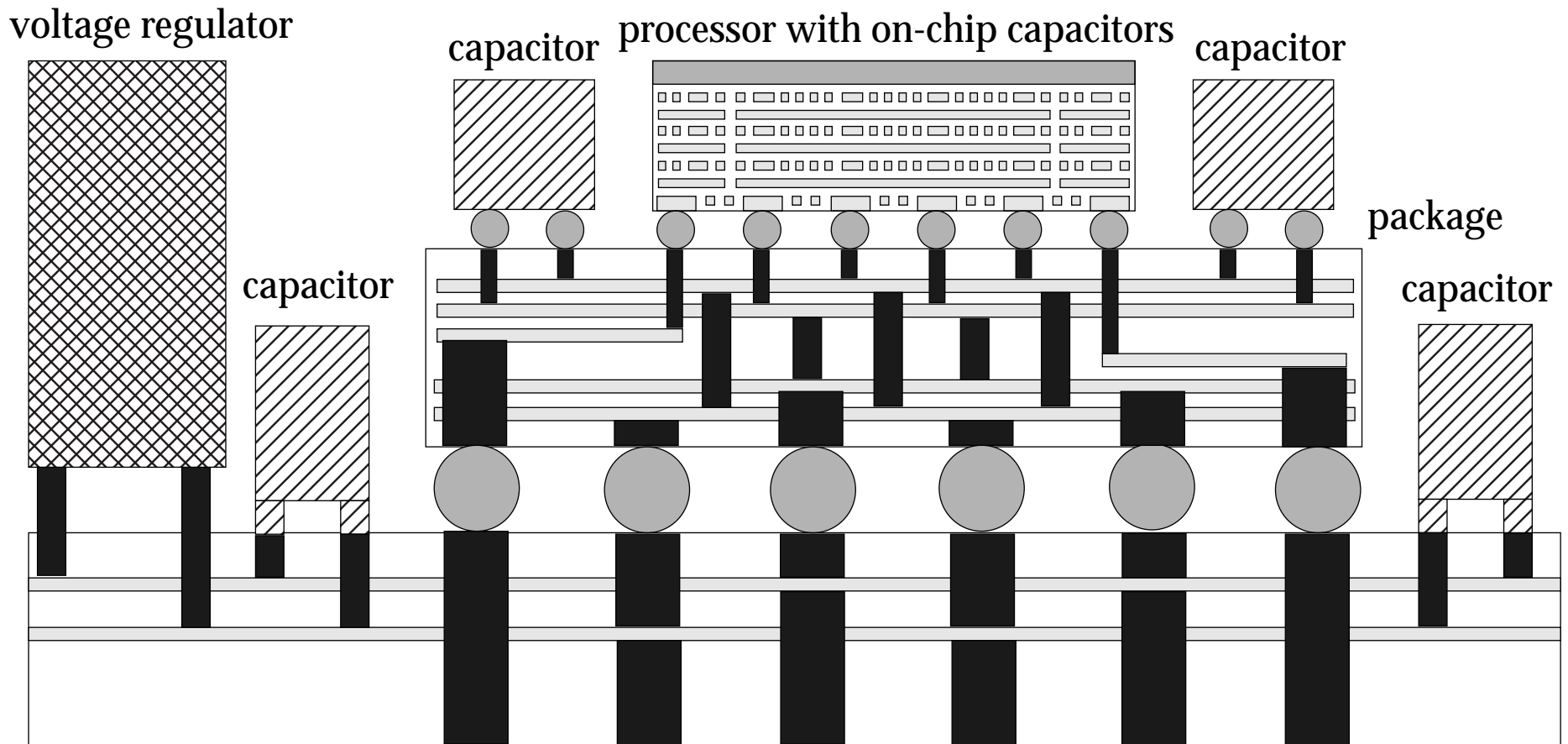
Architectural Power Model To Estimate ΔI



Microprocessor System

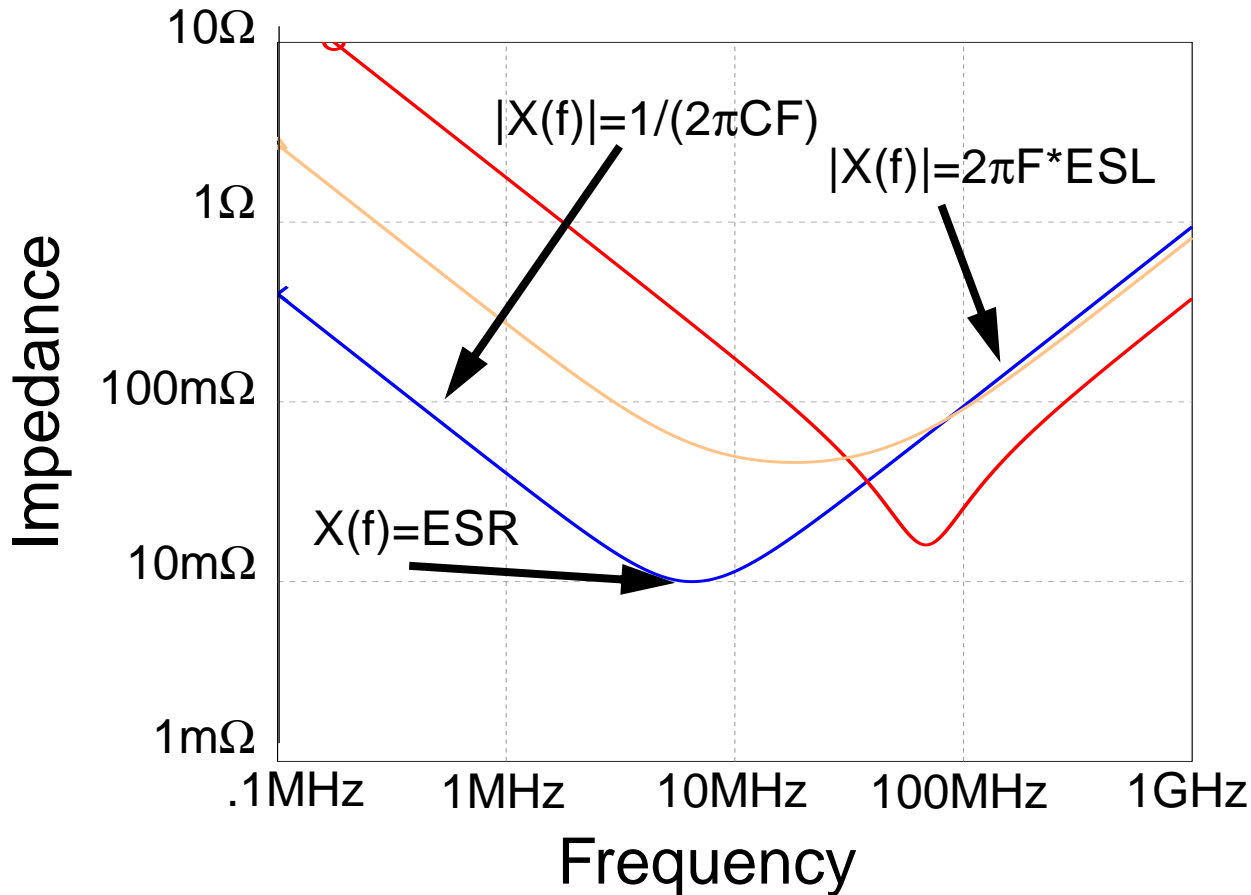
■ Power perspective

- Package types, attach strategy, board or MCM type, package/board layer assignments, decoupling capacitor requirements.

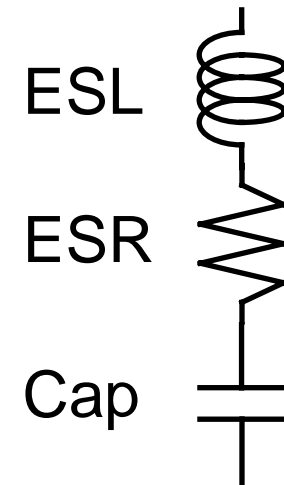


Decoupling Capacitor Modeling

- Wide range in performance and cost
 - Example: 3 different capacitors

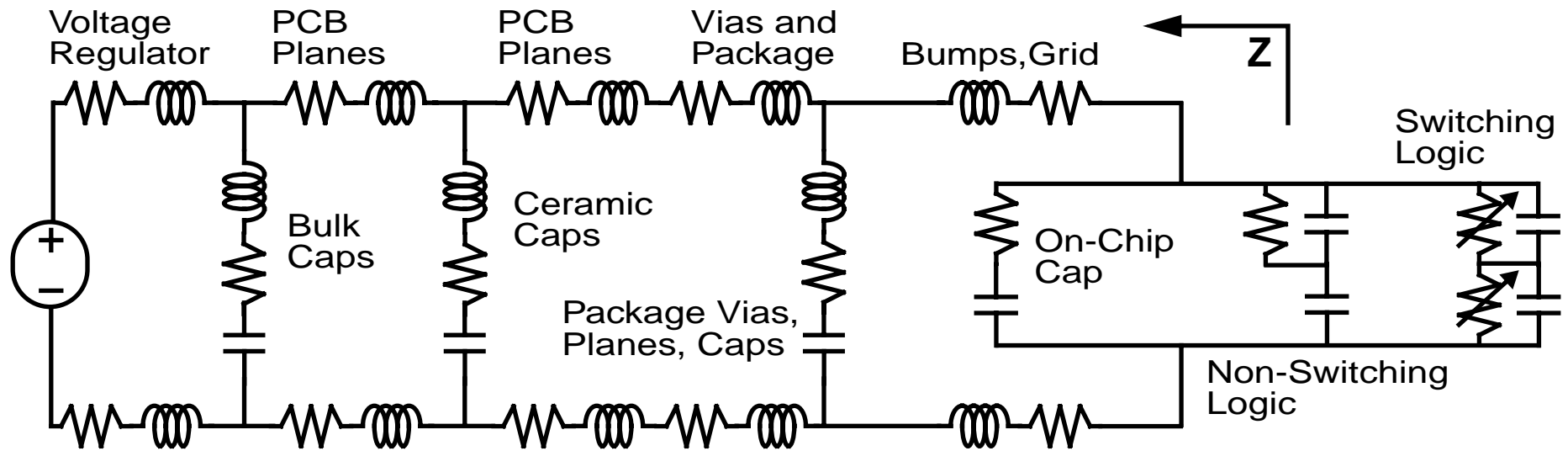


1st Order
Capacitor
Model

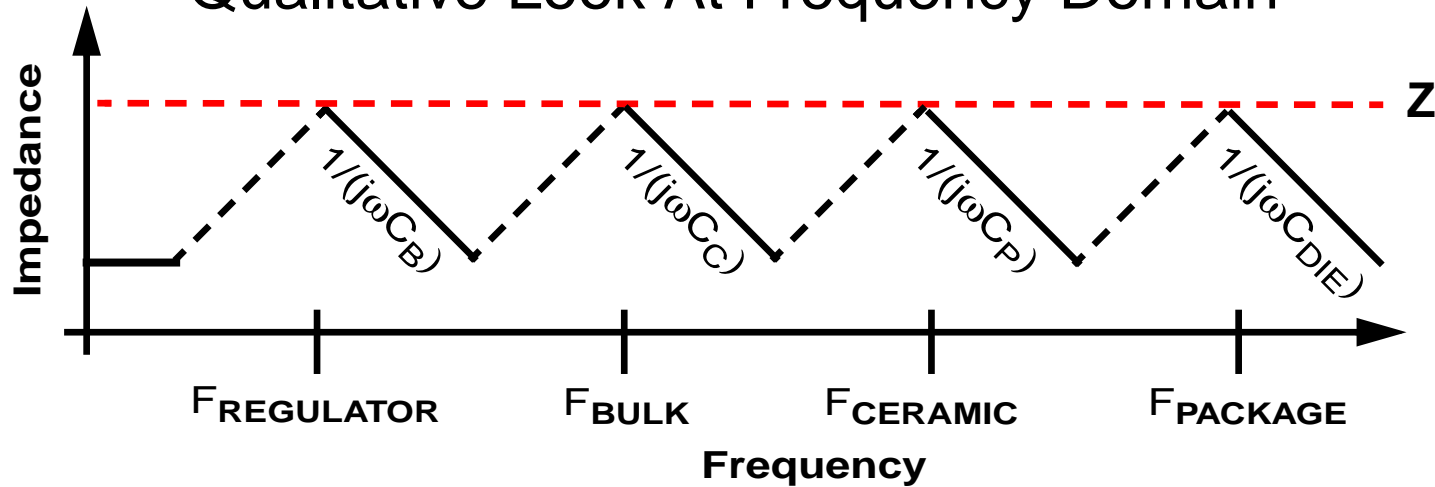


- Parasitics between banks must be included

Low Frequency Electrical View



Qualitative Look At Frequency Domain



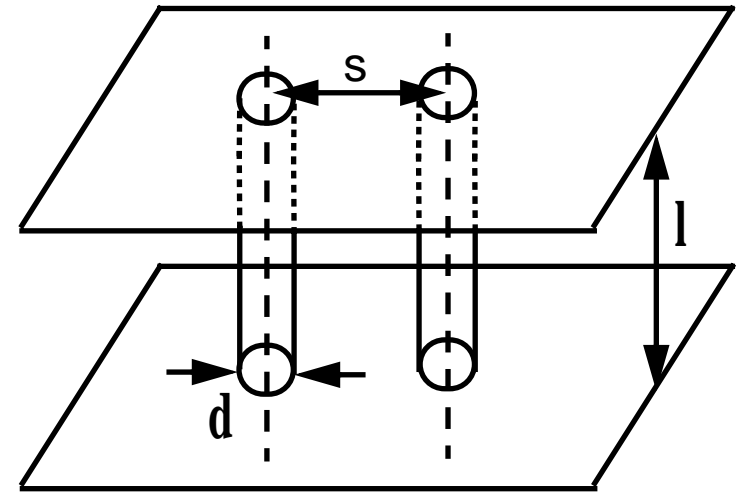
Inductance of Vias, Pins, Bumps

■ Mutual inductance [1],[2]

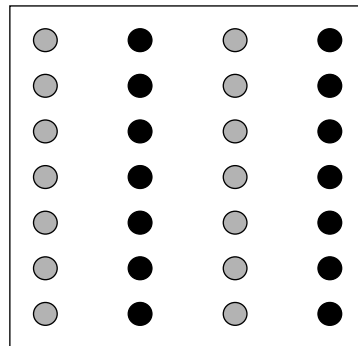
$$M = \frac{\mu_0 I}{2\pi} \left(\ln \left(\frac{l}{s} + \sqrt{1 + \frac{l^2}{s^2}} \right) - \sqrt{1 + \frac{s^2}{l^2}} + \frac{s}{l} \right)$$

■ Self inductance [1],[2]

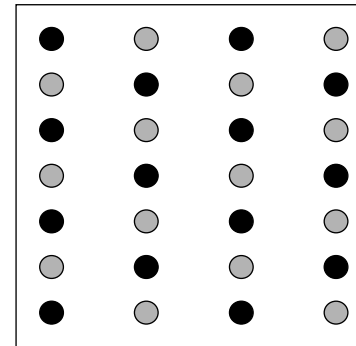
$$L = \frac{\mu_0 I}{2\pi} \left(\ln \left(2 \frac{l}{d} + \sqrt{1 + \frac{4l^2}{d^2}} \right) - \sqrt{1 + \frac{0.25d^2}{l^2}} + 0.5 \frac{d}{l} + \frac{\mu_r}{4} \right)$$



■ Loop inductance of arrays is pattern dependent [3]



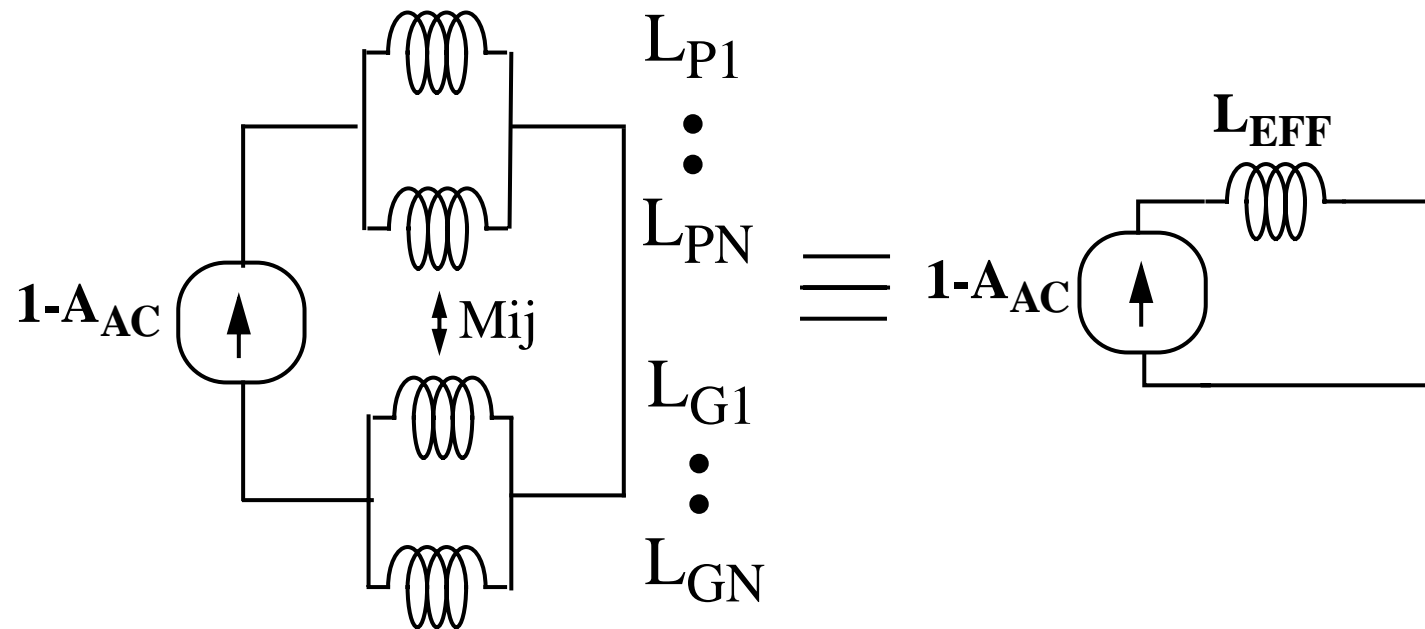
POOR



BETTER

Inductance Simplification

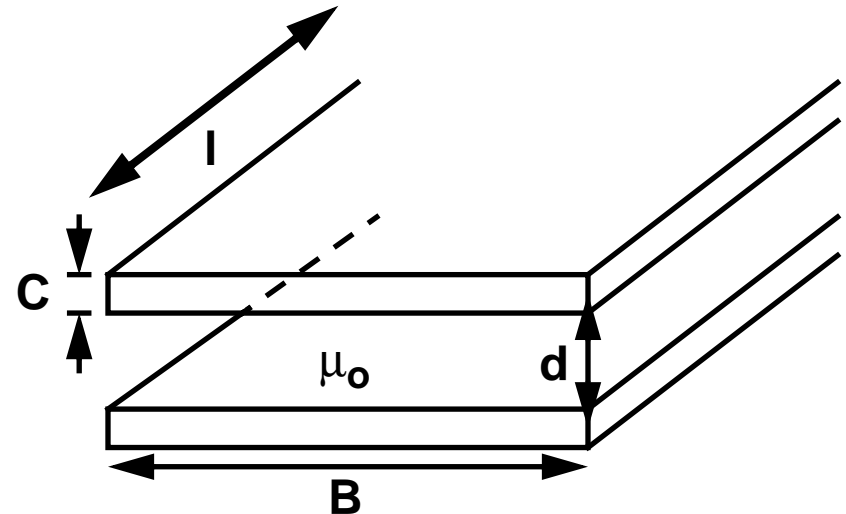
- Can collapse to single inductor
 - Use a script/spreadsheet to construct a matrix
 - Lump same-type inductors in parallel and place power and ground inductors in series
 - Simulate w/ spice in AC domain to determine equivalent series inductance ($V=I*j\omega L$)



Power Plane Inductance

- Planes are present in the package and on the board
- Loop inductance [2]:

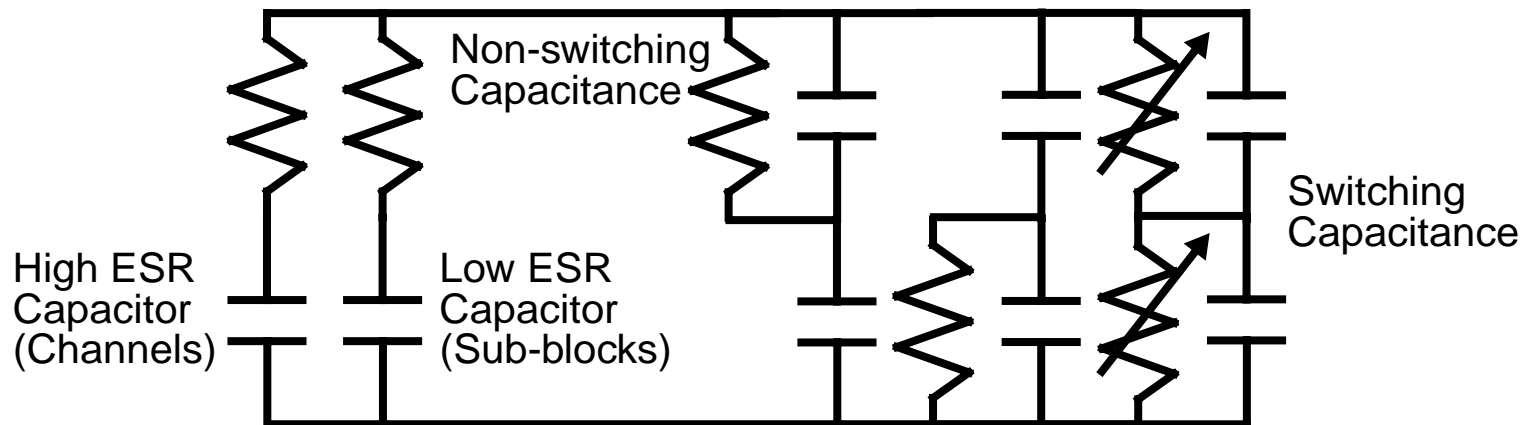
$$L = \frac{\mu_0}{\pi} l \left(\ln \left(\frac{d}{B + C} \right) + 1.5 \right)$$



- Most planes are actually perforated
- Decrease inductance for multiple pairs by $2n-1$ dielectrics, where n is the number of power plane pairs, assuming $V_{DD}-G_{ND}-V_{DD}-G_{ND}$ stack-up
- Thin spacing decreases inductance

Low/Mid-Frequency Chip Model

- Estimate switching capacitance from thermal power
 - $C_{\text{SWITCH}} = P / (V^2 f)$
- On-die decoupling capacitance is typically about 10x the switching capacitance (rule of thumb)
 - Yield issue (decoupling is ~15-20% of die area)
 - Scaling issue for process shrinks - leakage
- Equivalent series resistance (ESR)
 - Ratio of one type to the other is design-specific

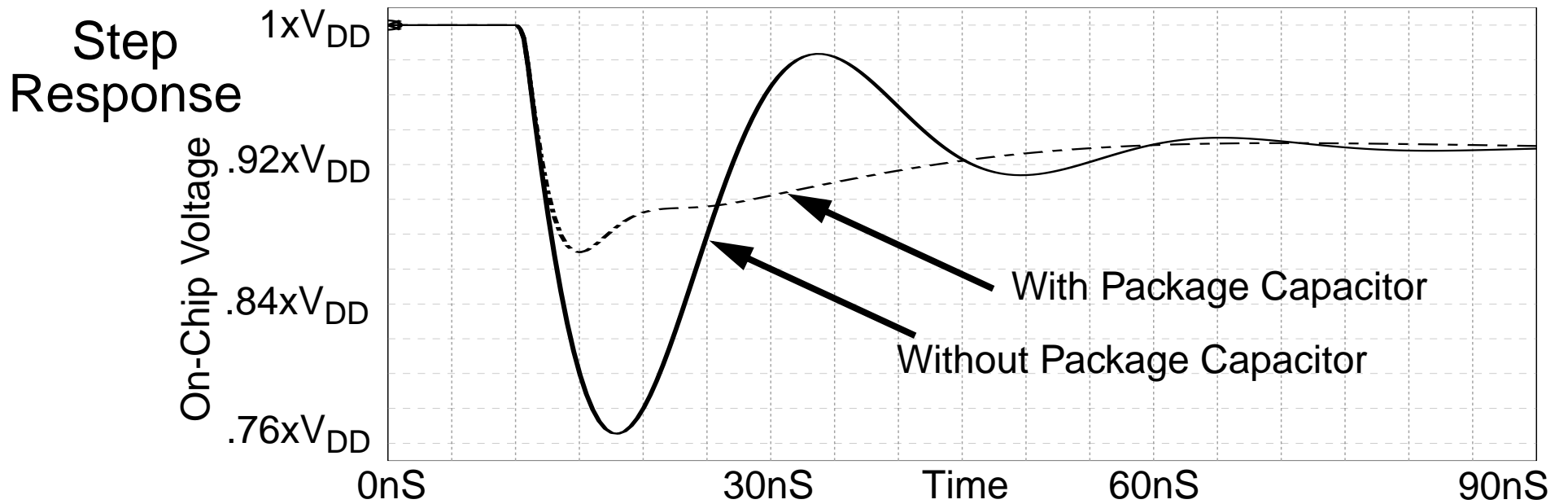
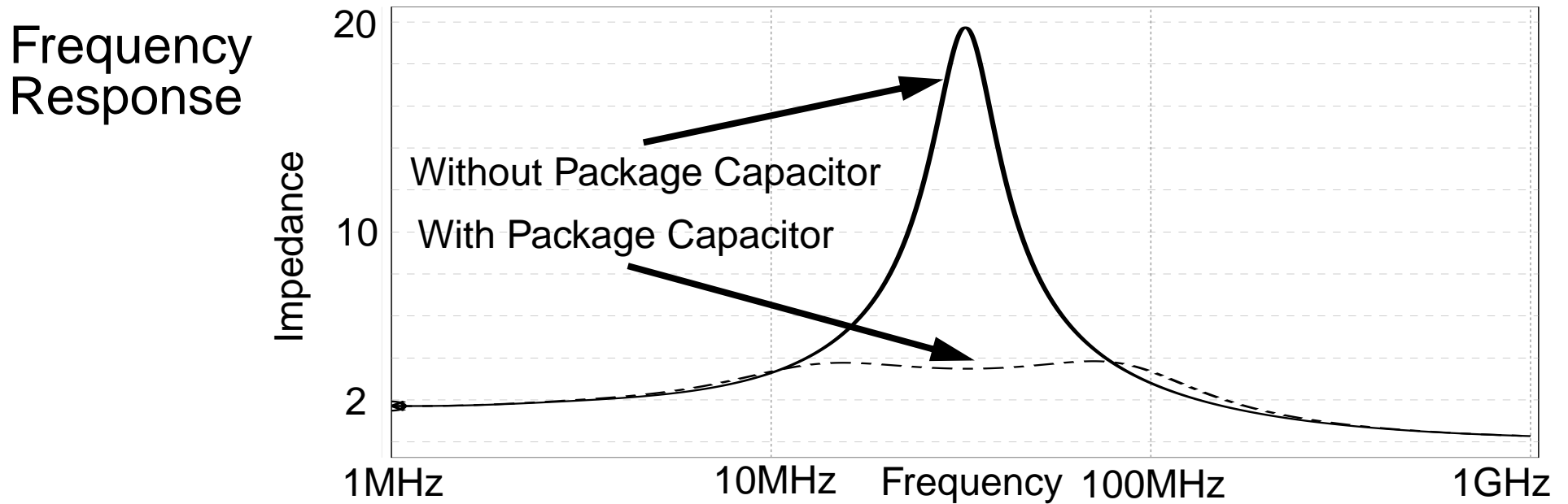


Selecting and Sizing Capacitors

- Construct system model and determine R and L from physical geometry
- Run AC analysis with circuit simulator by sweeping load switching frequency
- Different types of caps target different frequencies
 - Board Capacitor: 1-MHz to 10-MHz
 - Package Capacitor: 10-MHz to 200-MHz
 - On-Chip Capacitor: High-Frequency
- Find number & types of caps with spice simulation

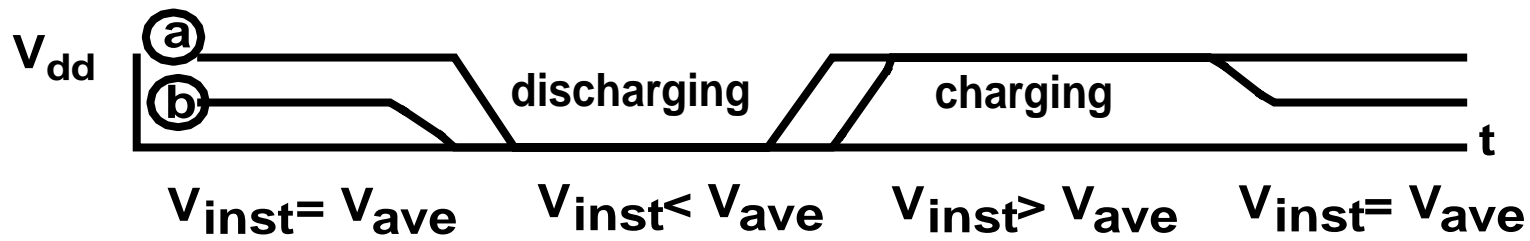
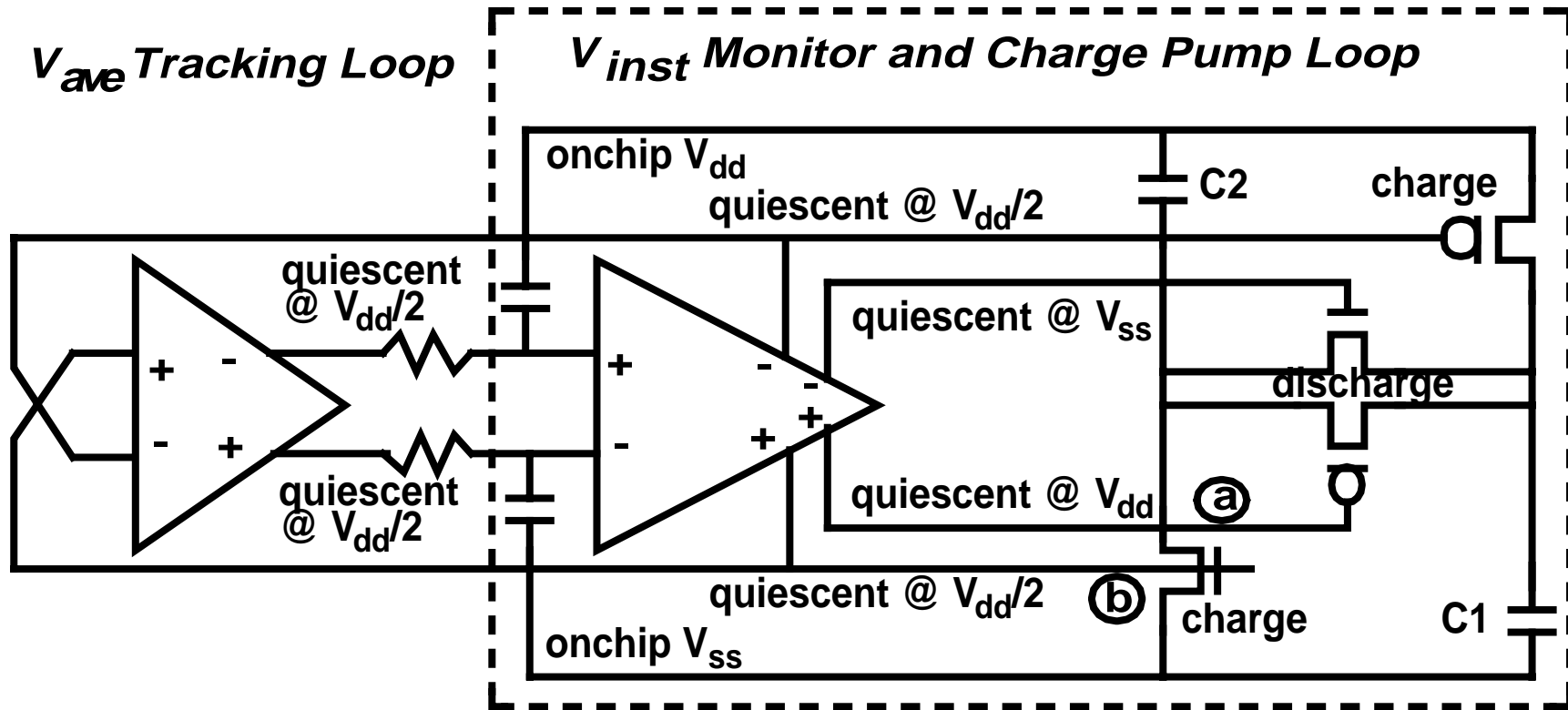
```
While (! full AND ! meeting_spec) Begin
increment num_cap
run_ac_analysis
extract_impedance
If (impedance < target) Begin
Exit
EndIf
If (full AND ! meeting_spec) Begin
replace_cap
EndIf
EndWhile
```

Decoupling Capacitor Design

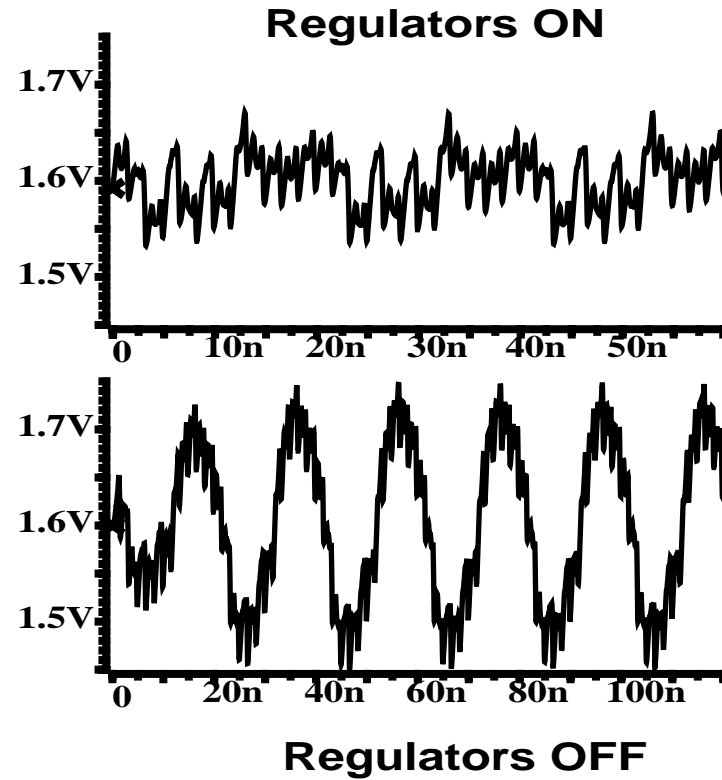
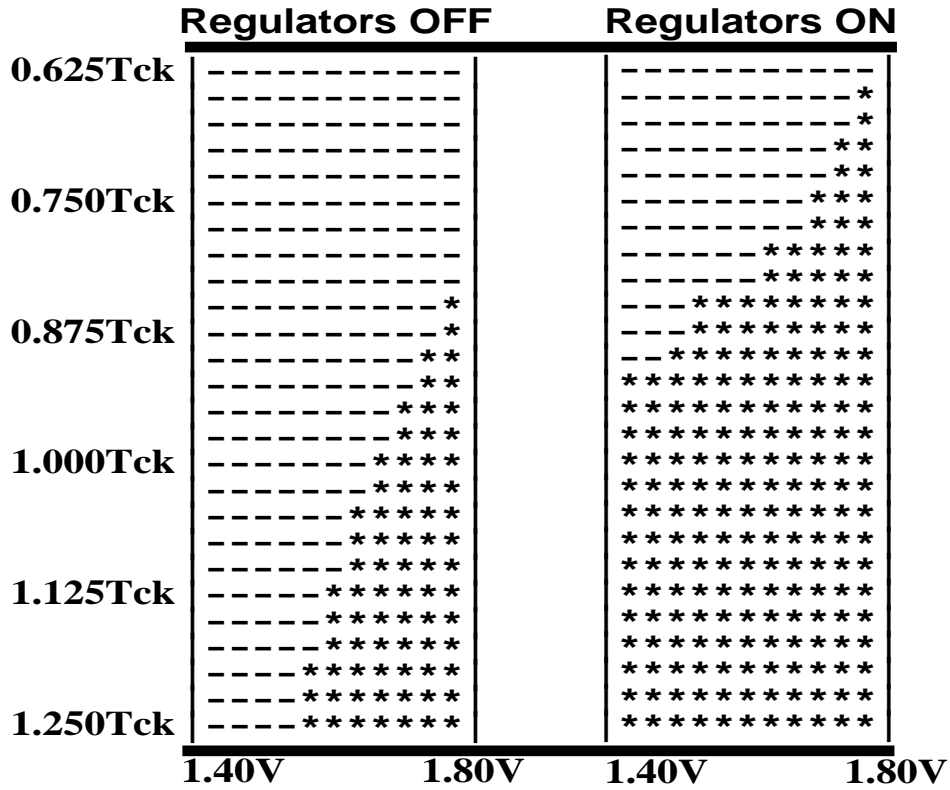


On-Die Voltage Regulator

- Detect, and actively compensate for voltage swings in the target frequency range:



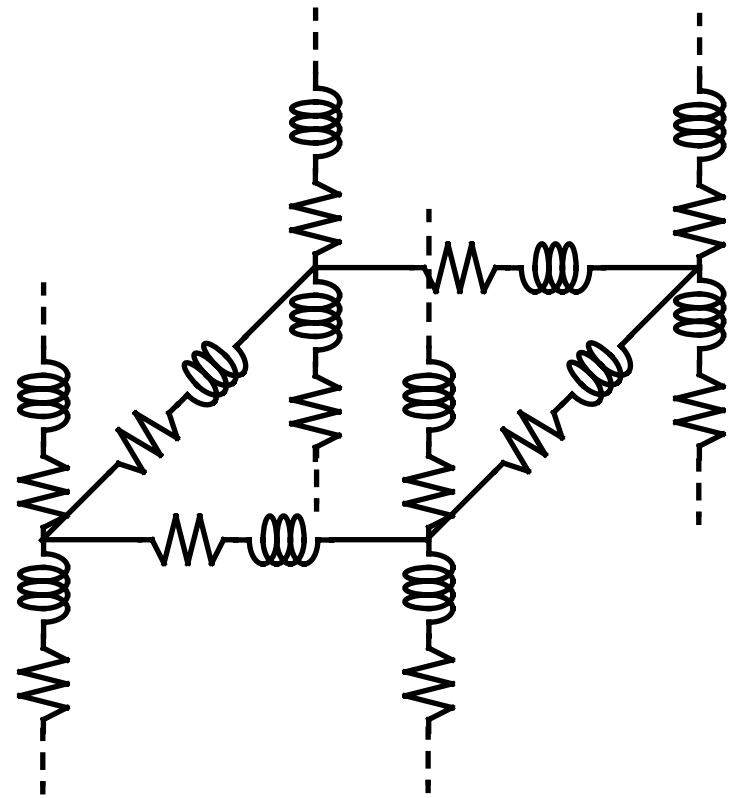
Results



■ See paper for more details

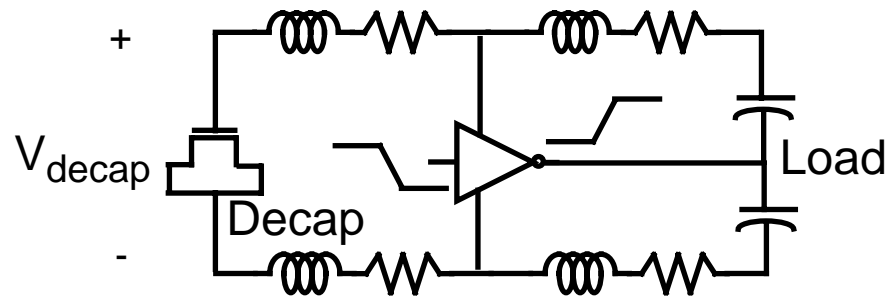
Higher Frequency Models

- Expand plane / via examples to derive a new model, with smaller 'lumps'
- Mid/high frequency
 - 3-D package/chip models
- Very high frequency
 - Small localized regions
 - 3-D chip model
 - Field solvers



On-Chip Decoupling

- Maximize on-die decoupling capacitance subject to yield/area constraints
- MOS capacitors provide on-die decoupling
 - Effectiveness is proportional to capacitor time constant - a long channel length will not decouple a signal rise time - a small channel length reduces area efficiency
 - Set a guideline based on simulations



- Scaling issue for process shrinks as rise times and parasitics scale

On-Chip Power Distribution Guidelines

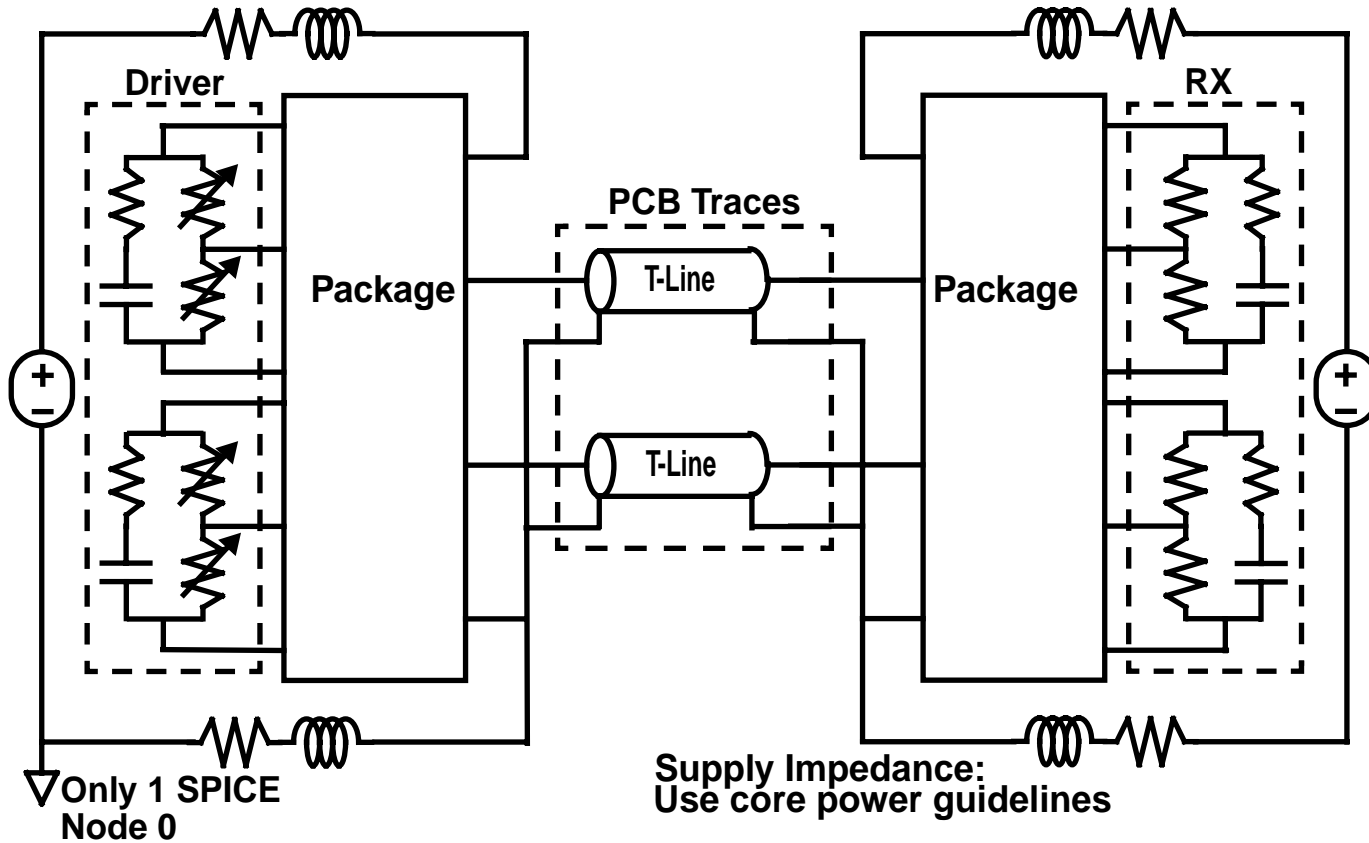
- Checkerboard bump pattern
 - Close to switching circuits
 - Watch for electromigration
- Dense power-grid
 - Alternate V_{DD}/V_{SS}
- Explore μ architectural fix for clock-gating
 - Control ramp-rates of clock gating
- Circuit techniques are also effective
 - Lower the Q of the power supply network or reduce ΔI

Off-Chip Power Delivery Guidelines

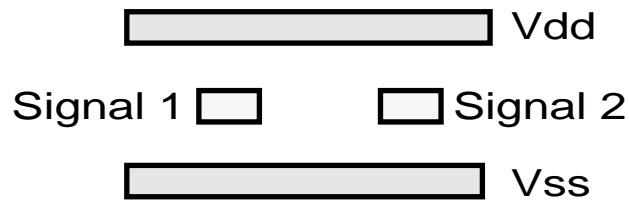
- Pay attention to the capacitor mounting and shorten the leads
- Place capacitors close to the chip
- Reduce spacing between planes
- Add more V_{DD} , V_{SS} planes in an alternating pattern
- Sockets, vias, bump arrays
 - Use checkerboard patterns where possible
 - Use as many parallel paths as possible, without eating up the entire plane with anti-pads

I/O Signaling

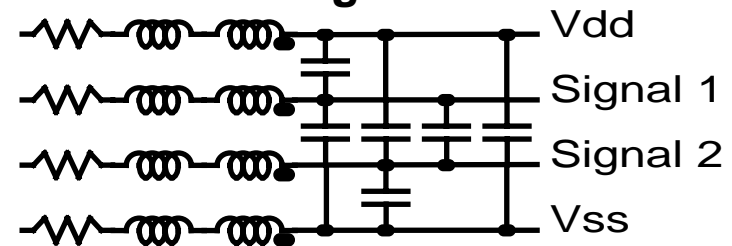
- Two separate paths to consider: power, signal return



Package Cross-Section

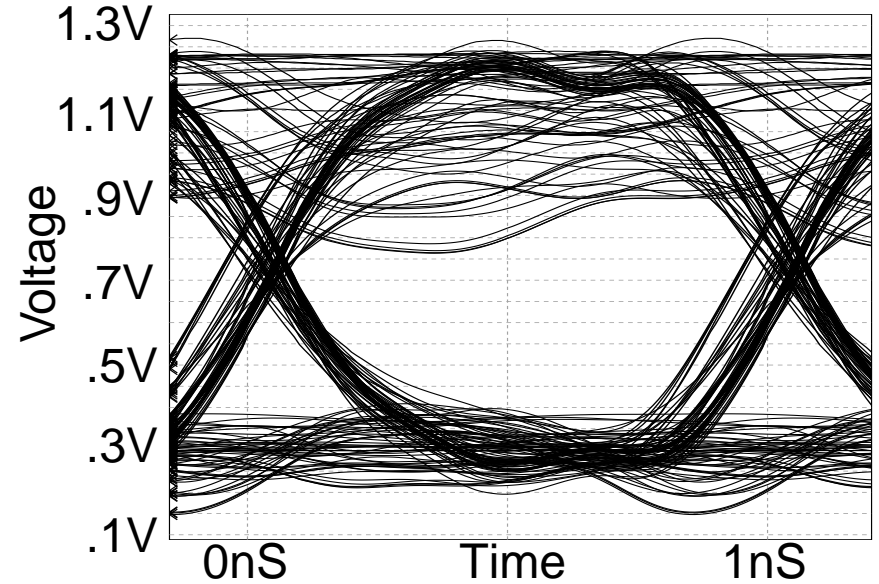
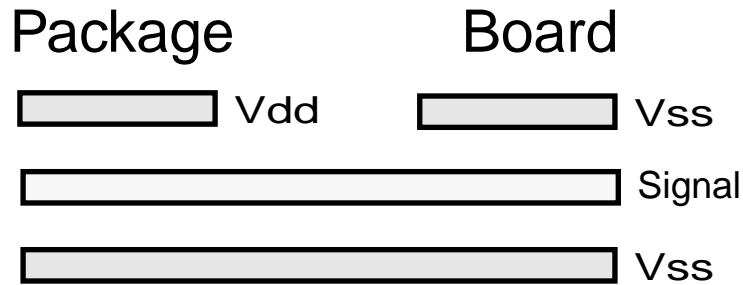


Package Model

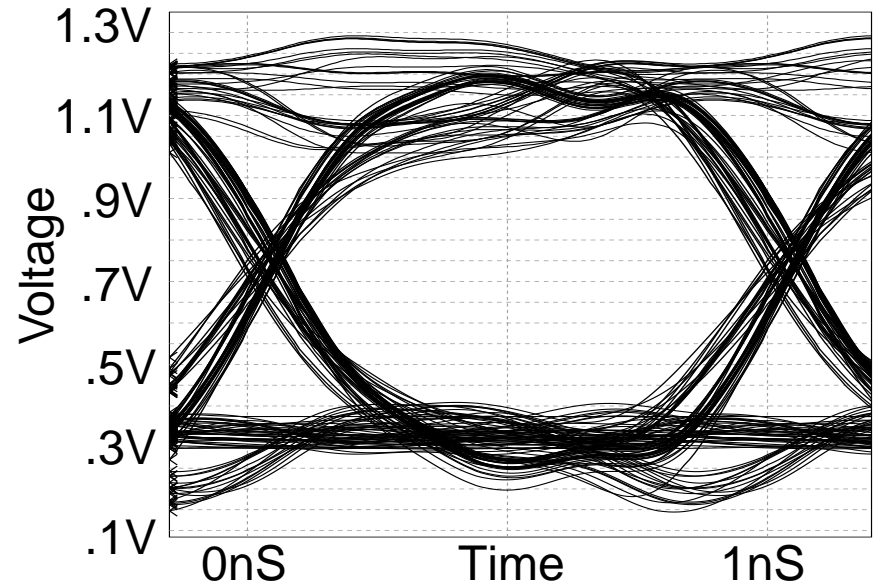
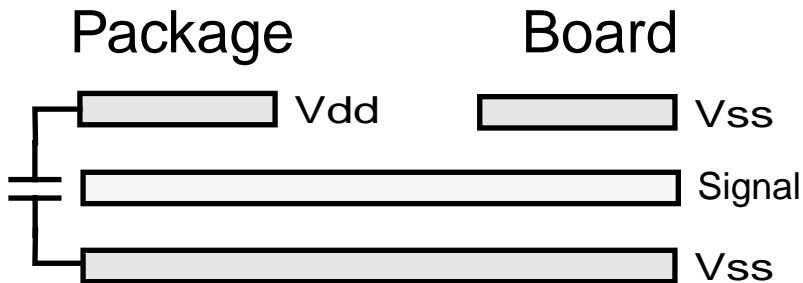


I/O Example

- How does signal return current get from board (V_{SS} only) to package (V_{DD}/V_{SS})?



- Package capacitors to reduce signal return impedance?

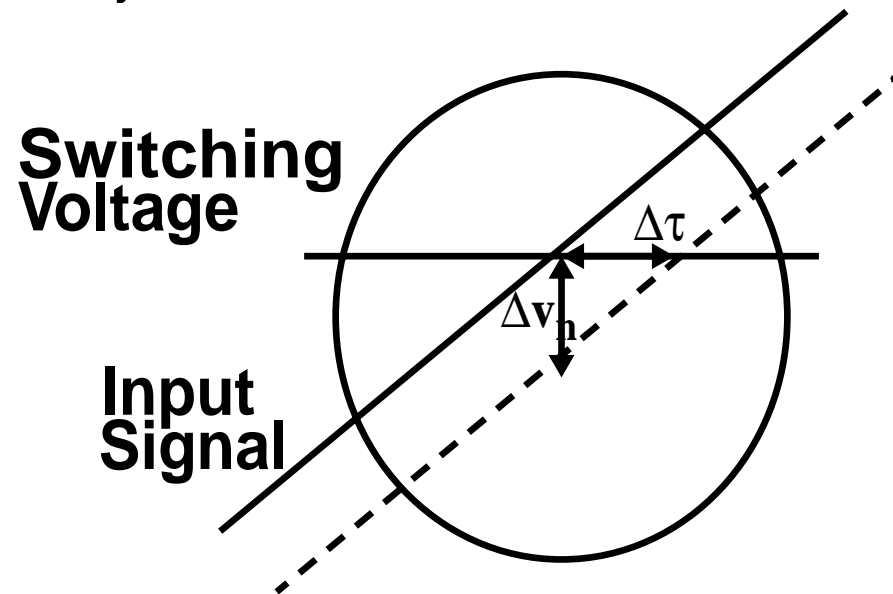


High-Speed I/O Guidelines

- Power Distribution Impedance
 - Same guidelines as core power
- Signal Return Impedance
 - Maximize the power/ground pins in the chip, package, and connector pin-out (under cost constraint)
 - Careful routing to avoid discontinuities
 - Minimize the effects of discontinuities by providing an alternate return path (i.e. through a decoupling capacitor)

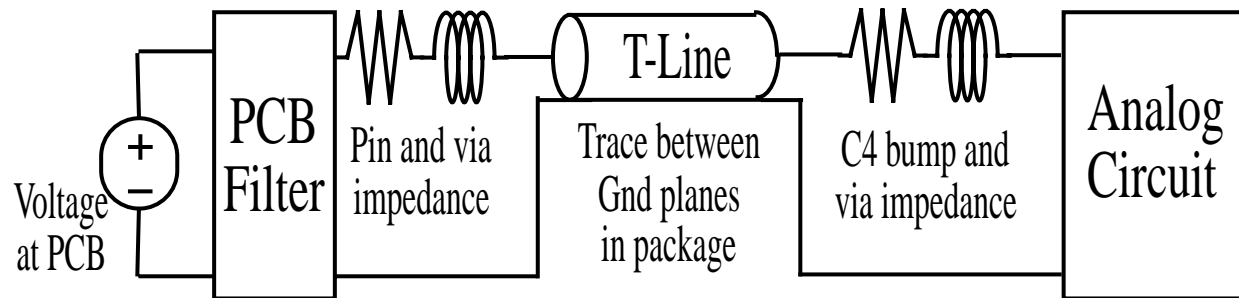
Analog Power

- Noisy digital circuits & sensitive analog circuits share the same environment
 - Power supply coupling
 - Crossing supply domains
- Quiet V_{DD}
 - In microprocessor PLLs and DLLs power supply noise dominates jitter

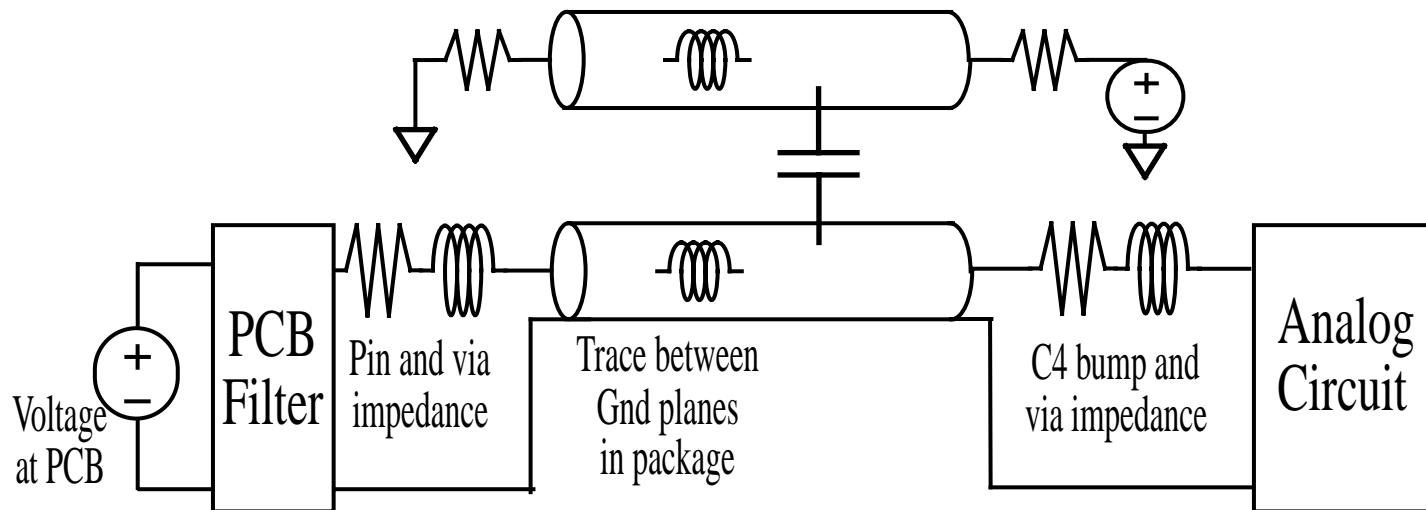


Providing Clean Analog Supplies

- On chip methods: regulators and RC filters
- System level approach:
 - Use separate trace for supply and PCB filter

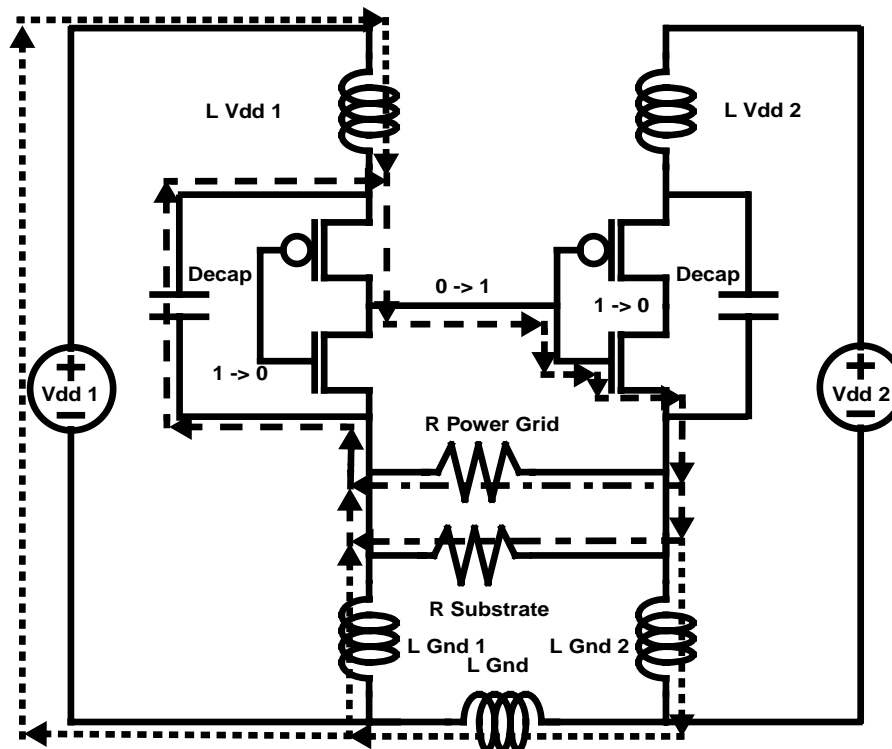


- Can model coupling from other traces/vias



Crossing Supply Domains

- What about noisy on-chip V_{SS} ?
 - V_{SS} isolation can be costly
 - Use shorted V_{SS} as on PCB
- Force V_{DD} to track the local V_{SS}
 - Reference bias lines to V_{DD} , decoupling capacitors



Summary

- Several important aspects of delivering clean power
 - Supplying power across a broad frequency spectrum
 - Decoupling capacitor sizing and placement
 - I/O return current discontinuities and supply impedance
 - Solutions encompass board, package, chip
- Modeling concepts
 - Vias, bumps, pins, power planes, capacitors, and processor
- General guidelines for power distribution

References

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