Lecture 18

Final Project Statistics

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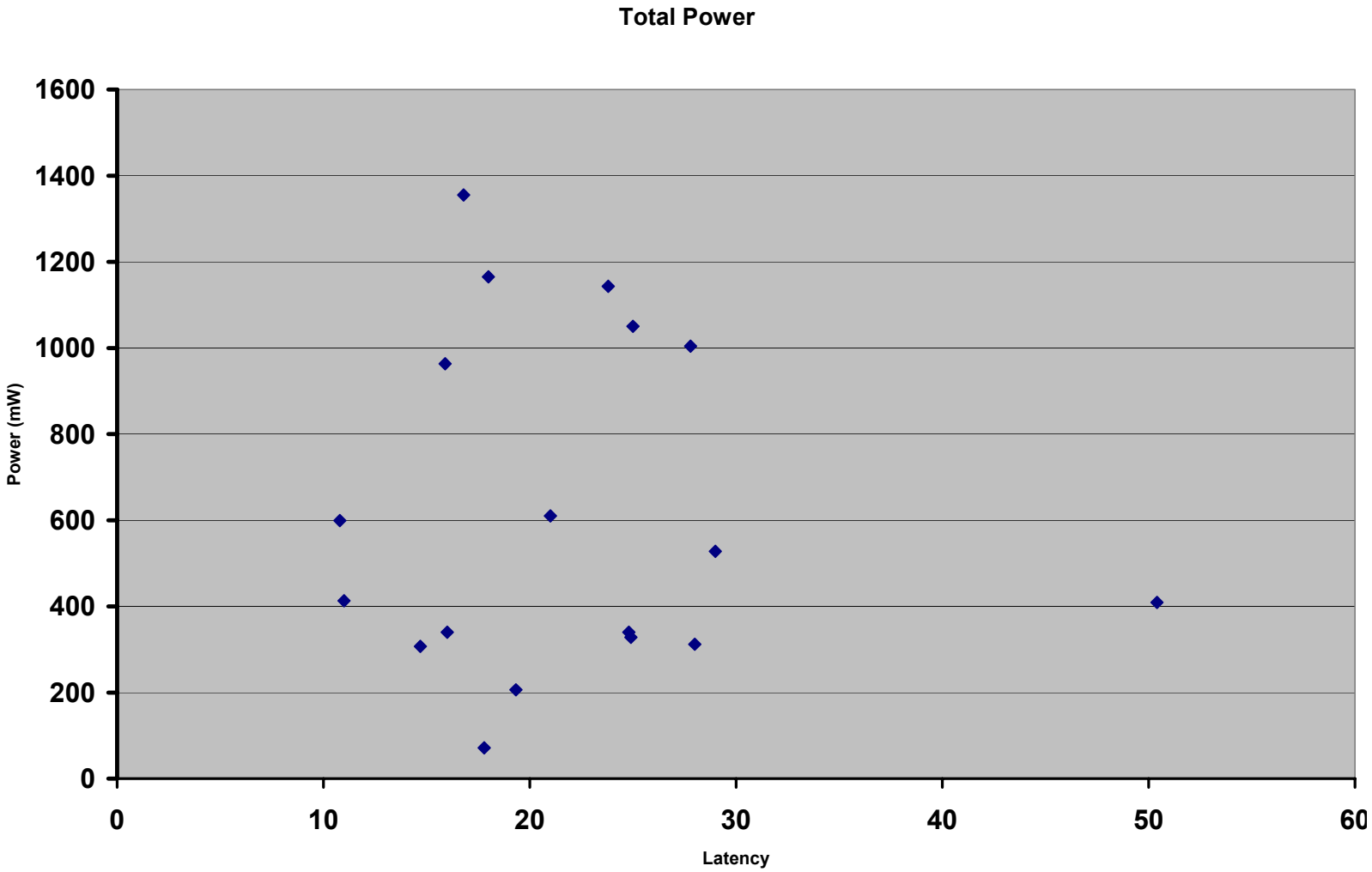
Overall

- 19 project papers turned in
  - Still waiting for a few SITN's to arrive
  - Report "size" ranged from 18 pages to 70 pages
- No strong trends
  - Speed and power do not seem to track circuit style very well
    - Static adders on the slower side, but still consume a lot of power
    - OPL adders on the faster side, but consume low power
    - Dynamic adders run the gamut
- Pipestages
  - Majority of design went with single pipestage (14)
  - Handful added add'l pipestage (4)
    - Frequencies generally on faster side for these designs
    - Latency tends to be on the slower side

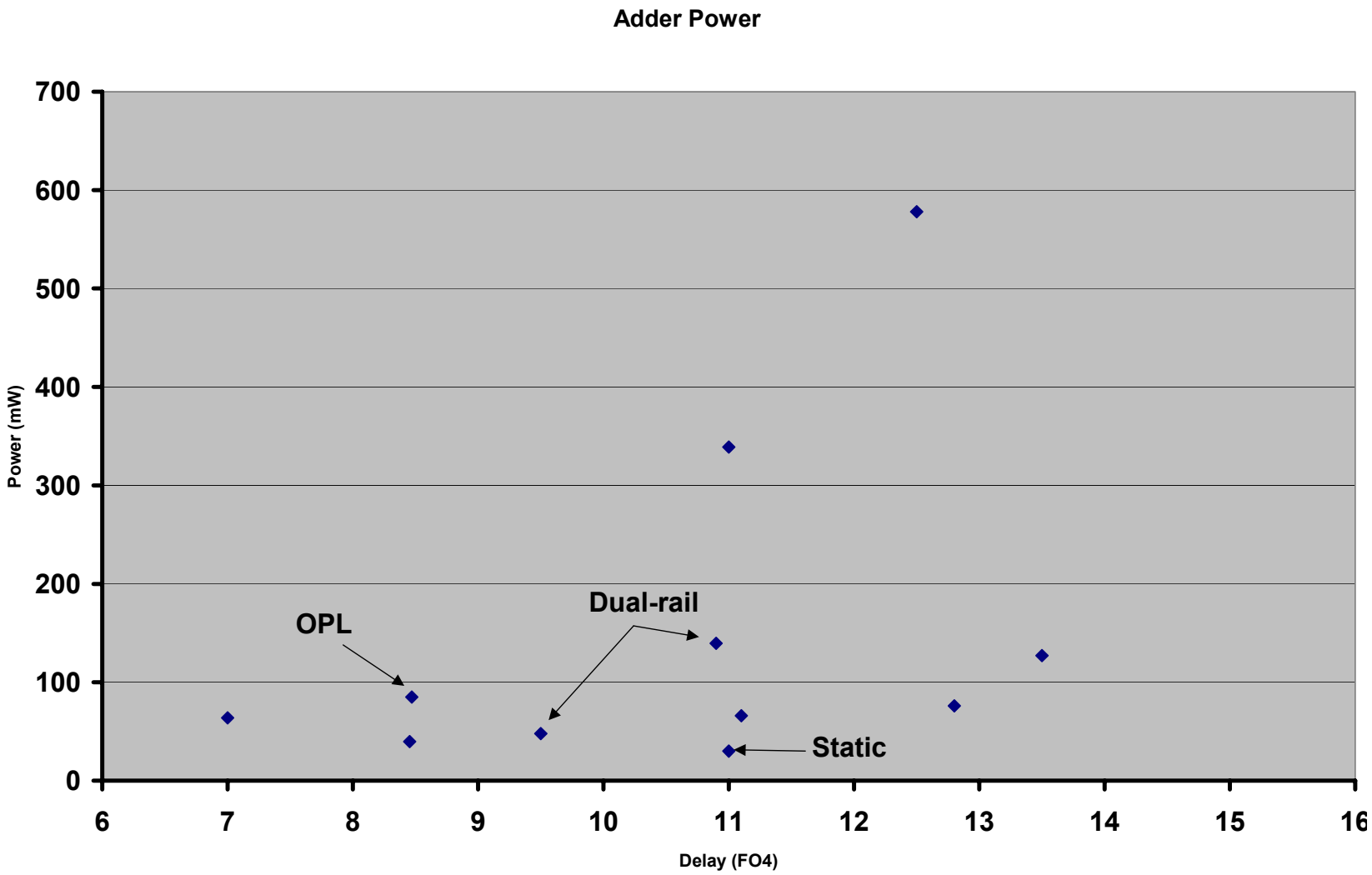
Latency vs. Power



Adders

- Majority are dynamic (15)
  - 5 of these are dual-rail
- 2 Static designs
- 2 OPL designs
- Adders primarily followed examples from Harris and/or Alpha adder presented in class
- Power and Speed trends
  - Speed “roughly” follows expectations
  - Power varies wildly

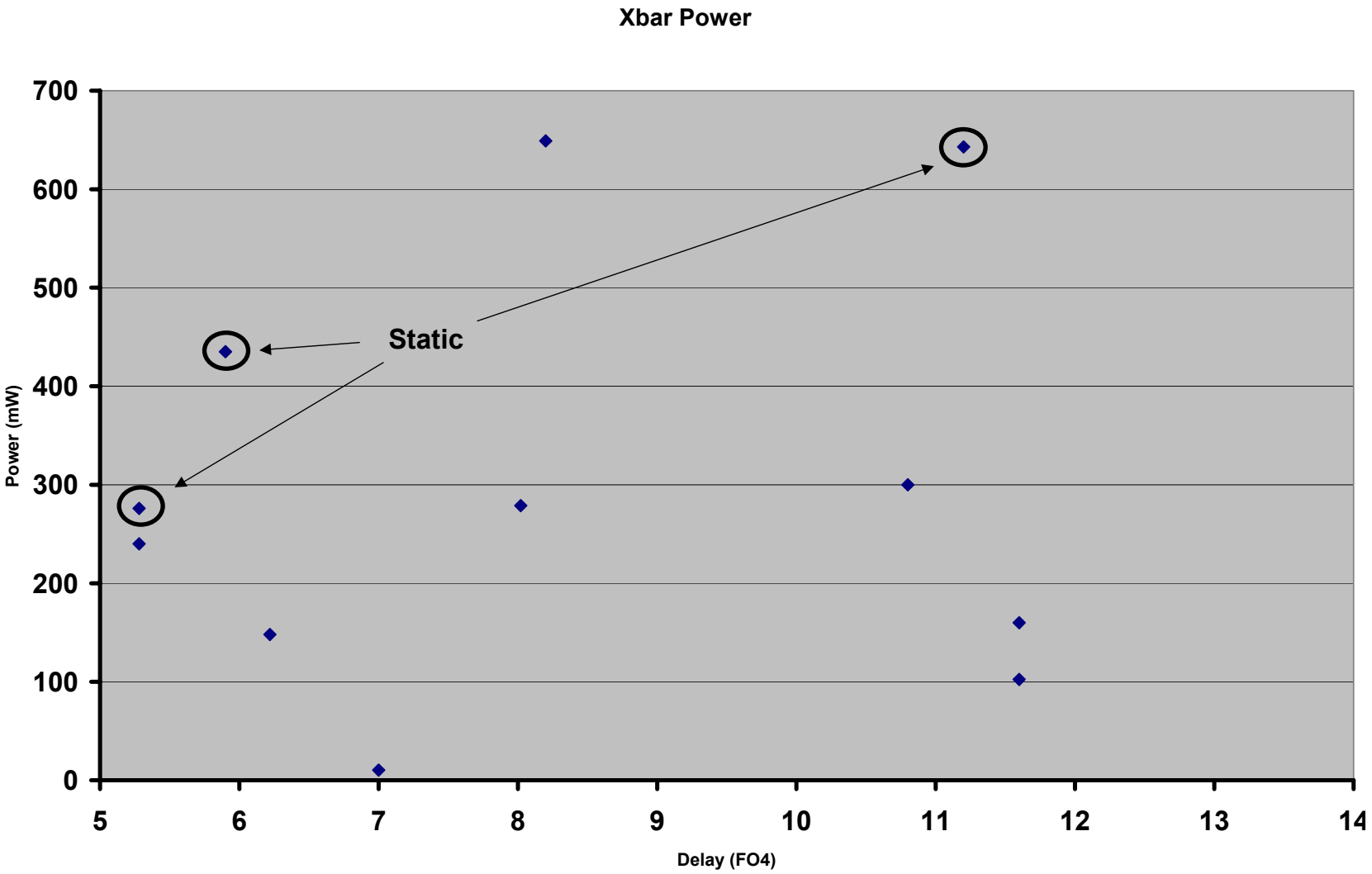
Adder Speed vs. Power



Crossbar

- Good mix of different styles
  - 5 full rail, static designs
  - 6 low swing
  - 3 low swing, differential signaling
  - 4 low swing, pseudo-differential
- Power and Speed trends
  - No strong trend for either power or speed

Crossbar Speed vs. Power



Clocking

- Distribution styles were all fairly consistent
  - Still evaluating buffer depth, but approx. 5 – 10 stages
  - From final point of divergence, most design had 2-3 stages
- Skew
  - Lots of variation: 0 – 1.66 FO4
    - Average: 0.94
  - One paper used deskewing buffers to attempt to reduce skew
- Jitter
  - Even more variation: 0.03 – 1.47 FO4
    - Average: 0.55
- Power
  - The most variation: 9.8 – 1000mW (wow!)
  - Follows general circuit styles (static and OPL), however, dynamic varies substantially

Presentations

- Weaver, Yue
  - Four phase clocking design and analysis
- Kavousian, Amirkhany
  - Crossbar wire sizing analysis
  - Crossbar low swing implementation and analysis
- Beckman, Gupta
  - Crossbar low swing signaling implementation
- Goodwill, Iroaga
  - Output Prediction Logic (OPL) adder implementation
  - Deskew'd clocking network