Deep Sub-Micron Cache Design

Agenda

- Bitcell Design
- Array Design
- SOI Considerations
- Surviving in the corporate world
Older Bitcell Design (>=130nm)

**Design**
- Pulldown / Passgate of 1.6 – 2.0
- Pullup small as possible
- Pullup / Passgate ~ = 1
- Use non-minimum channel length for Passgate devices

**Analysis (DC)**
- Run Static Noise Margin analysis for read stability
- Run Writability Analysis

**Results**
- Device variation did not greatly impact bitcell design.
- Redundant elements used primarily to repair hard defects
- Multiple-bit defects usually had a row failure signature
Current Bitcell Design (<= 90nm)

**Design**
- Pulldown / Passgate >= 2
- Pullup small as possible
- Use non-minimum channel length for all devices

**Analysis**
- Run AC Read Stability analysis with max device variation
- Run AC Writability Analysis with max device variation

**Results**
- Device variation greatly impacts the bitcell design!
- Redundant elements used primarily to repair soft defects
  - Weak bits limit frequency and can cause Vmin failures
- Multiple-bit failures typically exhibit column signatures

Array Design in Deep Sub-Micron
Array Design for Deep Sub-Micron

- Establish clear array design guidelines
  - Dynamic Logic guidelines
  - Unprotected input guidelines
  - SRAM and Sense Amp guidelines

- Must take process variation into account during design
  - 5-6 sigma bitcell design
  - 2-3 sigma sense amp
  - 2-3 sigma precharge

- Design for clock duty-cycle variation
  - Hard to ensure 50/50 duty cycles at higher frequencies
  - Design for 60/40 and 40/60 worst-case duty cycles if possible

Array Design for Deep Sub-Micron

- Simulate multiple process corners
  - Use TYP, nominal voltage, high temp for speed sims
  - Use FP/FN, max voltage, high temp for max-power sims
  - Also use SP/SN, FP/SN, and SP/FN, nominal voltage, high temp to maximize yield at lower speed grades
  - Need to also simulate low voltage and low temp effects

- Work with product engineering to address yield issues

- Review all layout
  - The engineer is responsible for the quality of the layout

- Use CAD tools to verify array design, not to do array design

- Conduct formal peer reviews of design and layout
Array Design for Deep Sub-Micron

Array Cross Sections

- Build up simulation cross sections of all paths such that schematic blocks can be replaced with extracted data
- Use 4x4 grouping of bitcells as basis for RAM modeling
  - Extract entire 4x4 bitcell layout
  - Use only inner 2x2 group of cells for simulation
- Use mults on symbols to correctly model loads
- Model all parasitics
  - Wire parasitics
  - Gate and diffusion loads

4-Corner RAM Model for 32x32 sub-array
Array Design for Deep Sub-Micron

Full Sub-Array Model

4-Corner Sub-Array Model (32x32)

Designing with SOI
**Designing with SOI**

**Pros of designing with SOI**
- Less source/drain capacitance means higher speed
- Less source/drain capacitance means lower power
- No danger of CMOS latch-up
- SER improvement in SRAM bitcells

**Cons of designing with SOI**
- Floating Body increases device variation
- History effects
- Differences in timing based on switching
  - First switch slower than second switch
- Bipolar parasitic effects impact circuit structures
  - Pass-gates
  - Dynamic Logic
  - Array bitlines
- SER degradation in dynamic circuit structures
### Designing with SOI

#### First Switch vs Second Switch

- After the sufficient time has passed for the device to reach DC equilibrium, the first transition to occur will be slower than the next transition due to body effects.
- Timing simulation strategy must take into account both 1\textsuperscript{st} switch and 2\textsuperscript{nd} switch timing.

![Diagram of first and second switch with time to reach DC equilibrium](image)

#### Dynamic Logic

- Bipolar parasitic effect impacts intermediate node voltage
  - Can’t pre-charge intermediate nodes to Vdd as in bulk
    - Increases charge sharing
  - Penalizes NFET Nand Structures
    - Need to decrease stack height in dynamic circuits
  - Increases parallel leakage in NFET Nor trees
Designing with SOI

SRAM Design

- Bipolar parasitic effect impacts bitline leakage
  - Parasitic bipolar device on bitcell pass-gates causes additional leakage on bitline
  - Must simulate worst-case reads using opposite data in all other rows in the given column

- History Effect can cause a read/write of a given value to fail immediately following several successive reads/writes of opposite data
  - Must add read/write hammer tests to production tests to detect failures

Sense Amp Design

- Floating body increases sensitivity to process variation
  - Must use body ties on devices sensitive to variation
  - If bodies are not tied to ground, bodies must be shielded to avoid noise problems

- Sense Amp is also subject to history effects
Surviving in the Corporate World

- Be a team player
  - This sometimes means doing boring work

- Pay your dues
  - New grads will often be given simple, boring tasks at first
  - Don’t complain about boring task – your time will come!

- Act professionally when dealing with other groups in the company
  - Be nice, even if others are not being nice
  - Resist getting angry
  - Don’t attack others
  - Focus on solving the technical problem at hand
Surviving in the Corporate World

• Don’t try to save the world – the world doesn’t want saved!
  – Report what you find to your manager, let him/her save the world
  – Just make sure your piece of the world works OK!

• Learn all you can from the senior designers in your group
  – Education doesn’t stop with college
  – It’s up to you to make sure you understand how things work
  – Learn all parts of doing design
    • This includes Design for Manufacturing (DFM) and Design for Test (DFT)

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