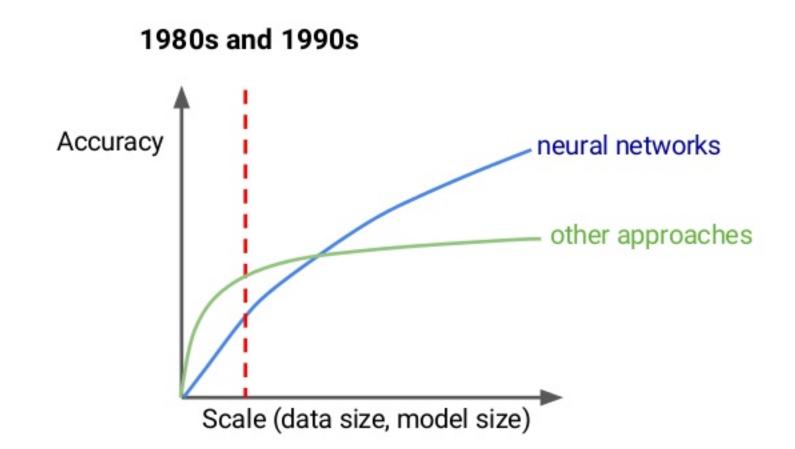
Automatically Discovering Systems Optimizations for Deep Learning

Zhihao Jia

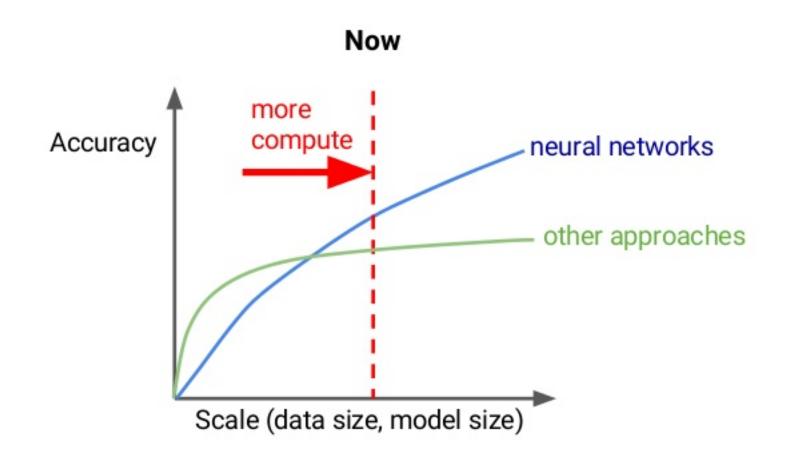
CMU and Facebook

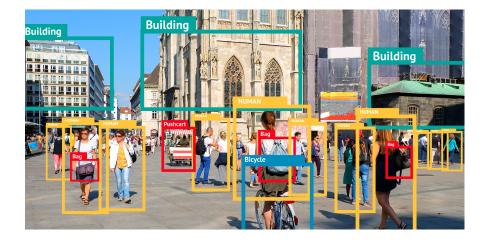
2/11/21

The Rise of ML and Neural Networks



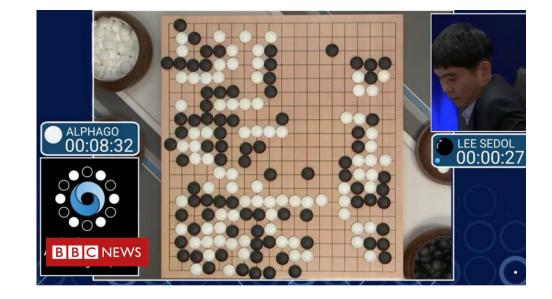
The Rise of ML and Neural Networks



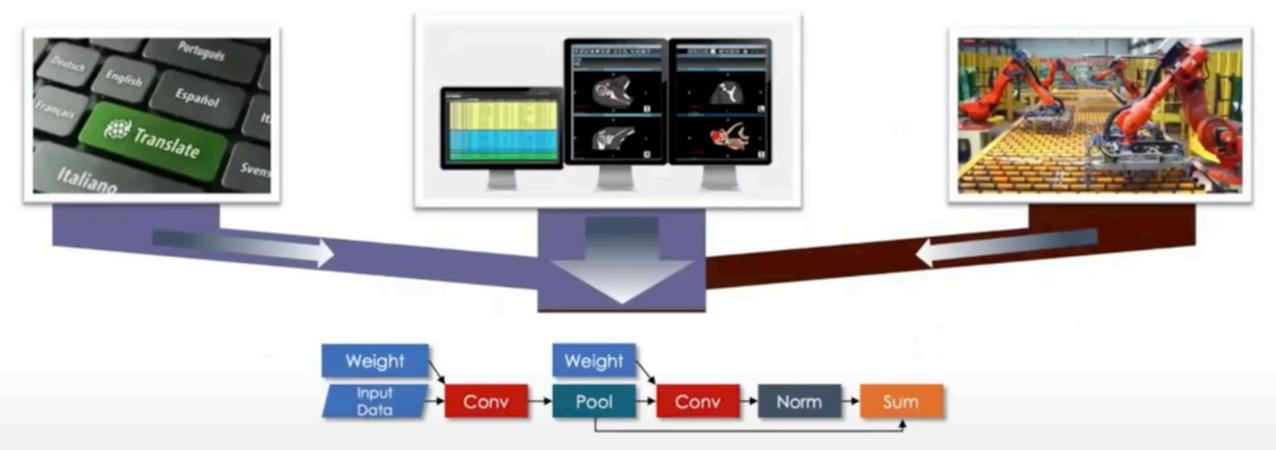








Deep Neural Networks for Machine Translation

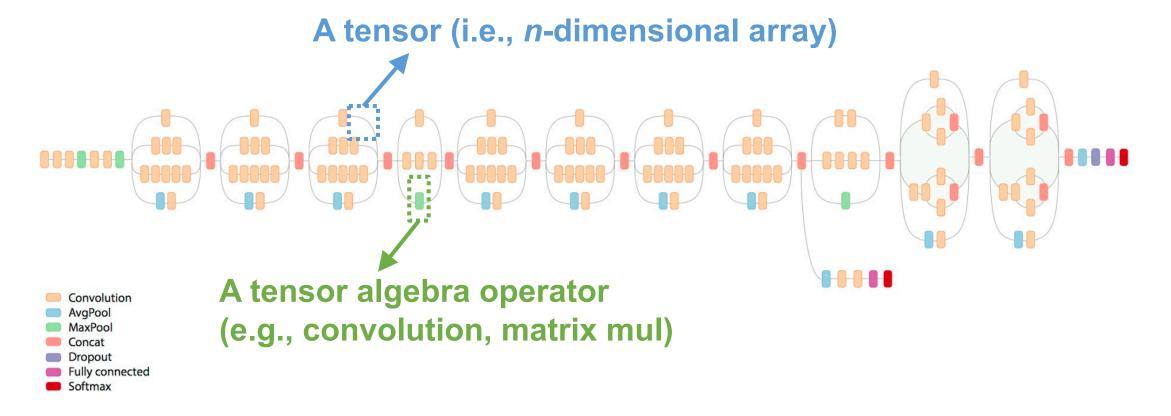


1000x Productivity

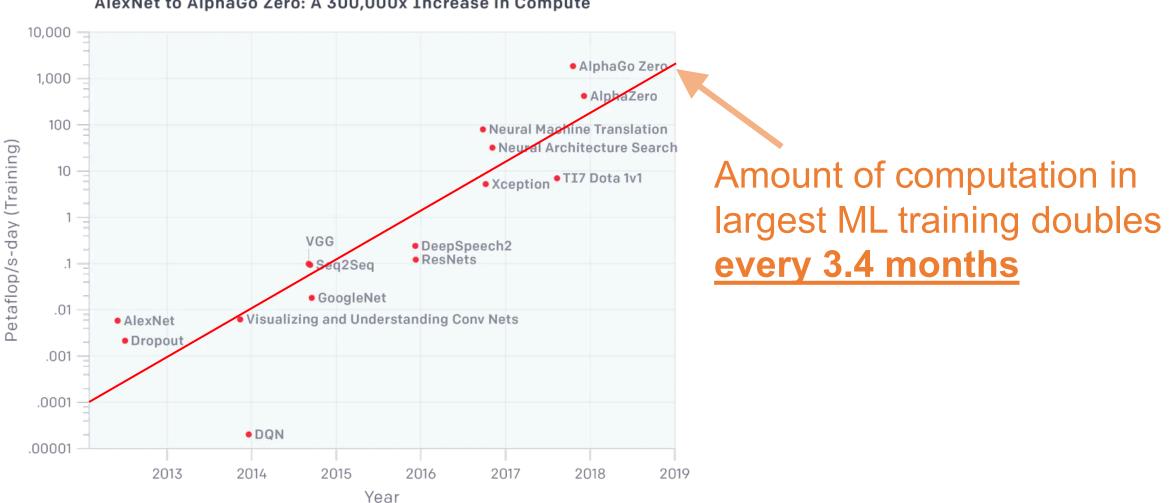
Google shrinks language translation code from 500k imperative LoC to **500 lines of dataflow**

What is a Deep Neural Network?

 Collection of simple trainable mathematical units that work together to solve complicated tasks

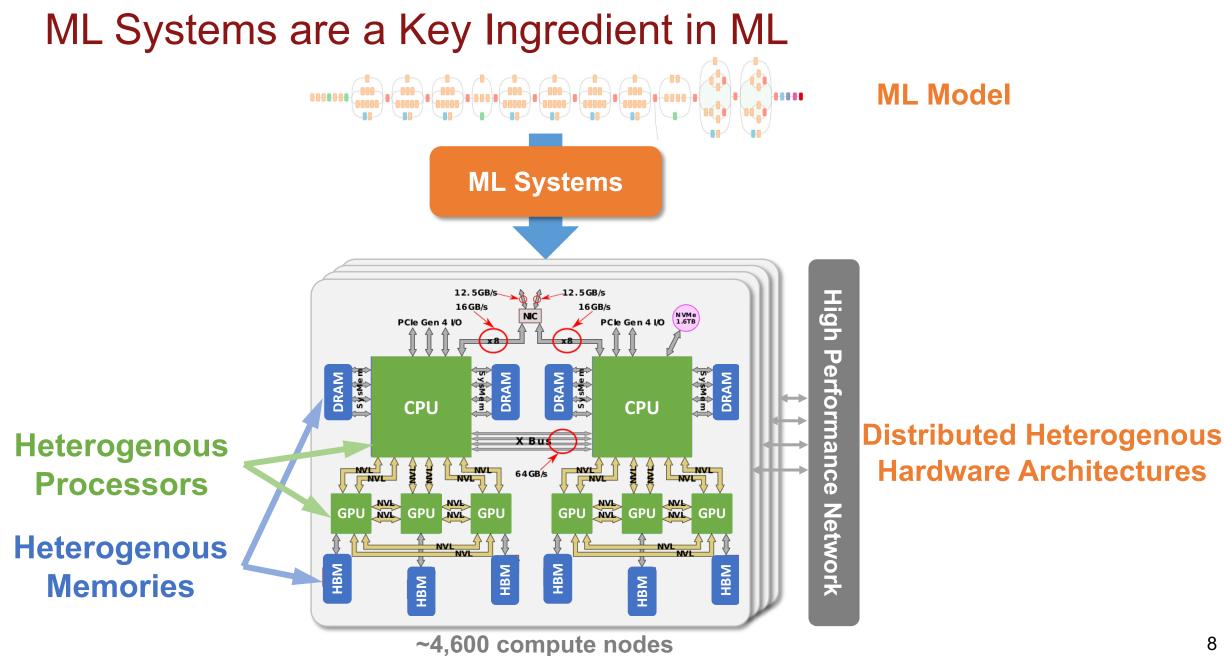


ML Computation is Increasing Exponentially

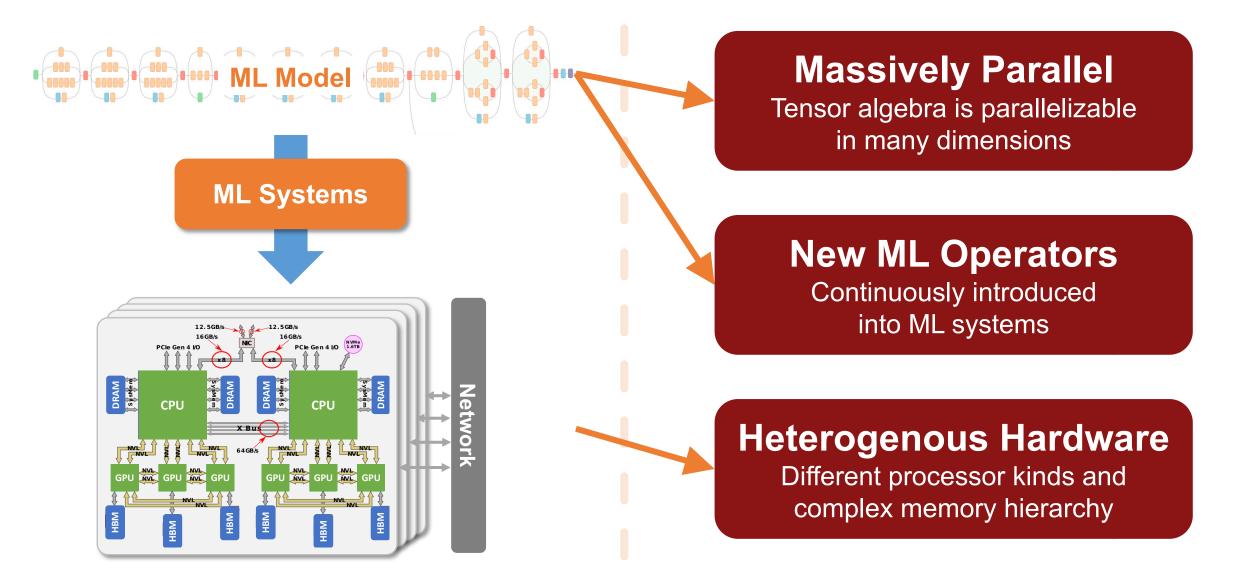


AlexNet to AlphaGo Zero: A 300,000x Increase in Compute

[[]OpenAl Blog, 2018]



Challenges of Building ML Systems



CMU Automated Learning Systems Lab

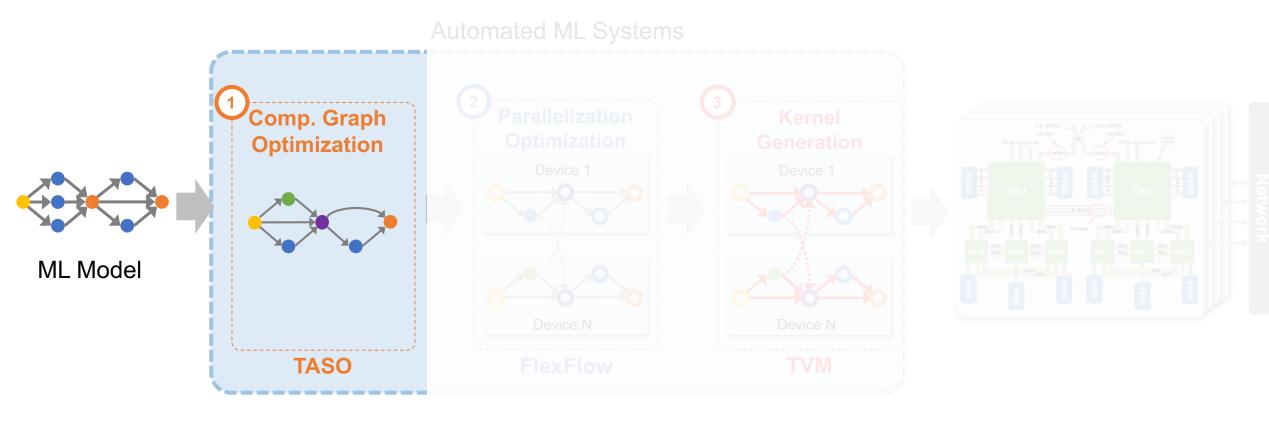
Mission: Automate the design and optimization of ML systems by leveraging

- 1. Statistical and mathematical properties of ML algorithms
- 2. Domain knowledge of modern hardware platforms



https://catalyst.cs.cmu.edu/

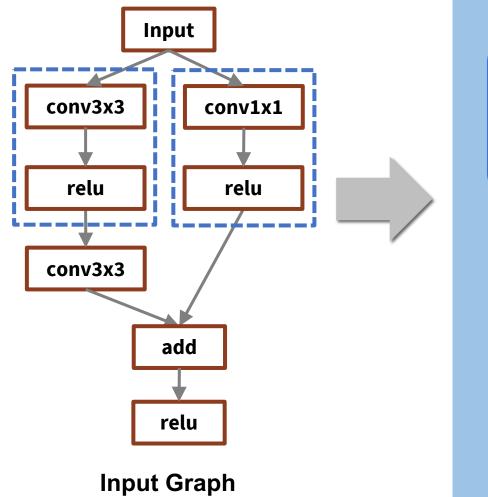
CMU Automated Learning Systems Lab

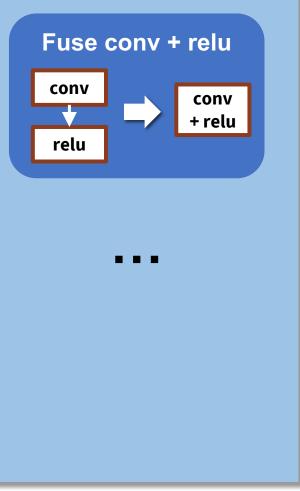


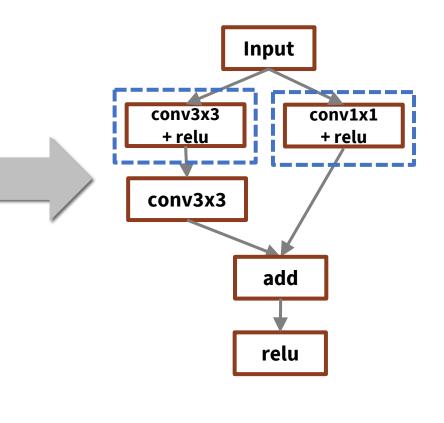


https://catalyst.cs.cmu.edu/

Current Rule-based Graph Optimizations







Optimized Graph

Rule-based Optimizer

// during inference. Current Rule-based Graph Optimizations "*"}, {"Const"}, {"Const"}, // clang-format on Fuse conv + relu 60 69 **TensorFlow currently** Fuse conv + includes ~200 rules int64 weights_cols; batch normalization weights cols = (~<u>53,000</u> LOC) 81 } else { 82 83 84 85 86 87 88 Fuse multi. convs 89 91 94 95 96 98 99 100 101 102 103 104 105 106 107 108 109 110 return Status::OK(); return Status::OK(): **Rule-based Optimizer**

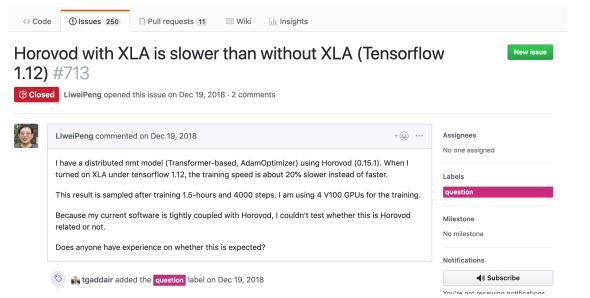
namespace tensorflow { namespace graph_transforms { // Converts Conv2D or MatMul ops followed by column-wise Muls into equivalent // ops with the Mul baked into the convolution weights, to save computation Status FoldBatchNorms(const GraphDef& input_graph_def, const TransformFuncContext& context, GraphDef* output_graph_def) { GraphDef replaced_graph_def; TF_RETURN_IF_ERROR(ReplaceMatchingOpTypes(input_graph_def, // clang-format off
{"Mul", // mul node {"Conv2D|MatMul|DepthwiseConv2dNative", // conv_node // input_node // weights_node // mul_values_node }, // clang-format on
[](const NodeMatch& match, const std::set<string>& input_nodes, const std::set<string>& output_nodes, std::vector<NodeDef>* new_nodes) { // Find all the nodes we expect in the subgraph. const NodeDef& mul_node = match.node; const NodeDef& conv node = match.inputs[0].node; const NodeDef& input_node = match.inputs[0].inputs[0].node; const NodeDef& weights_node = match.inputs[0].inputs[1].node; const NodeDef& mul_values_node = match.inputs[1].node; // Check that nodes that we use are not used somewhere else. for (const auto& node : {conv_node, weights_node, mul_values_node}) { if (output_nodes.count(node.name())) // Return original nodes. new_nodes->insert(new_nodes->end(), {mul_node, conv_node, input_node, weights_node, mul_values_node}); return Status::OK(); Tensor weights = GetNodeTensorAttr(weights_node, "value"); Tensor mul_values = GetNodeTensorAttr(mul_values_node, "value"); // Make sure all the inputs really are vectors, with as many entries as // there are columns in the weights. if (conv_node.op() == "Conv2D") { weights_cols = weights.shape().dim_size(3); } else if (conv_node.op() == "DepthwiseConv2dNative") { weights.shape().dim_size(2) * weights.shape().dim_size(3); weights_cols = weights.shape().dim_size(1); if ((mul_values.shape().dims() != 1) || (mul_values.shape().dim_size(0) != weights_cols)) { return errors::InvalidArgument("Mul constant input to batch norm has bad shape: ". mul_values.shape().DebugString()); // Multiply the original weights by the scale vector. auto weights_vector = weights.flat<float>(); Tensor scaled weights(DT FLOAT, weights.shape()); auto scaled weights vector = scaled weights.flat<float>(); for (int64 row = 0; row < weights_vector.dimension(0); ++row) {</pre> scaled_weights_vector(row) = weights_vector(row) * mul_values.flat<float>()(row % weights_cols); // Construct the new nodes. NodeDef scaled_weights_node; scaled_weights_node.set_op("Const"); scaled_weights_node.set_name(weights_node.name()); SetNodeAttr("dtype", DT_FLOAT, &scaled_weights_node); SetNodeTensorAttr<float>("value", scaled_weights, &scaled_weights_node); new_nodes->push_back(scaled_weights_node); new_nodes->push_back(input_node); NodeDef new_conv_node; new_conv_node = conv_node; new_conv_node.set_name(mul_node.name()); new_nodes->push_back(new_conv_node); {}, &replaced_graph_def)); *output_graph_def = replaced_graph_def; REGISTER_GRAPH_TRANSFORM("fold_batch_norms", FoldBatchNorms); // namespace graph transforms

// namespace tensorflow

Limitations of Rule-based Optimizations

Robustness

Experts' heuristics do not apply to all models/hardware



When I turned on XLA (TensorFlow's graph optimizer), the training speed is about 20% slower

🖄 stack overflow	Search
Home	Tensorflow XLA makes it slower?
PUBLIC	
Stack Overflow	I am writing a very simple tensorflow program with XLA enabled. Basically it's something like:
Tags	1 import tensorflow as tf
Users Jobs	<pre>def ChainSoftMax(x, n) tensor = tf.nn.softmax(x) for i in range(n-1):</pre>
	<pre>tensor = tf.nn.softmax(tensor) return tensor</pre>
Teams Q&A for work	<pre>config = tf.ConfigProto() config.graph_options.optimizer_options.global_jit_level = tf.OptimizerOptions.ON_1</pre>
Learn More	<pre>input = tf.placeholder(tf.float32, [1000]) feed = np.random.rand(1000).astype('float32')</pre>
	<pre>with tf.Session(config=config) as sess: res = sess.run(ChainSoftMax(input, 2000), feed_dict={input: feed})</pre>
	Basically the idea is to see whether XLA can fuse the chain of softmax together to avoid multiple kernel launches. With XLA on, the above program is almost 2x slower than that without XLA on a machine with a GPU card. In my gpu profile, I saw XLA produces lots of kernels named as "reduce_xxx" and "fusion_xxx" which seem to overwhelm the overall runtime. Any one know what happened here?

With XLA, my program is almost 2x slower than without XLA

Limitations of Rule-based Optimizations

Robustness

Experts' heuristics do not apply to all models/hardware

Scalability

New operators and graph structures require more rules

TensorFlow currently uses ~4K LOC to optimize convolution

Limitations of Rule-based Optimizations

Robustness

Experts' heuristics do not apply to all models/hardware

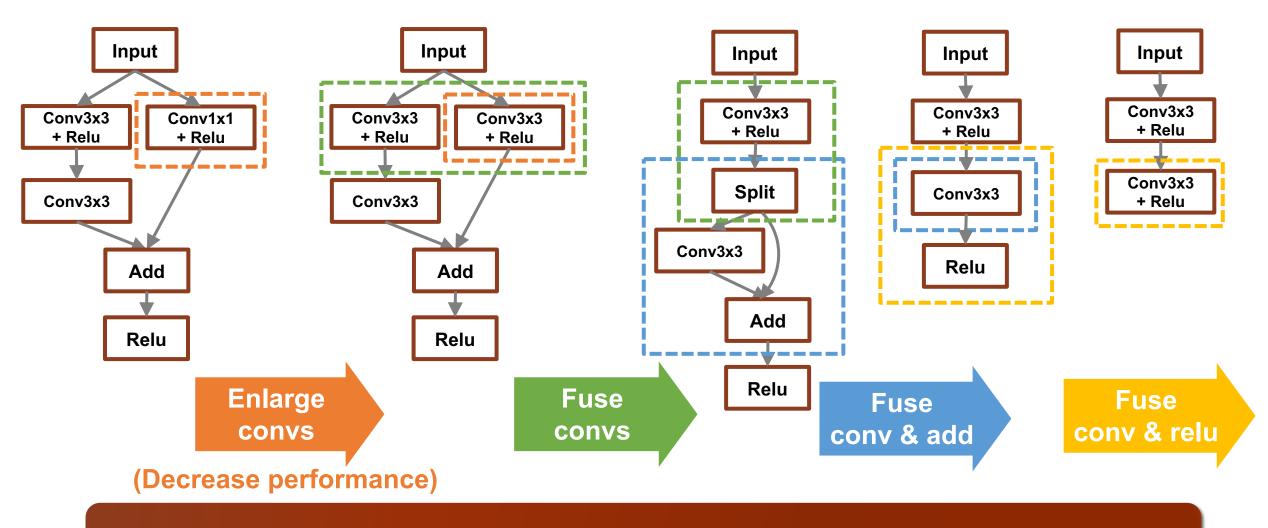
Scalability

New operators and graph structures require more rules

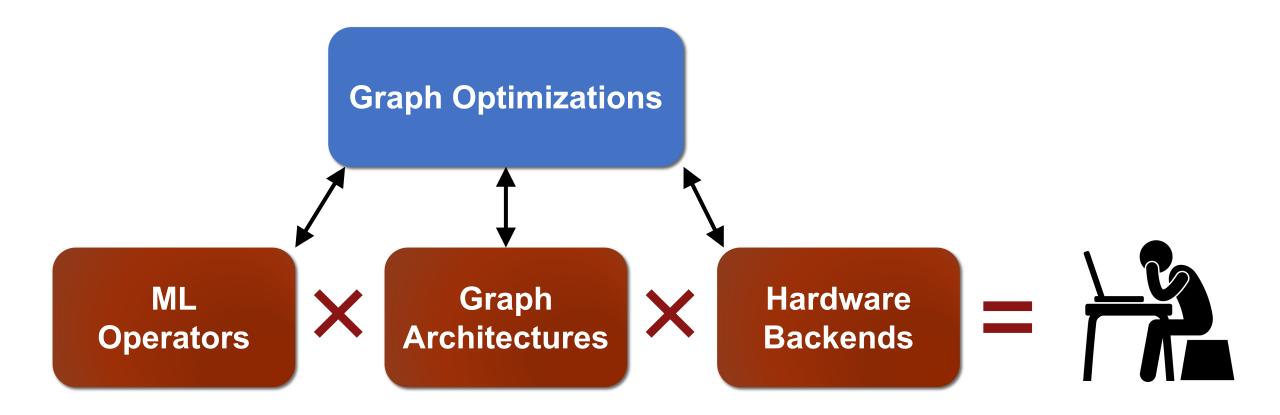
Performance

Miss subtle optimizations for specific models/hardware

Motivating Example (ResNet)



The final graph is <u>30% faster</u> on V100 but <u>10% slower</u> on K80.



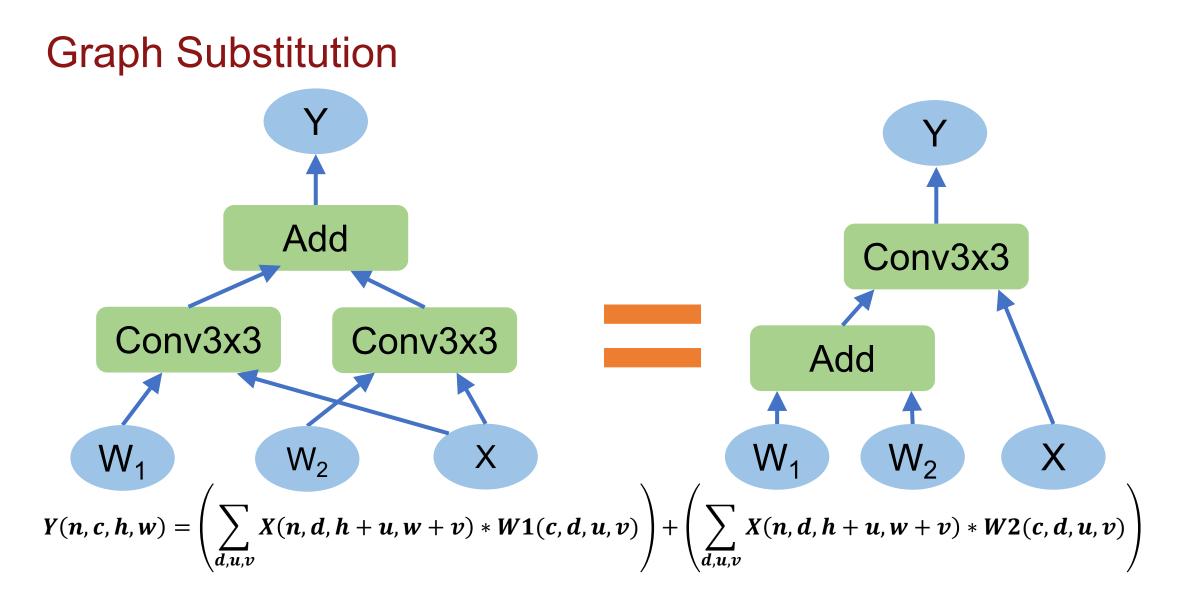
Infeasible to manually design graph optimizations for all cases

Is it possible to generate them automatically?

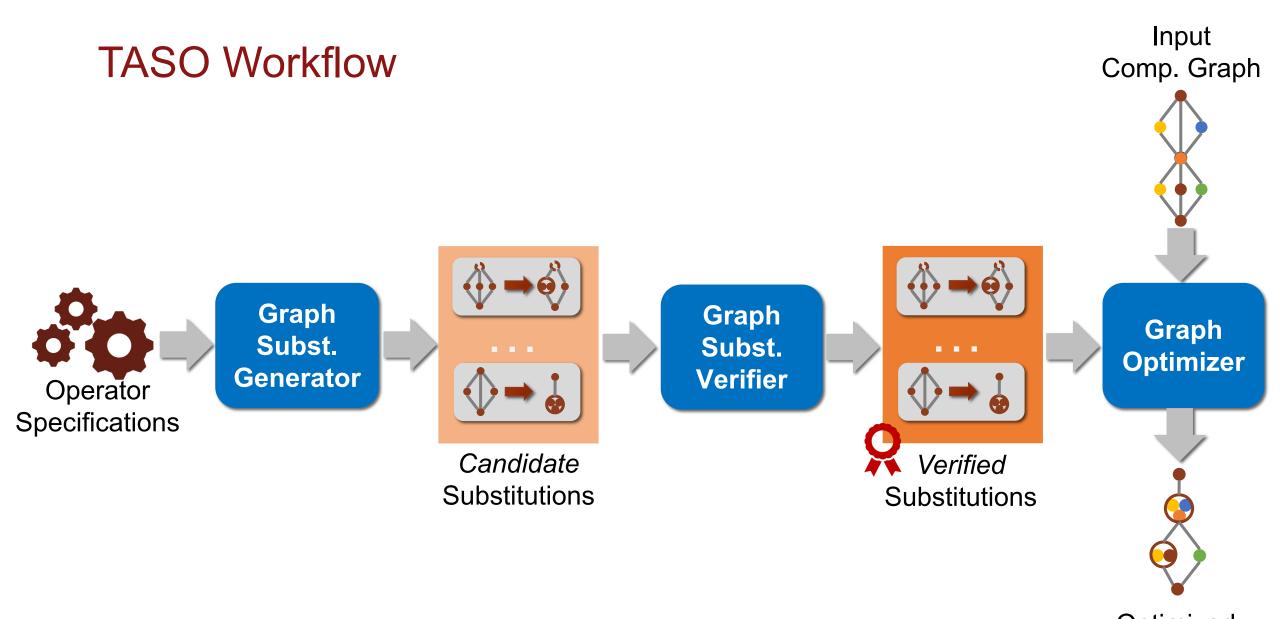
TASO: Tensor Algebra SuperOptimizer

Key idea: replace manually-designed graph optimizations with *automated generation and verification* of graph substitutions for tensor algebra

- Less engineering effort: <u>53,000</u> LOC for manual graph optimizations in TensorFlow $\rightarrow 1,400$ LOC in TASO
- Better performance: outperform existing optimizers by up to 3x
- Stronger correctness: formally verify all generated substitutions



$$\Leftrightarrow Y(n,c,h,w) = \sum_{d,u,v} X(n,d,h+u,w+v) * \left((W_1(c,d,u,v) + W_2(c,d,u,v)) \right)$$



Optimized Comp. Graph 21



1. How to generate potential substitutions?

Graph fingerprints

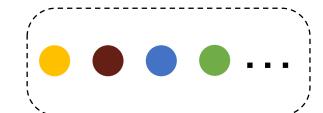
2. How to verify their correctness?

Operator specifications + theorem prover

Graph Substitution Generator



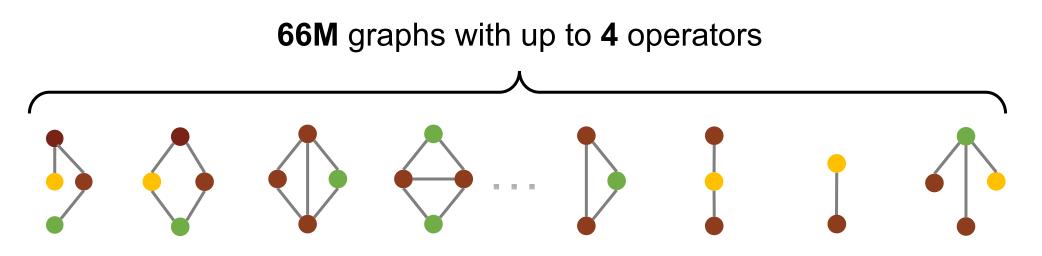
Enumerate <u>all possible</u> graphs up to a fixed size using available operators



Operators supported by hardware backend



Graph Substitution Generator

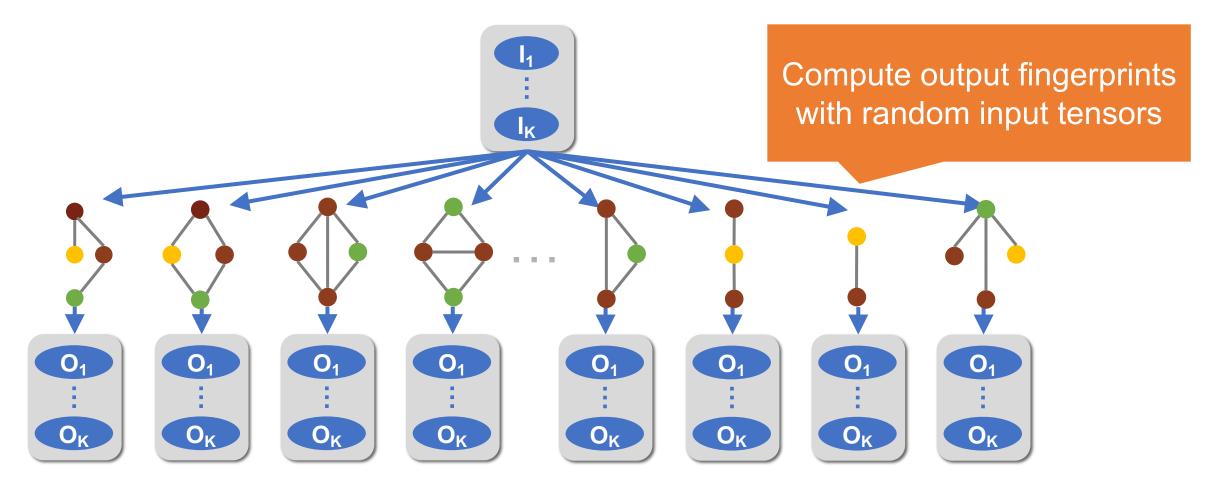


A substitution = a pair of equivalent graphs

Explicitly considering all pairs does not scale

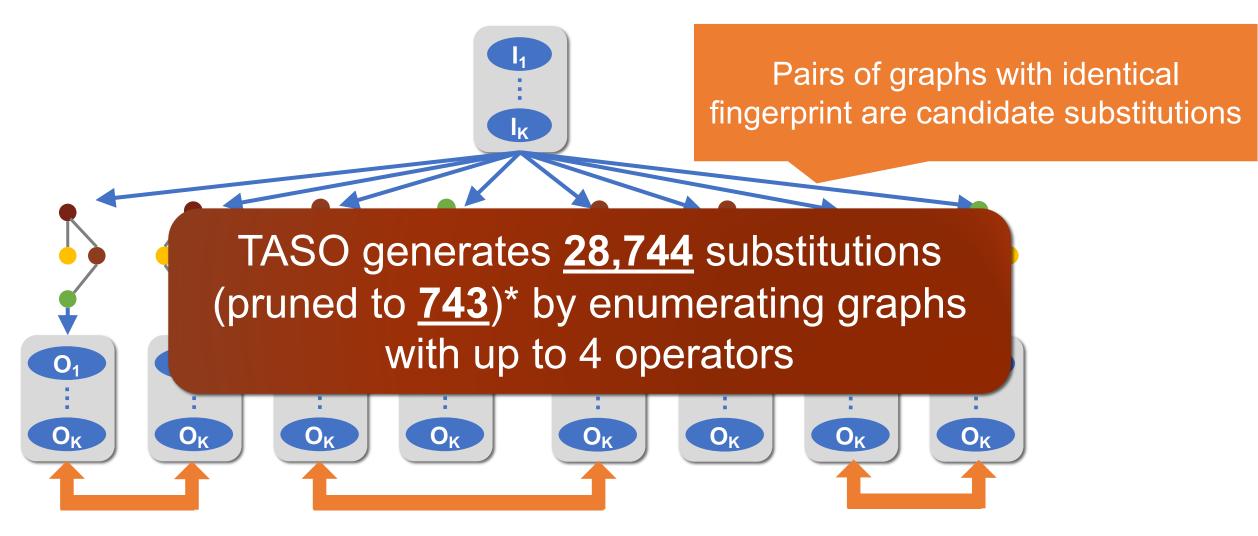
Graph Substitution Generator







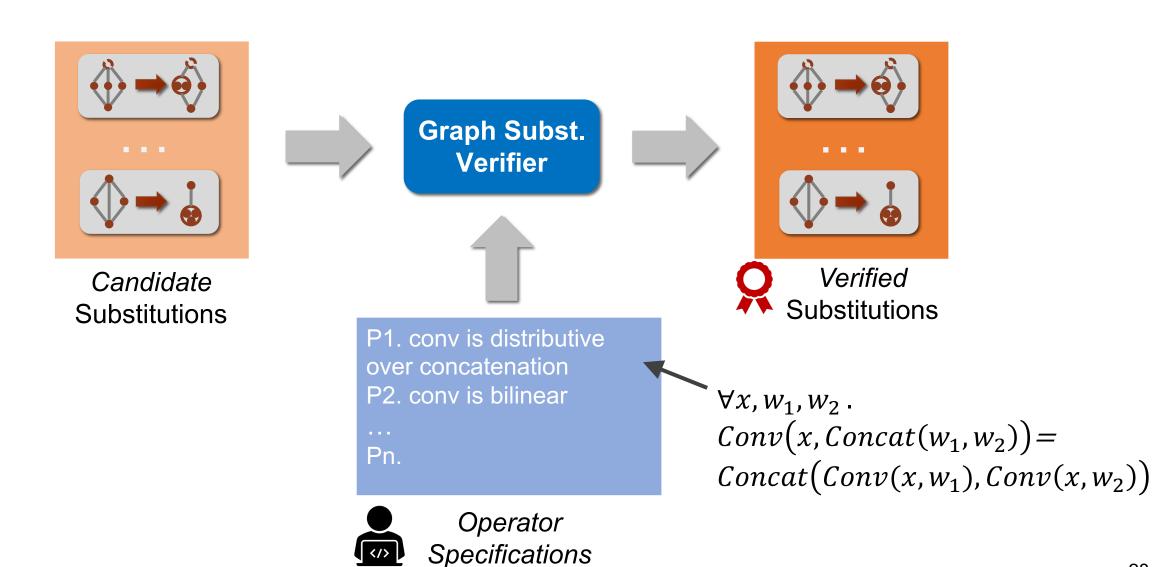




*Pruning details available in Z. Jia et al. SOSP'19



Graph Substitution Verifier

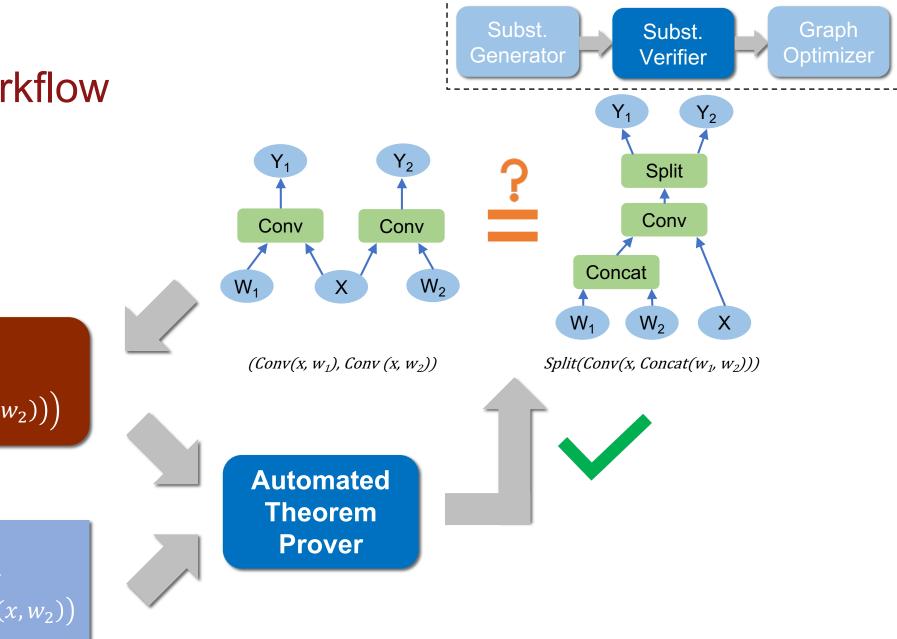


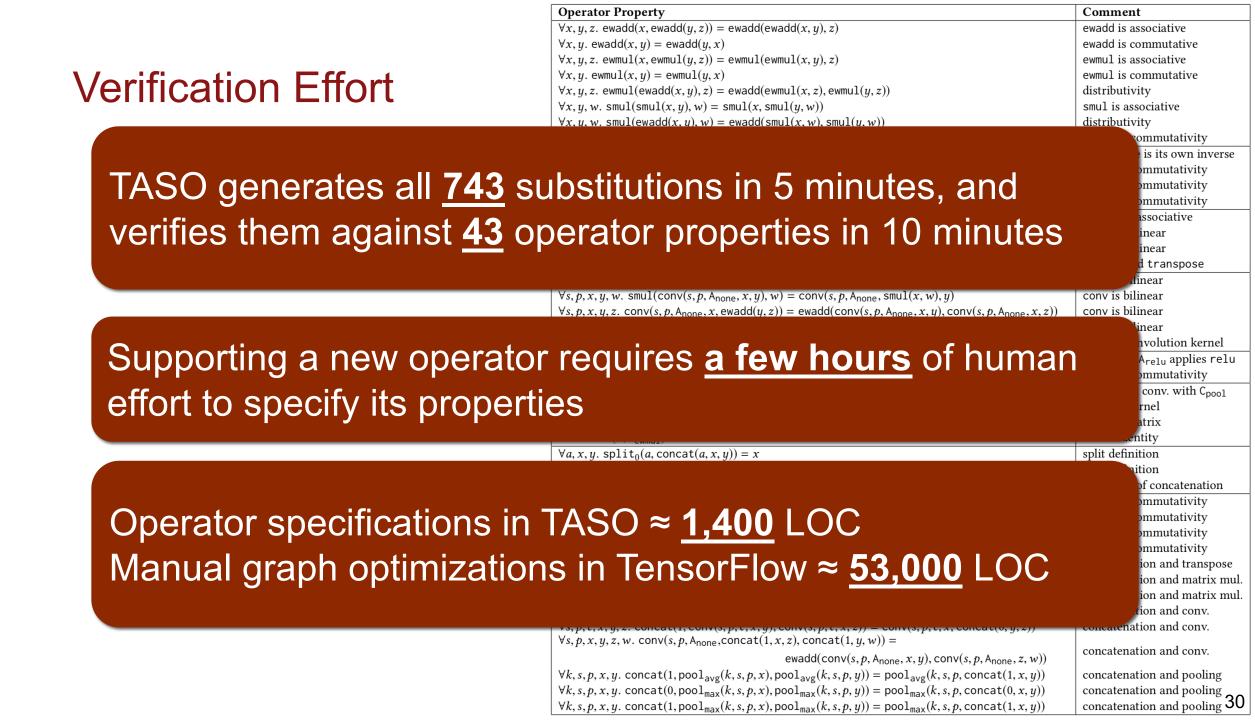
Verification Workflow

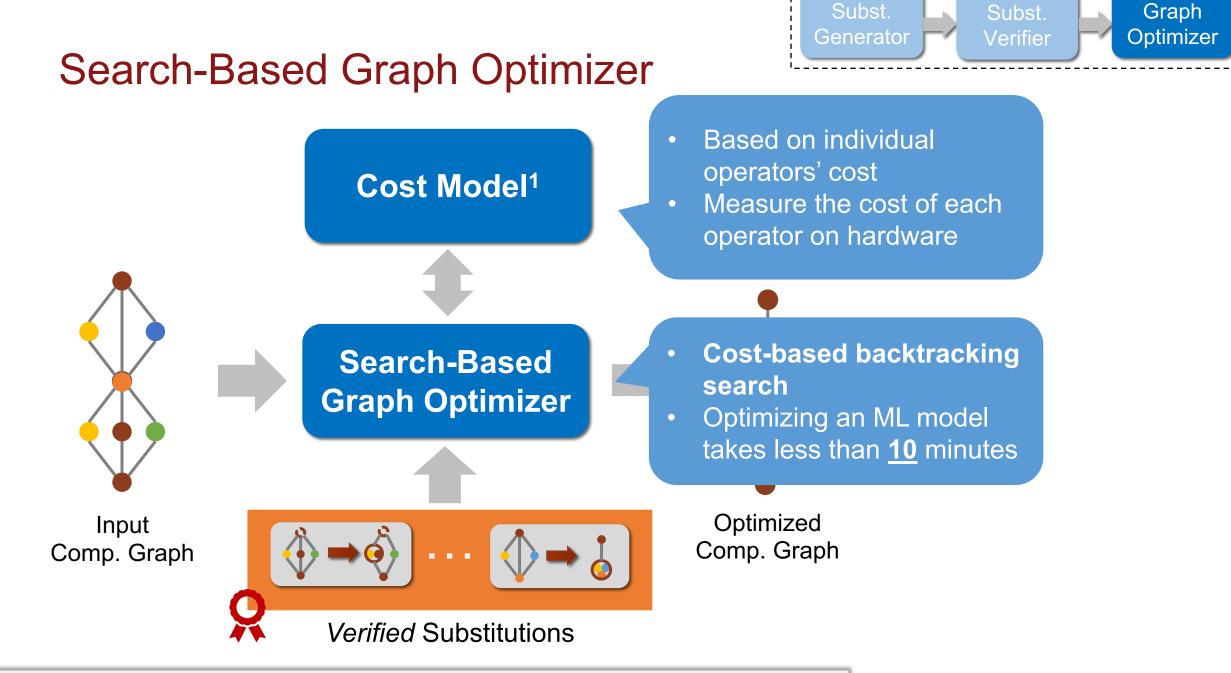
 $\begin{aligned} \forall x, w_1, w_2 . \\ & \left(Conv(x, w_1), Conv(x, w_2) \right) \\ &= Split \left(Conv(x, Concat(w_1, w_2)) \right) \end{aligned}$

P1. $\forall x, w_1, w_2$. $Conv(x, Concat(w_1, w_2)) =$ $Concat(Conv(x, w_1), Conv(x, w_2))$ P2. ...

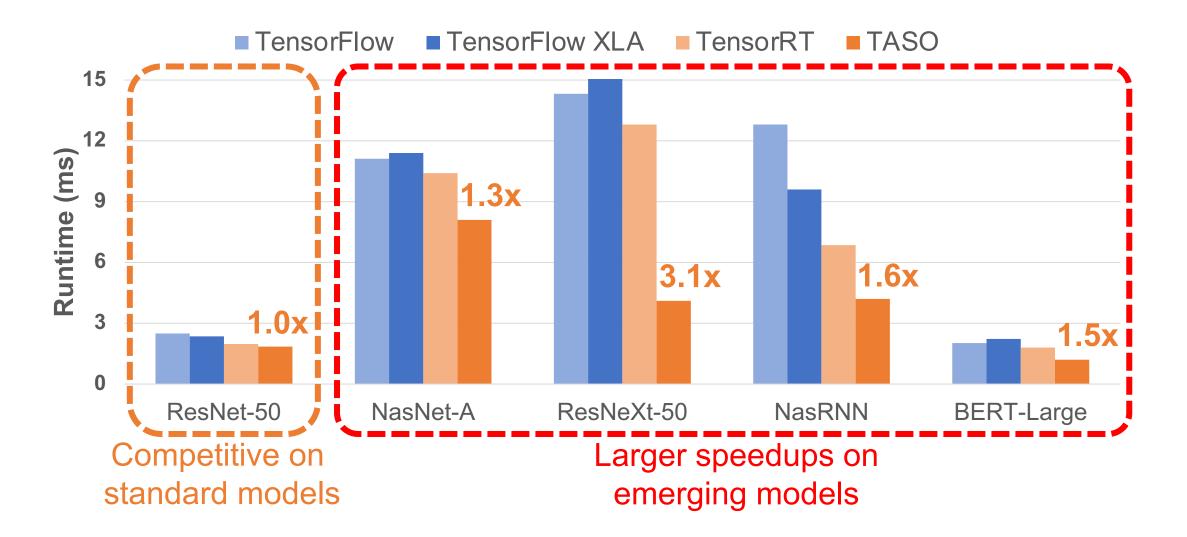
Operator Specifications







End-to-end Inference Performance (Nvidia V100 GPU)





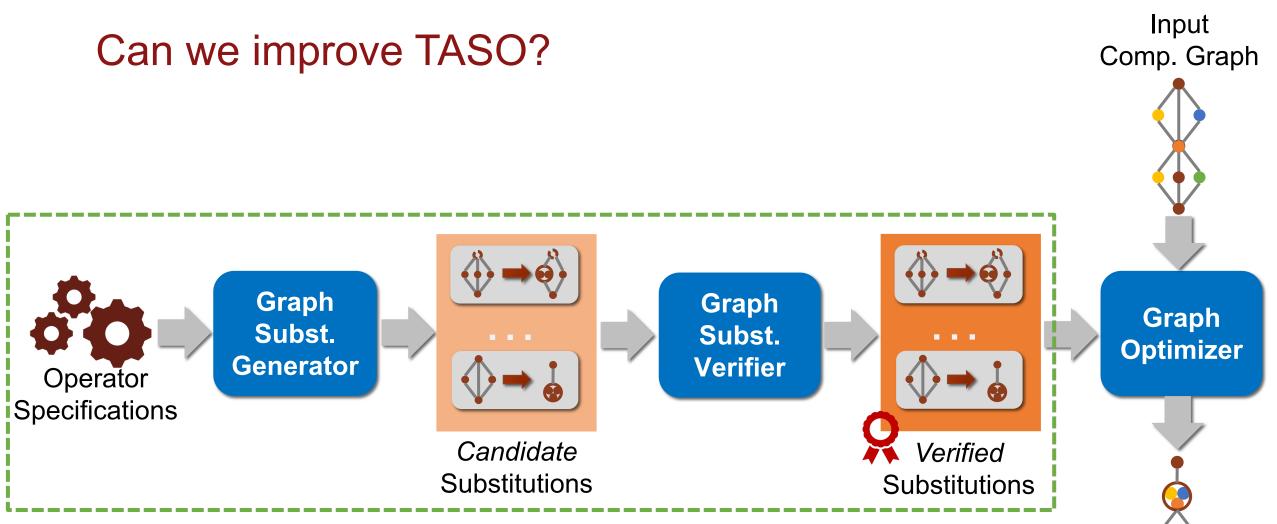


First DNN graph optimizer that automatically generates substitutions

- Less engineering effort
- Better runtime performance
- Stronger correctness guarantee



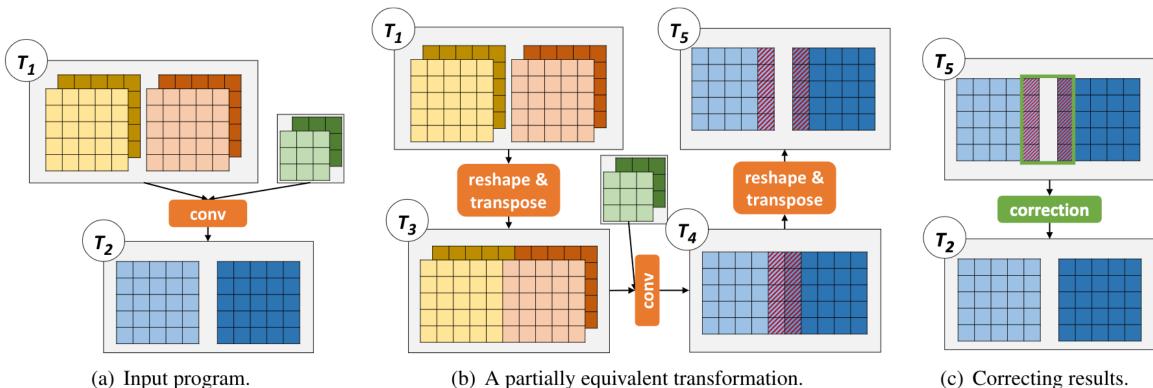
- 1. TASO: Optimizing Deep Learning Computation with Automated Generation of Graph Substitutions. SOSP'19.
- 2. Optimizing DNN Computation with Relaxed Graph Substitutions. MLSys'19.
- 3. Exploring Hidden Dimensions in Parallelizing Convolutional Neural Networks. ICML'18.



TASO only discovers fully equivalent substs. Can we use substs that are partially equivalent and correct the results afterwards?

Optimized Comp. Graph

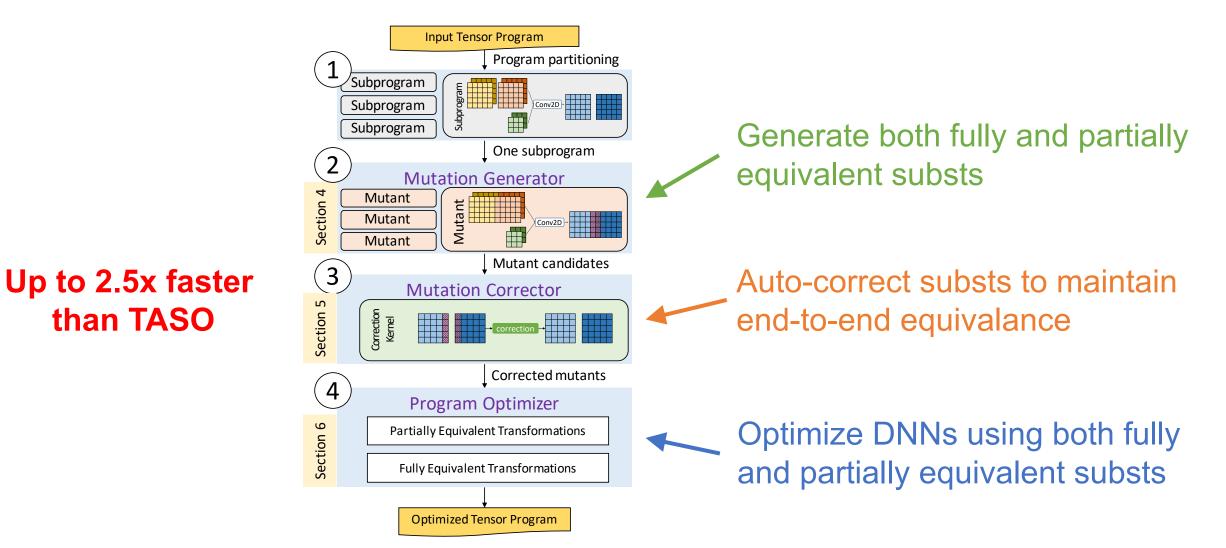
Motivating Example: Partially Equivalent Substs



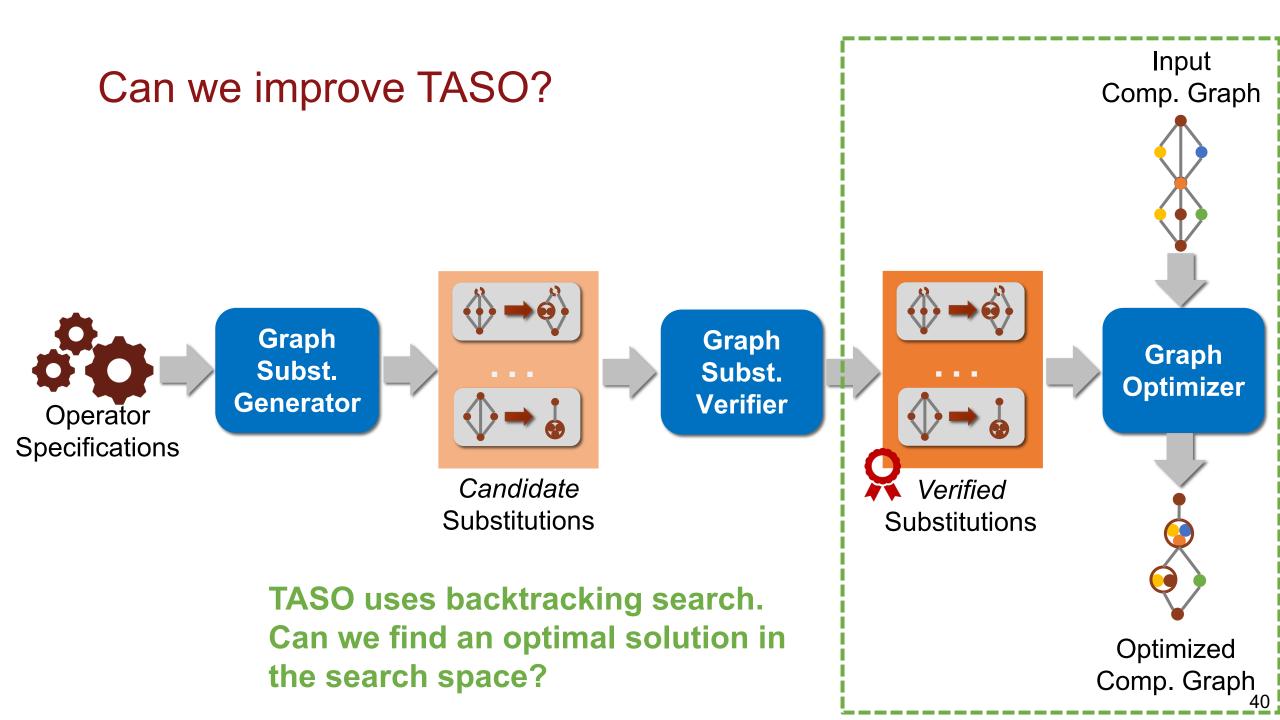
(b) A partially equivalent transformation.

(c) Correcting results.

PET: Partially Equivalent Substs and Auto Corrections

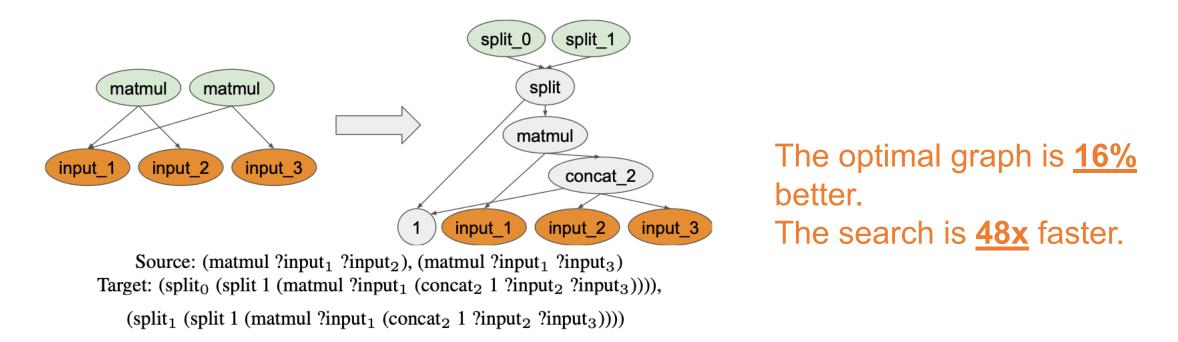


Optimizing Tensor Programs with Partially Equivalent Transformations and Automated Corrections. H. Wang et al. 38



Equality Saturation for TASO

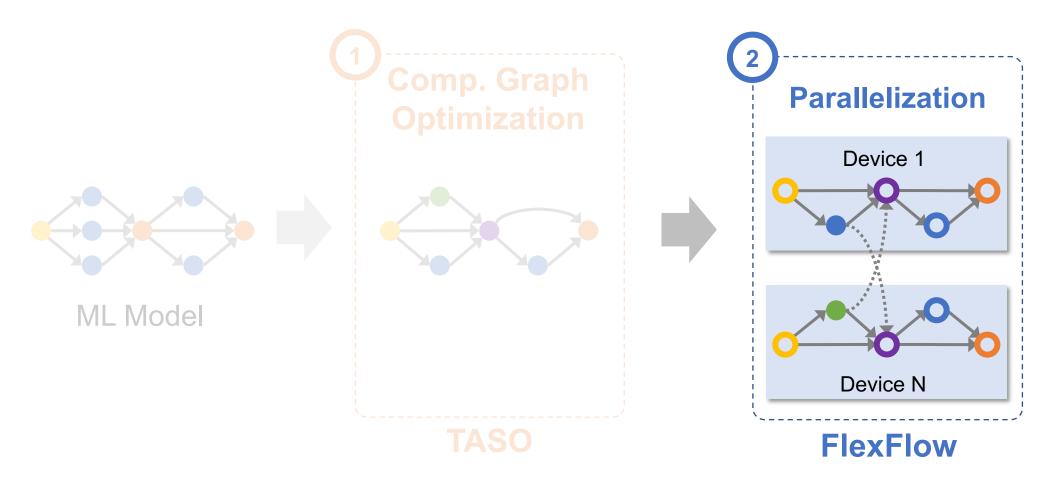
 Key idea: a new representation that can express all possible computation graphs at once



Can we apply TASO to other problem domains?

- Cross-optimizations between ML and DB operations
 - Why: ML and DB operations are optimized separately in today's DB systems
 - How: automatically generate co-optimizations of linear algebra and relational algebra operations
- Optimizing Compilers for Quantum Computing
 - Why: today's quantum machines support different sets of instructions -> impossible to manually design optimizations for all quantum architectures
 - How: automatically generate quantum program transformations given a set
 of instructions
- Others?

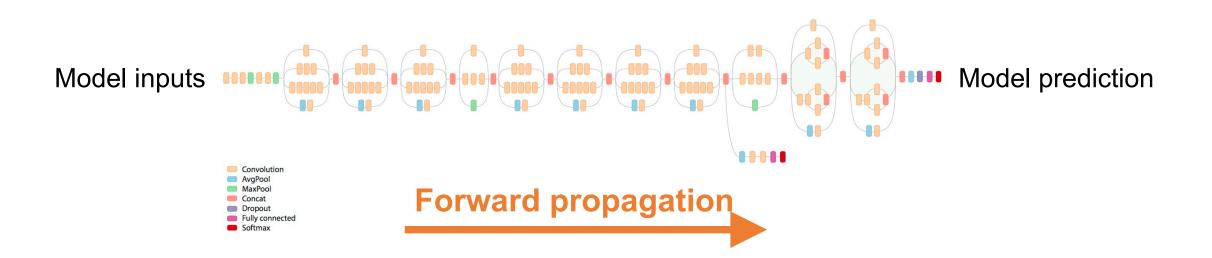
Automated Discovery of ML Optimizations



Stochastic Gradient Descent (SGD)

Train ML models through many iterations of 3 stages

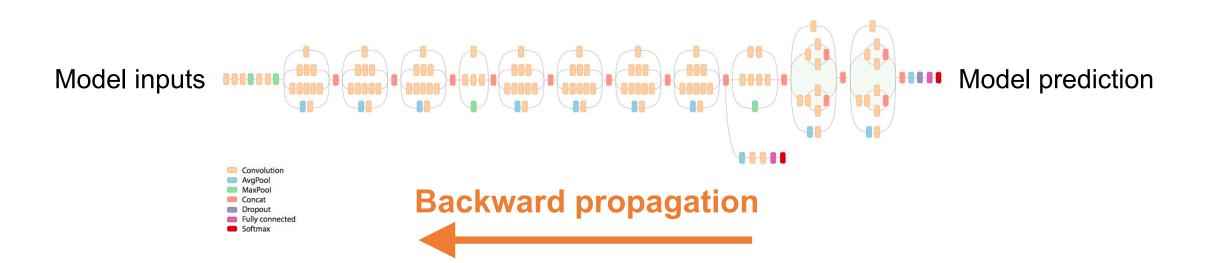
- 1. Forward propagation: apply model to a batch of input samples and run calculation through operators to produce a prediction
- 2. Backward propagation: run the model in reverse to produce error for each trainable weight
- 3. Weight update: use the loss value to update model weights



Stochastic Gradient Descent (SGD)

Train ML models through many iterations of 3 stages

- 1. Forward propagation: apply model to a batch of input samples and run calculation through operators to produce a prediction
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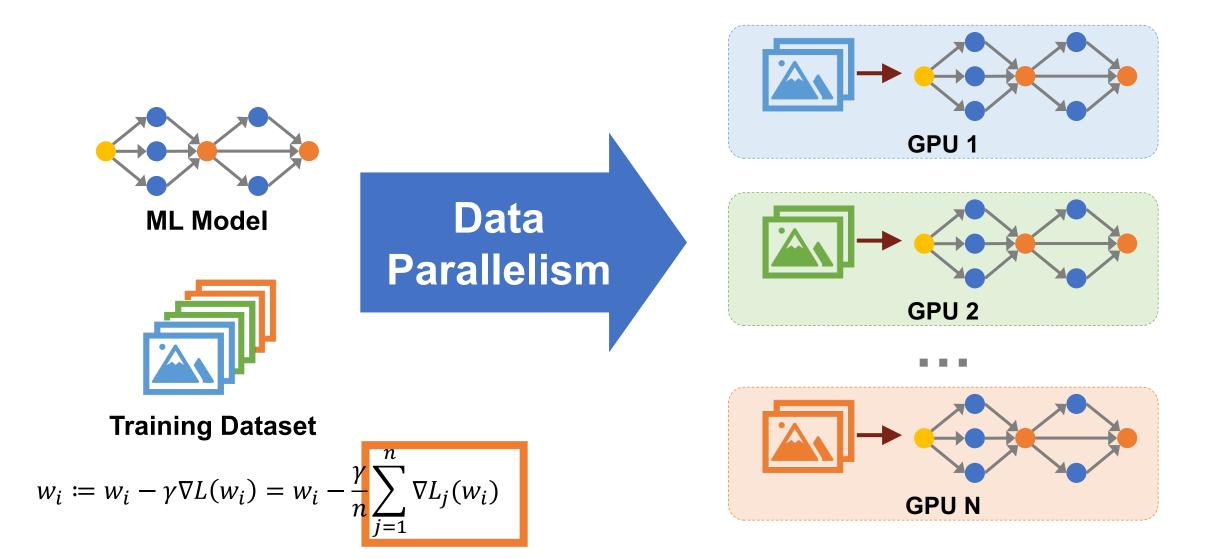
Stochastic Gradient Descent (SGD)

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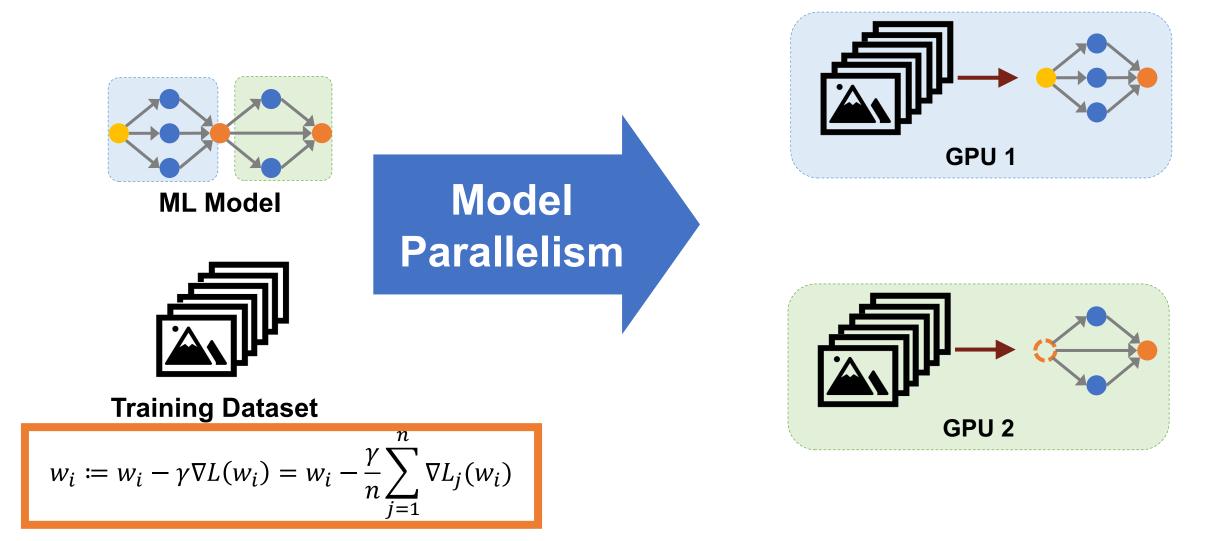
- 1. Forward propagation: apply model to a batch of input samples and run calculation through operators to produce a prediction
- 2. Backward propagation: run the model in reverse to produce error for each trainable weight
- 3. Weight update: use the loss value to update model weights

$$w_i \coloneqq w_i - \gamma \nabla L(w_i) = w_i - \frac{\gamma}{n} \sum_{j=1}^n \nabla L_j(w_i)$$

Current Strategies to Parallelize ML Training: Data and Model Parallelism



Current Strategies to Parallelize ML Training: Data and Model Parallelism



Are there strategies beyond data/model parallelism? Can we discover fast ones automatically?

FlexFlow: Automated Search for Fast Strategies

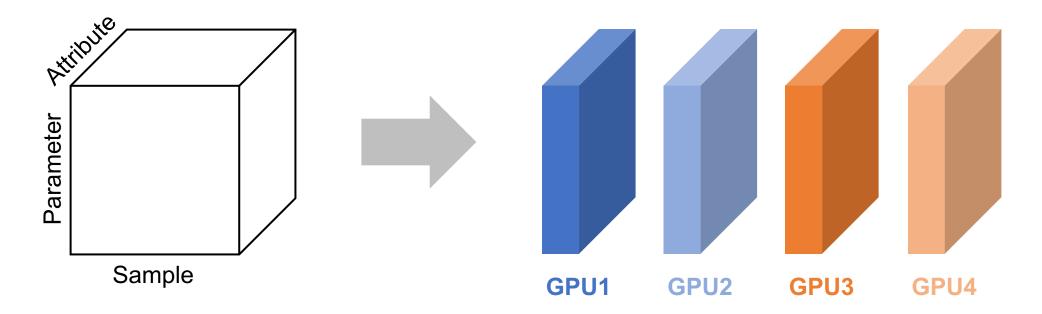
Define a **search space** of possible parallelization strategies

A cost model and a search algorithm

Optimized Parallelization strategies

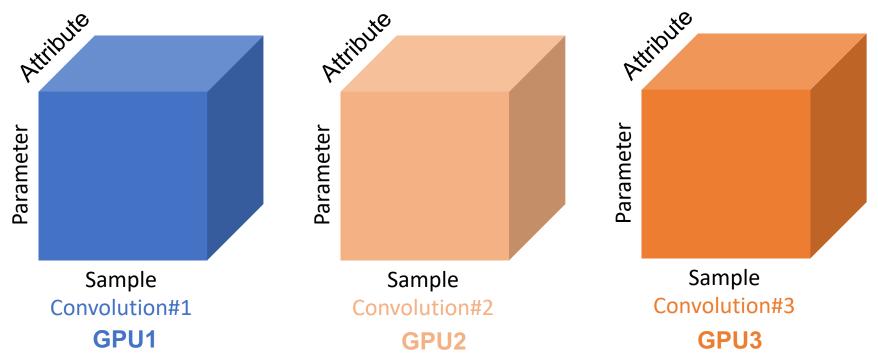
- Samples
- Operators
- Attributes
- Parameters

- Samples: partitioning training samples (Data Parallelism)
- Operators
- Attributes
- Parameters



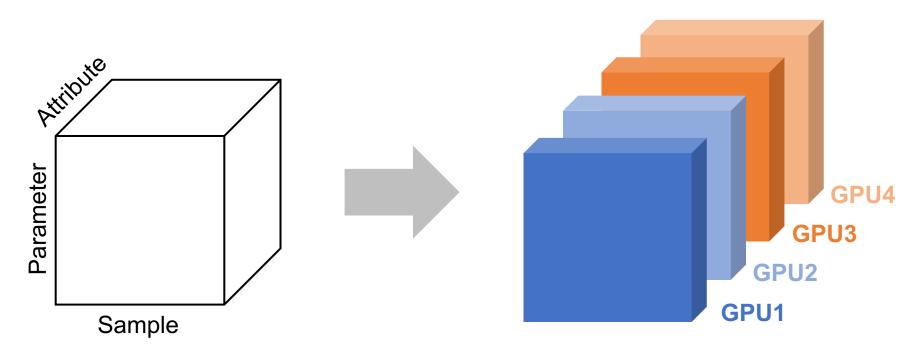
Parallelizing a 1D convolution in **Sample**

- Samples: partitioning training samples (Data Parallelism)
- Operators: partitioning ML operators (Model Parallelism)
- Attributes
- Parameters



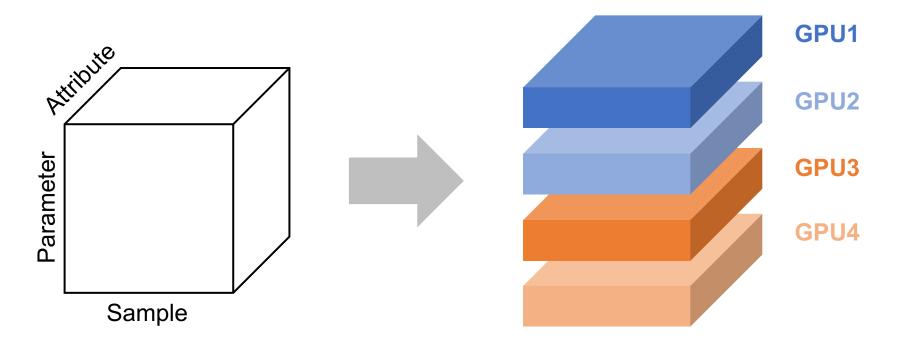
Parallelizing multiple convolutions in *Operator*

- Samples: partitioning training samples (Data Parallelism)
- Operators: partitioning ML operators (Model Parallelism)
- Attributes: partitioning attributes in a sample (e.g., pixels)
- Parameters



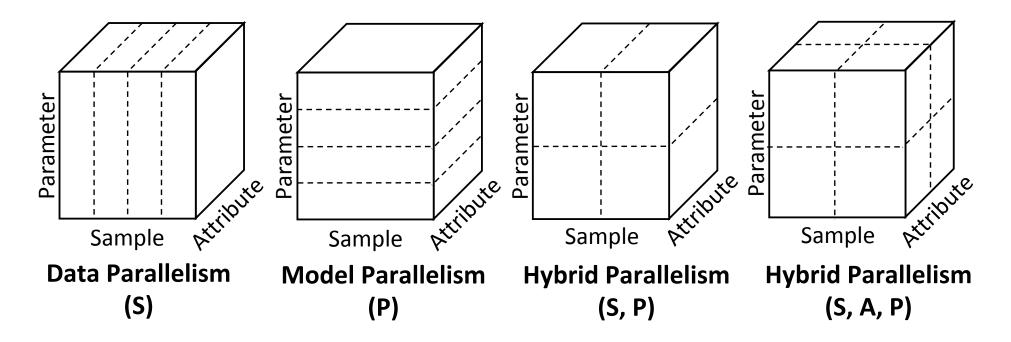
Parallelizing a 1D convolution in Attribute

- Samples: partitioning training samples (Data Parallelism)
- Operators: partitioning ML operators (Model Parallelism)
- Attributes: partitioning attributes in a sample (e.g., pixels)
- Parameters: partitioning parameters in an operator



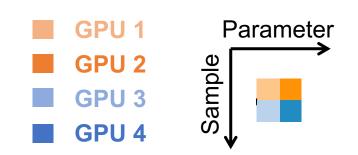
Parallelizing a 1D convolution in *Parameter*

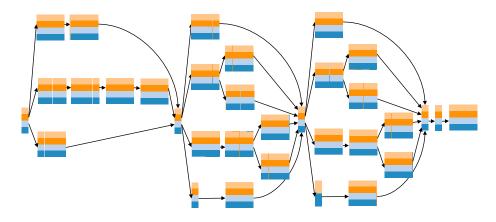
Hybrid Parallelism in SOAP



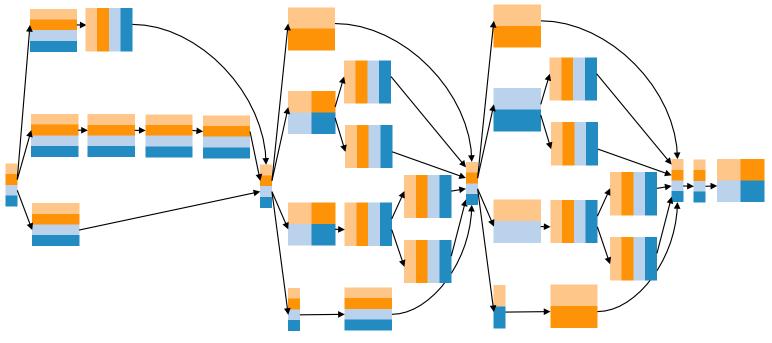
Example parallelization strategies for 1D convolution

Different strategies perform the same computation.

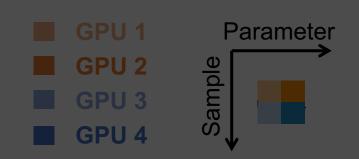


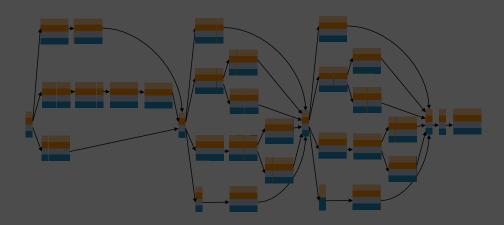


Data parallelism

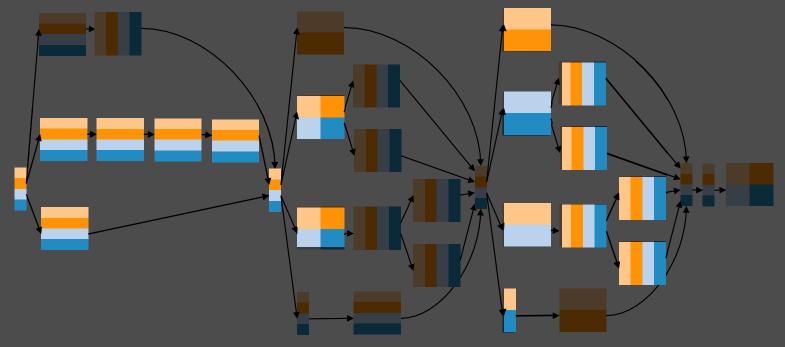


A parallelization strategy in SOAP (1.2x faster)





Data parallelism



A parallelization strategy in SOAP (1.2x faster)

Challenges of Discovering Fast Strategies in SOAP

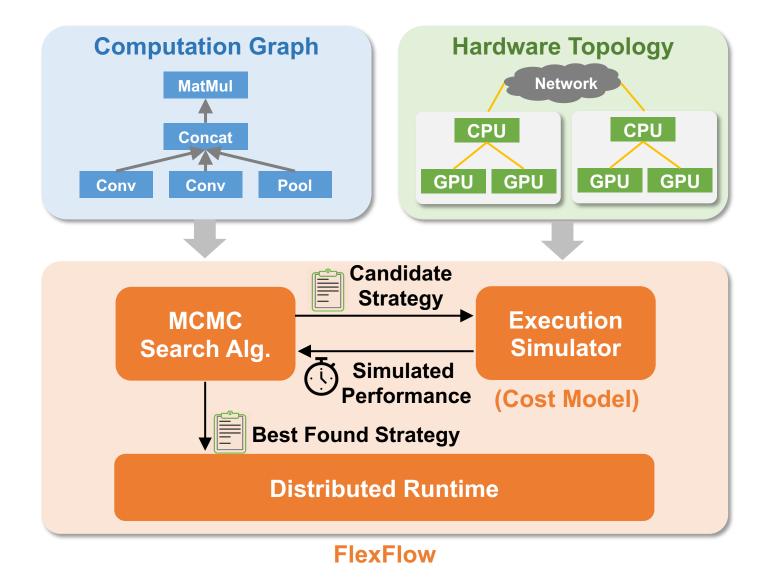
1. SOAP contains billions or more possible strategies

MCMC search algorithm

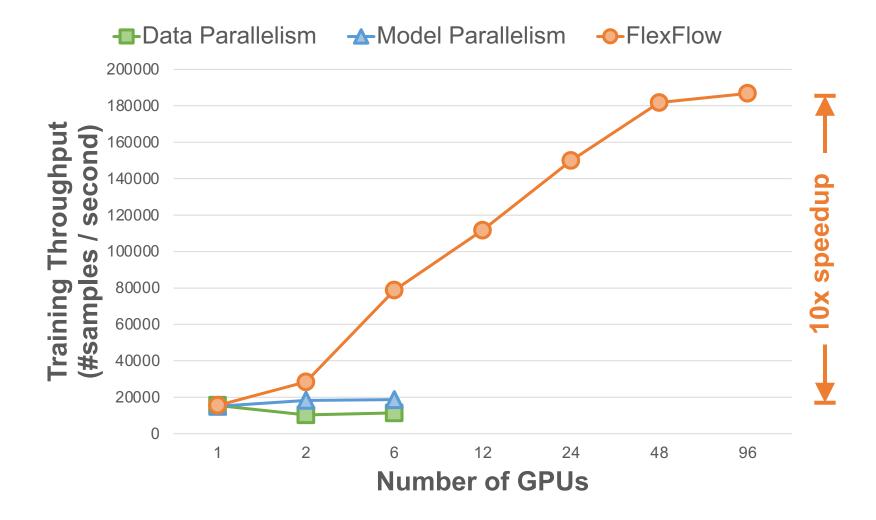
2. Evaluating a strategy on hardware is too slow

Execution simulator

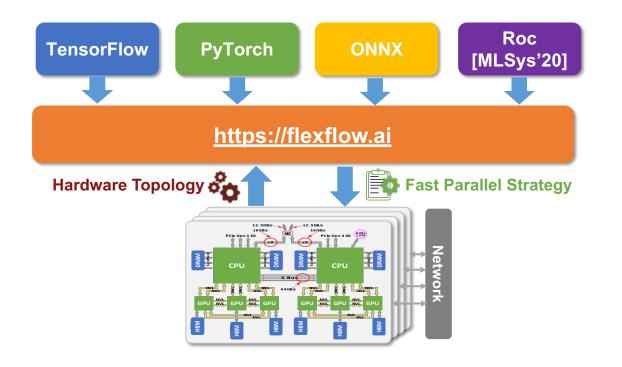
FlexFlow Overview



Deep Learning Recommendation Model (DLRM) **facebook** A deep learning model for ads recommendation



FlexFlow: Automatically Discover Fast Parallelization for DNNs



https://flexflow.ai



Performance Autotuning

Learn more

FlexFlow accelerates DNN training by automatically discovering fast parallelization strategies for a specific parallel machine.

Keras Support

FlexFlow provides a drop-in replacement for TensorFlow Keras and requires only a few lines of changes to existing Keras programs.

Learn more

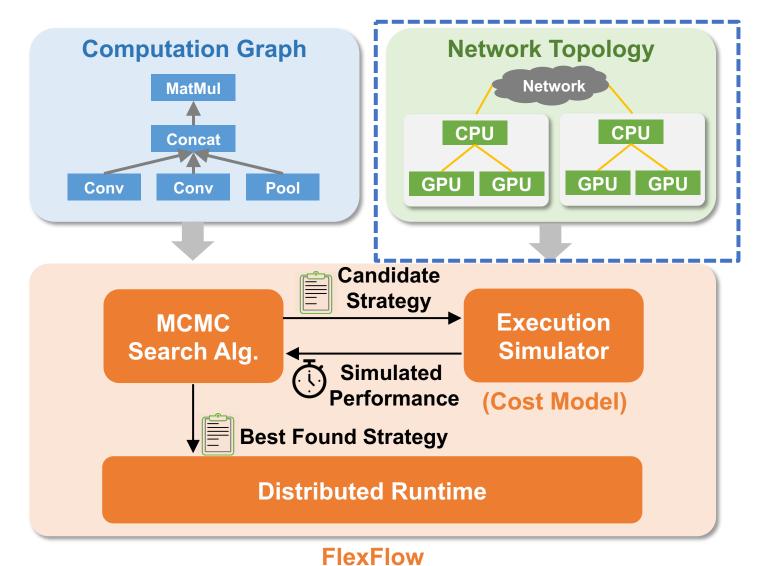


FlexFlow enables fast graph neural network training and inference on large-scale graphs by exploring attribute parallelism.

Learn more



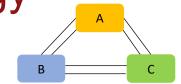
Can we improve FlexFlow?

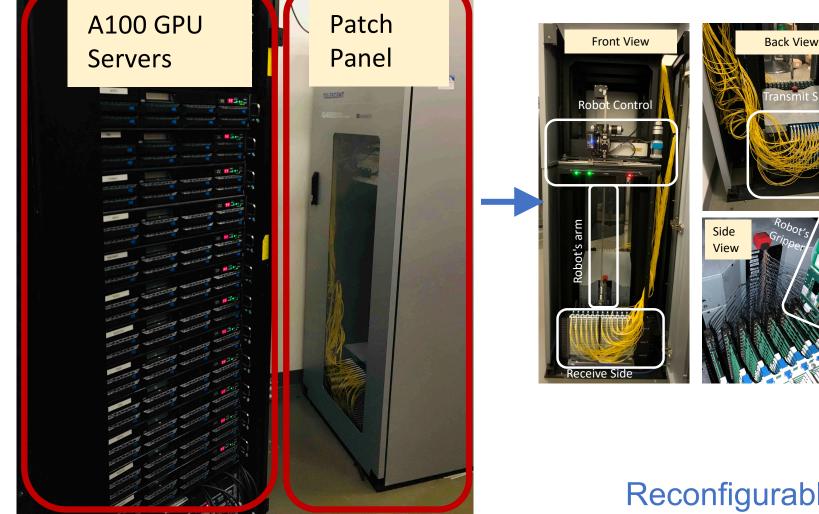


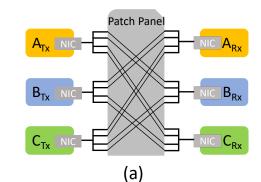
FlexFlow takes network topology as an input.

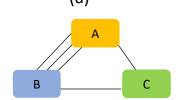
Can we co-optimize network topology and parallelization strategies?

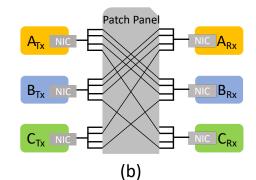
Testbed with Reconfigurable Network Topology





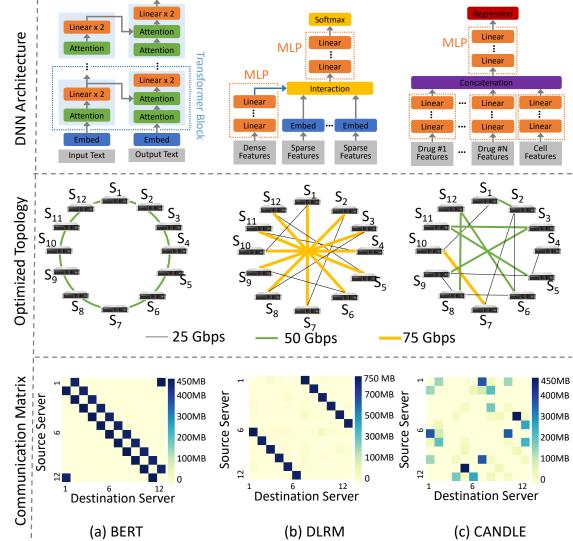






Reconfigurable network topology

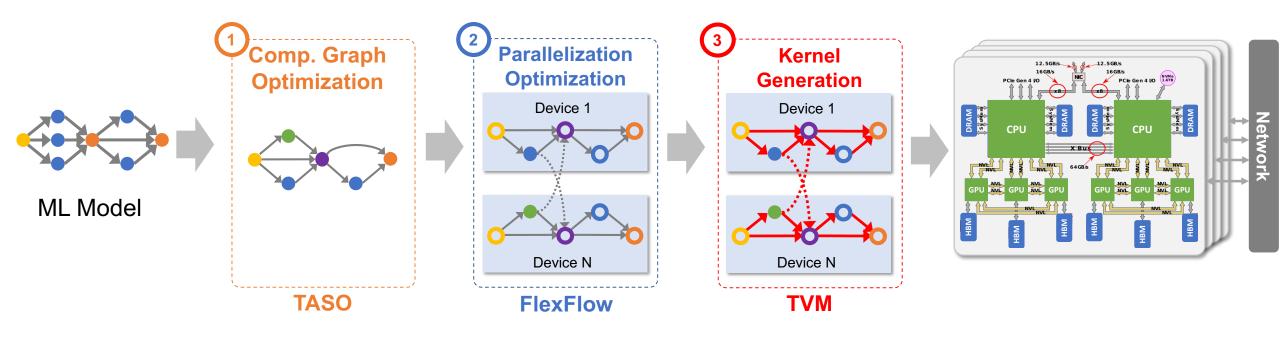
Joint Optimization of Parallelization Strategy and Network Topology



Up to 5.7x faster than FlexFlow w/ Fat-tree interconnect

Optimizing the Network Topology for Distributed DNN Training. W. Wang et al.

Automated Machine Learning Systems



catalyst

https://catalyst.cs.cmu.edu/