

## EE180 Digital Systems Architecture Course Information

<http://ee180.stanford.edu>

Lectures:

Monday & Wednesday      3:00 PM – 4:20 PM      [STLC 111](#)

Review Sessions:

Friday      3:00 PM – 4:00 PM      [Hewlett 102](#)

Instructors:

Christos Kozyrakis

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Office Hours: Monday 4:30 PM – 5:30 PM or by appointment, [Gates 444](#)

Teaching Assistants:

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Office Hours: Check webpage

Course Support:

Julie Hitchcock

Email: [julieh1@stanford.edu](mailto:julieh1@stanford.edu)

**\*\* Handouts are available in digital form on the class webpage\*\***

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- Units:** This class is offered for 4 units as either a letter grade or a S/NC course. Please check your degree requirements before you select a grading option.
- Prerequisites:** The prerequisites for EE180 are CS107/CS107E (Computer Organization & Systems) and EE108 (Digital Systems Design). Both prerequisites can be waived assuming you have a good background on programming with C or C++ or Java (CS107) and basic digital design (EE108). Appendix B of the Computer Organization and Design textbook covers all the logic design material needed for this class. We will teach you the small subset of Verilog necessary for some laboratory assignments. If you are uncertain about prerequisites, check with the instructors.
- Website:** The class website is located at:  
<https://ee180.stanford.edu>  
All important class information including lecture notes, homework assignments and solutions, and past exams will be posted to this site or the [Canvas class portal](#). **Check the website frequently** since new information and announcements will be added regularly. We will use [EdStem](#) for Q&A on all class material. If you are registered with the class on Axess, you will automatically get access to Canvas, EdStem, and Gradescope.
- Mailing List:** A class mailing list will also be used for important or late-breaking announcements. The mailing list is auto-populated from Axess, so make sure you are registered for the class.
- Textbook:** The required text for this course is [Computer Organization & Design: The Hardware/Software Interface](#), David A. Patterson and John L. Hennessy, 6We MIPS Edition, Morgan-Kaufmann, 2020 (ISBN 978-0128201091 for printed book, also available in eBook). The book is available at the Stanford Bookstore and one copy is on reserve at the Engineering Library. The book is also available in print or digital form by online retailers.
- Lectures:** All lectures this quarter will be in person. We strongly encourage you to come to lectures, ask questions, and contribute to the in-class discussion. This is how you will get the most of this class. To encourage attendance, we will give in-class quizzes which will count towards your participation points in the class. We will use Poll Everywhere to facilitate in-class quizzes.
- Homework:** There will be three homework sets during the quarter. Solving the homework is critical to learning the material and understanding the concepts presented in this course. Since there is often a significant benefit to teamwork, we recommend groups of **2 students**. A single copy of the answers should be submitted with all students' names. If necessary, we will allow students to submit individual assignments, but please check with us first. Homework assignments are due at 11.59pm on the announced due date. We will use [gradescope](#) for electronic submission. Do not email your homework to the TAs or the instructors unless asked.
- Accessible Education:** Students who may need an academic accommodation based on the impact of a disability must initiate the request with the [Office of Accessible Education \(OAE\)](#). Professional staff will evaluate the request with required documentation, recommend reasonable accommodations, and prepare an Accommodation Letter for faculty dated in the current quarter in which the request is being made. Students should contact the OAE as soon as possible since timely

notice is needed to coordinate accommodations.

**Laboratory Assignments:** There will be four laboratory assignments. Due to limited FPGA resources, we require that you work in groups of **2 students**. For some labs, we will pair groups to share an FPGA board. You can work on your assignments with remote access to the FPGA boards or you can use them directly at Packard Hall room 052. A short, written report (roughly 3 pages) is required for each assignment. Submissions are due by 11:59 P.M. on the announced due date. We will use [gradescope](#) for submission.

**Late Policy** Late assignments will not be accepted. If you are sick or have another legitimate issue, contact us as soon as possible to make proper arrangements.

**Exams:** There will be one midterm exam and one final exam at the end of the quarter. The midterm *may be* in the form of an online quiz. The exam will be held in person and it will be a closed book exam. Details about the exams will be announced later on.

**Review Session:** The TAs will hold review sessions on most Fridays. These sessions will clarify topics covered during lecture, introduction to homework and laboratory assignments, and review special topics. Attendance is optional, but highly recommended.

**Honor Code:** The Honor Code is taken seriously in this course and suspected violations will be referred to the Office of Community Standards. Please refer to the honor code webpage at <https://communitystandards.stanford.edu/policies-guidance/honor-code>. We use automatic tools to detect plagiarism in programming and lab assignments.

You are encouraged to discuss the assignment, algorithms, tricky conditions, testing strategies, etc. with other students. However, each group must independently write its own solution to homework or laboratory assignments. Submitting solutions or code written by another person is a violation of the Honor Code.

**AI Policy:** We encourage the use of AI tools in the class. Examples of good uses of AI are the following: use AI for further Q&A on lecture or reading material and to help learn and use the tools needed for various assignments. We require students to report AI tool use in the class in assignments. We will also collect and share best practices in AI uses to improve learning.

We will follow [guidance from the Board of Judicial Affairs](#) regarding use of AI and the Stanford Honor Code, which notes that use of generative AI to “substantially complete” an assignment by entering the prompt and submitting the output as one’s own work is not permitted. Students should acknowledge the use of generative AI and default to disclosing such assistance when in doubt.

**Grading:** Final grades will be computed approximately as follows:

Homework:	10 %
Lab Assignments:	35 %
Midterm exam:	15 %
Final exam:	35 %
Class participation	5%

**Tentative Course Schedule**  
**All lectures take place on 1:30 PM – 2:50 PM at STLC111**

Date	Lecture	Subject	Textbook Reading	Assigned	Due
Mo Jan 5	1	Introduction	1.{1-5}		
We Jan 7	2	Hardware/software interface I	2.{1-4, 6}		
Mo Jan 12	3	Hardware/software interface II	2.{7-10}	Lab 1	
We Jan 14	4	Hardware/software interface III	2.{4, 11-14} 6.3		
Mo Jan 19	--	MLK Day, no class	-		
We Jan 21	5	Efficiency metrics	1.{6-7}		Lab 1
Mo Jan 26	6	Hardware design overview	Appendix B	Lab 2 HW 1	
We Jan 28	7	Processor design	4.{1-4}		
Mo Feb 2	8	Pipelined processor I	4.{5-6}		
We Feb 4	9	Pipelined processor II	4.7		
Mo Feb 9	10	Pipelined processor III	4.{8-10}	Lab 3	Lab 2
We Feb 11	11	Memory hierarchy I	5.{1-4}	HW2	HW 1
Mo Feb 16	--	Presidents' day, no class			
We Feb 18	12	Memory hierarchy II	5.{8-10}		
Mo Feb 23	13	Memory hierarchy III	5.10, 6.5		
We Feb 25	14	Custom accelerators	Lecture notes	Lab 4	HW2 Lab 3
Mo Mar 2	15	Virtual memory	5.7	HW3	
We Mar 4	16	Operating system support	4.9		
Mo Mar 9	17	I/O devices & interfaces	6.9		
We Mar 11	18	I/O optimizations	Lecture notes		HW3 Lab4
Tu Mar 17	-	Final exam (8.30 – 11.30am)			

Midterm?