EE282H Computer Architecture and Organization
Information Sheet

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Course Support:	Darlene Hadding	
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***** Handouts are always available in filing cabinet on Gates 3rd floor open area.*****

Assignments

Homework and programming assignments (three) should be done in teams of two people. We will supply homework solutions. If you still do not understand the problem after receiving the graded homework and solutions, you should arrange to see the instructor or TA for further explanation. The programming assignments will be given during Chapters 2, 4, and 5. The purpose of the first programming assignment is to familiarize you with the Verilog® hardware description language and a simple CPU model. In the second programming assignment, you will use pipelining to improve the CPU's performance. In the third programming assignment, you will make modifications to a cache simulator. You will have 1-1/2 weeks for the first assignment, 3 weeks for the second assignment, and 2-1/2 weeks for the third assignment. There is a Midterm during the second programing assignment; however, it is not a good idea to wait until after the Midterm to begin this assignment. The programming assignments will be available on AIR. You are free to port them to your own machines, but we cannot provide any assistance. For questions regarding assignments, send electronic mail to the TAs. You **must** read the class web page **http://www-leland.stanford.edu/class/ee282h/** for updates and clarifications to the assignments.

Late Assignment Policy

Exercises are due on the dates indicated in the schedule. You have two free late days that you may use at any time during the quarter. You must indicate on your assignment that you want a free late day used — no exceptions. After you have used your free late days, late assignments will be assessed a penalty of 20% off the possible score per day. No other arrangements for late homework or programming assignments will be made.

Exams: There will be both a Midterm and a Final. The Midterm will cover material in Chapters 1-4 and the Final will cover everything. The Midterm will be given in the evening to allow two hours for the exam. Before each exam, the TAs will hold a review session. Local TV students are expected to come to Stanford for the Midterm and the Final.

Grading: Homework and programming assignments will constitute 40-50% of the grade, Midterm 25%, and Final 25-35%.

Text: J. Hennessy and D. Patterson, "Computer Architecture: A Quantitative Approach" second edition. If you find any bugs or discrepancies, send e-mail to the publisher (arc2bugs@mkp.com) and receive $1.00 if your bug is accepted.

Prerequisites: EE182. You **must** have a good knowledge of basic machine organization and logic design. You should also have exposure to at least one machine language **in detail** and a basic knowledge of operating system concepts, such as paging and segmentation. This course moves relatively fast; if you are unsure of your background, take EE182.

Review Sessions: The TAs will have a review session every other week.

Tentative Course Schedule

Date	*Lecture*	*Subject*	*Reading*	*HW Assigned*	*HW Due*
Thu, Sept 24	1	Introduction , computer design	Ch 1		
Tue, Sept 29	2	evaluating perfromance and cost	Ch 1	1	
Thu, Oct 1	3	ISA design principles and the VAX (CISC)	2.1–2.6	2	1
Tue, Oct 6	4	DLX (RISC), compiler effects, ISA measurements	2,7–2.8	Pgm 1	
Thu, Oct 8	5	basic pipelining, pipeline hazards	3.1–3.4		
Tue, Oct 13	6	control hazards	3.5–3.6	3	2
Thu, Oct 15	7	multicycle operations, exceptions	3.7–3.9	Pgm 2	Pgm 1
Tue, Oct 20	8	instr level parallelism, dynamic scheduling	4.1–4.2		
Thu, Oct 22	9	branch prediction	4.3	4	3
Tue, Oct 27	10	speculation and compilers	4.5,4.6		
Thu, Oct 29	11	multiple instruction issue, speculation	4.4,4.8		
Tue, Nov 3		***Midterm exam***	Ch 1-3		
Thu, Nov 5	12	Caches 1: design, evaluation, reducing misses	5.1–5.3		4
Tue, Nov 10	13	Caches 2: reducing penalties	5.4–5.5	Pgm 3	Pgm 2
Thu, Nov 12	14	Memory 1: main memory	5.6	5	
Tue, Nov 17	15	Memory 2: virtual memory	5.7–5.10		
Thu, Nov 19	16	MIPS R10000 pipeline	handout		
Tue, Nov 24	17	I/O 1: performance, disks, buses	6.1–6.3	6	5
Tue, Dec 1	18	I/O 2: memory interface, I/O benchmarks	6.4–6.6		Pgm3
Thu, Dec 3	19	I/O 3: I/O design, file caches	6.7–6.8		
Thu, Dec 10		***Final exam, 3:30-6:30 PM***	Ch 1-7		