

EE282H Homework #5

Due: Tuesday, Dec 1, 1998

Question 1.0 (30 points)

Exercise 5.4

Question 2.0 (30 points)

Exercise 5.5

Question 3.0 Memory Hierarchy Design (75 points)

For evaluating the following memory hierarchy we will use a benchmark with the instruction mix given in the following table (CPI given for a perfect cache with 1 cycle access time).

Instr. Type	Frequency	CPI
ALU Instr.	30%	1.2
Load	25%	1.0
Store	10%	1.0
Branches	25%	1.8
Other	10%	2.0

The memory system has the following characteristics:

- Main Memory: 48 MB

Average Main Memory Access Time: 50 cycles (L2 miss penalty).

- L2 Unified Cache: 256KB, 2 way set-associative

Write Back, Write Allocate

Access Time: 5 cycles

Global Miss Rate: 2%

20% of the replaced lines are dirty.

- L1 I-Cache: 8KB, Direct Mapped

Write Through, Write Allocate

Read Hit: 1 cycle (including TLB access)

Miss Rate: 5%

- L1 D-Cache: 8KB, Direct Mapped
Write Through, Write Allocate
Read Hit: 1cc (including TLB access)
Miss Rate: 15%

- All Caches are physically addressed with physical tags,
Block size is 32 bytes.
- Assume we have a perfect write buffer.
- Page Size = 16KB

- D-TLB: 32 entries, Fully Associative
Miss Rate: 0.2%

- I-TLB: 32 entries, Fully Associative
Miss Rate: 0.1%

- Average TLB Miss Penalty: 30 cycles

The replacement policy for all caches and buffers is LRU.

3.a (5 points) Given this memory system how would you implement write hits to maximize performance? How many cycles do write hits take using your implementation?

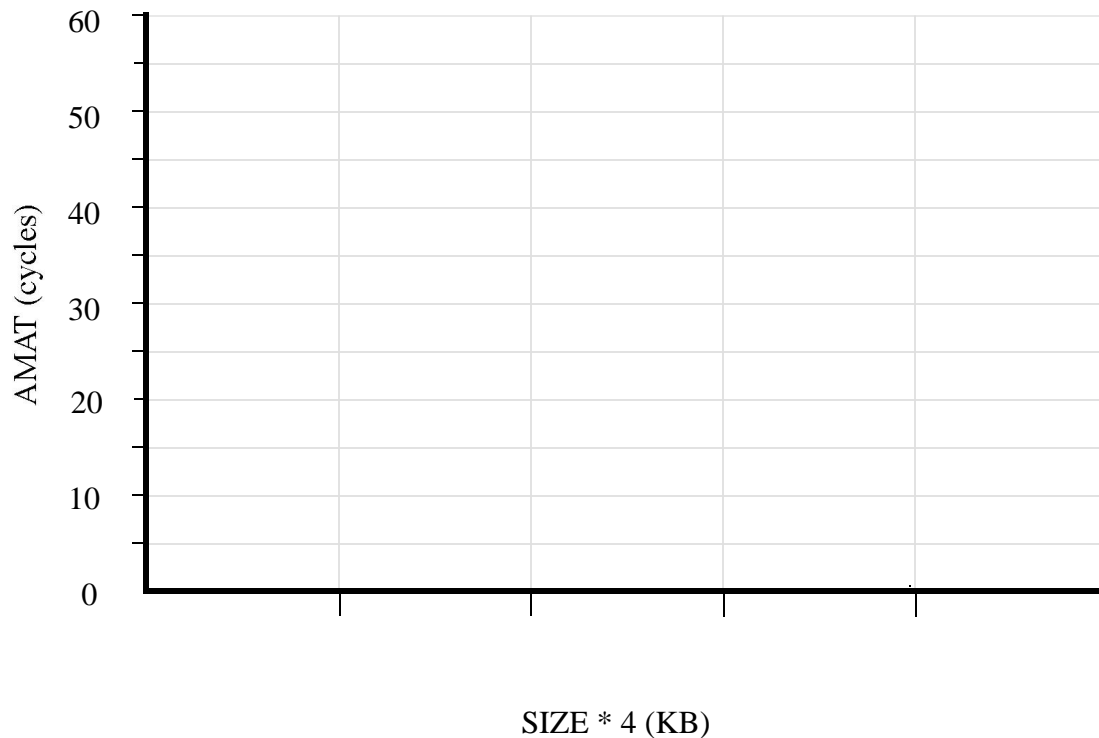
3.b (10 points) Assume ideal TLBs, what is the AMAT of the memory system? (access = read or write).

3.c (5 points) What is the AMAT for the system with the realistic TLBs?

3.d (10 points) Calculate the CPI for the system with realistic TLBs.

3.e (15 points) Given the following small C-program. Please draw the AMAT graph for data accesses versus SIZE in the range of [0..1M]. Assume that the cache is empty at the beginning of the program and that integers are 4 bytes long.

```
int x[SIZE];
int y,j,i;
for (j=0;j<1000000;j++)
    for (i=0;i<SIZE;i=i+8)
        y=x[i];
```



3.f (15 points) You decide to improve your memory system by making all the caches non blocking. What is the speedup for the memory reads on the program from part (e) for $SIZE=600K$ with the new memory system? Assume you can have up to 8 outstanding requests on the memory bus and the bandwidth of the bus is 300MB/s. Also assume that the processor runs at 200 MHz that you have a split transaction bus with separate address and data wires.