Outline

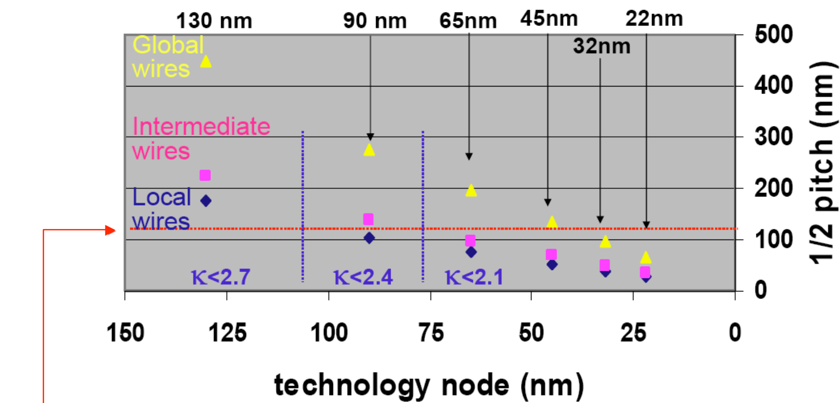
•Interconnect scaling issues

•Aluminum technology

•Copper technology

Wire Half Pitch vs Technology Node

ITRS 2002



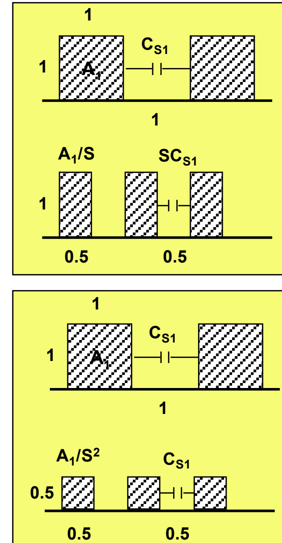
Narrow line effects

Ref: J. Gambino, IEDM, 2003

Interconnect Scaling Scenarios

- **Scale Metal Pitch with Constant Height**
  - R, C_s and J increase by scaling factor
  - Higher aspect ratio for gapfill / metal etch
  - Need for lower resistivity metal, Low-k

- **Scale Metal Pitch and Height**
  - R and J increase by square of scaling factor
  - Sidewall capacitance unchanged
  - Aspect ratio for gapfill / metal etch unchanged
  - Need for very low resistivity metal with significantly improved EM performance



Why Cu and Low-k Dielectrics?

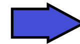
Low ρ (Resistivity)

Metal	Bulk Resistivity [μΩ•cm]
Ag	1.63
Cu	1.67
Au	2.35
Al	2.67
W	5.65

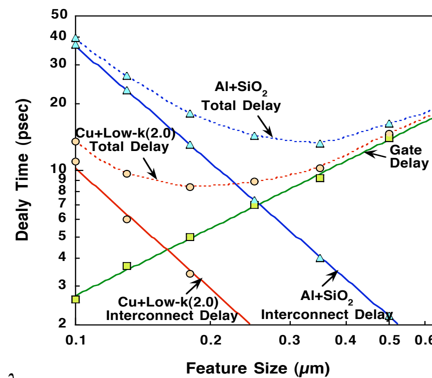
Cu is the second best conducting element

$$\tau_{RC}\ \alpha\ K_{ox}\varepsilon_o\rho\frac{L^2}{WH}\left(\frac{W}{X_{ox}}+\frac{H}{L_S}\right)$$

$$\alpha\ K_{ox}\varepsilon_o\rho\frac{L^2}{\lambda^2}\ for\ W = H = L_S = X_{ox} = \lambda$$

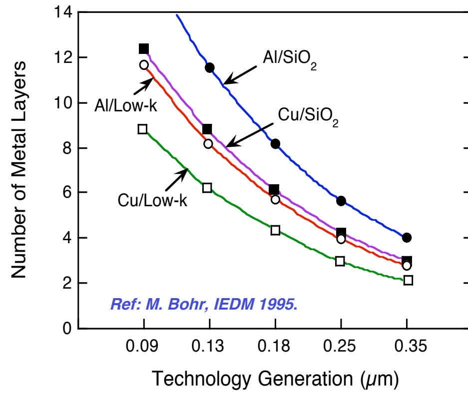


Reduced RC delay

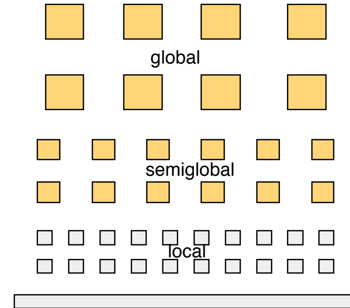


Calculations assume longest interconnect in the chip controls delay

Why Cu and Low-k Dielectrics?



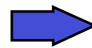
Technology Generation (μm)



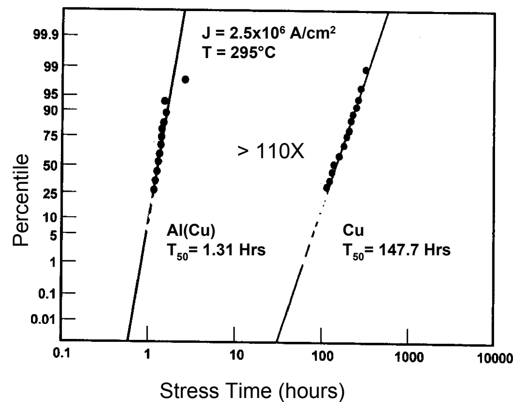
Better electromigration resistance, reduced resistivity and dielectric constant results in reduction in number of metal layers as more wires can by placed in lower levels of metal layers.

Why Cu?: Excellent Reliability

	Al	Cu
Melting Point	660 ºC	1083 ºC
E_a for Lattice Diffusion	1.4 eV	2.2 eV
E_a for Grain Boundary Diffusion	0.4 – 0.8 eV	0.7 – 1.2 eV



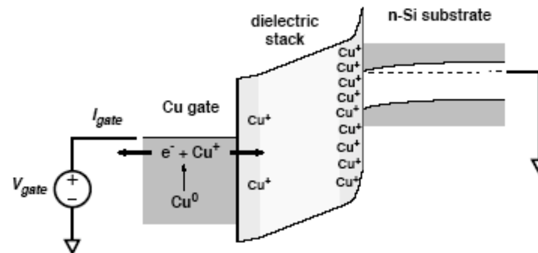
high electromigration resistance



Stress Time (hours)

Ref: S. Luce, (IBM), IEEE IITC 1998

Problem: Copper Diffusion in Dielectric Films

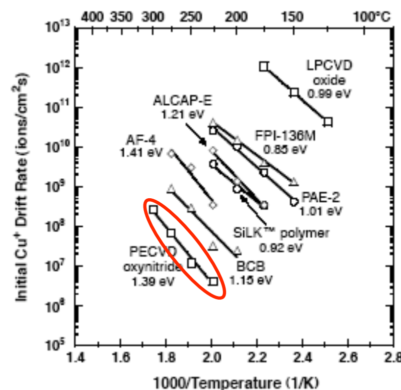


Cu atoms ionize, penetrate into the dielectric, and then accumulate in the dielectric as Cu+ space charge.

Copper Diffusion in Dielectric Films

Bias temperature stressing is employed to characterize behavior

- Both field and temperature affect barrier lifetime
- Neutral Cu atoms and Cu ions contribute to Cu transport through dielectrics



Ref: A. Loke et al., Symp. VLSI Tech. 1998

Silicon nitride and oxynitride films are better barriers

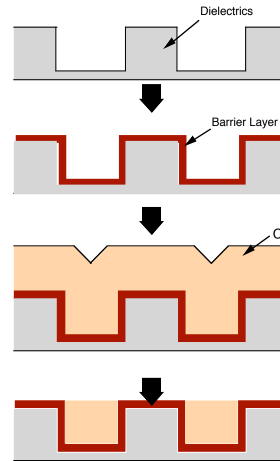
Solutions to Problems in Copper Metallization

- Fast diffusion of Cu into Si and SiO_2
- Poor oxidation/corrosion resistance
- Poor adhesion to SiO_2

Diffusion barrier /adhesion promotor
Passivation

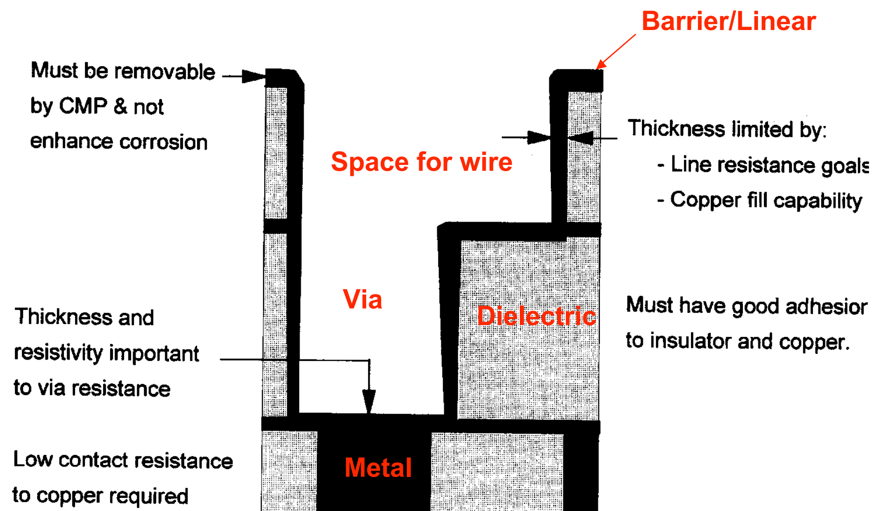
- Difficulty of applying conventional dry-etching technique

Damascene Process



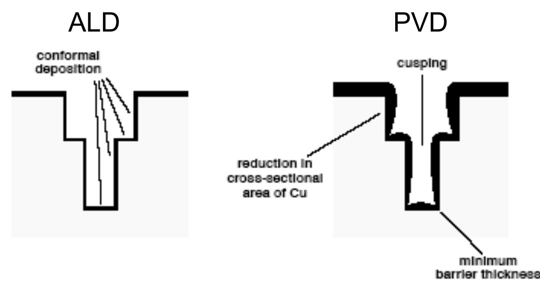
Typical Damascene Process

Barriers/Linears

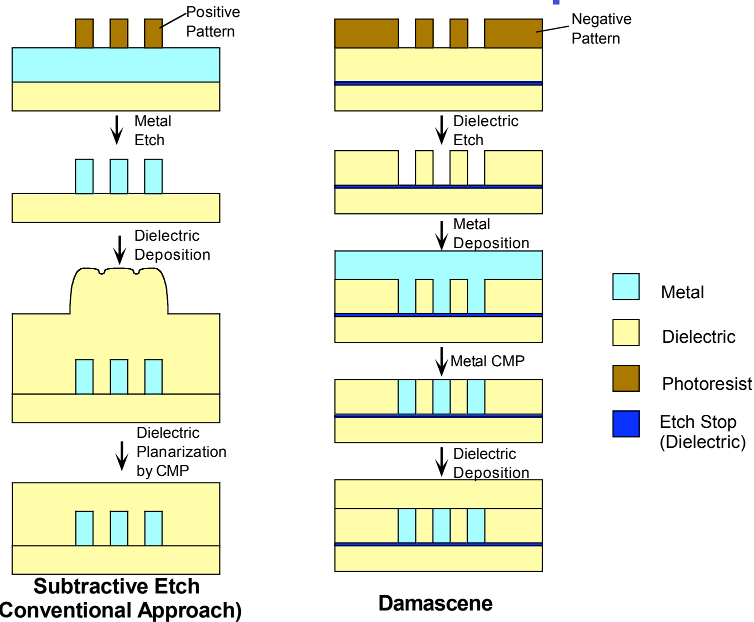


Materials for Barriers / Liners

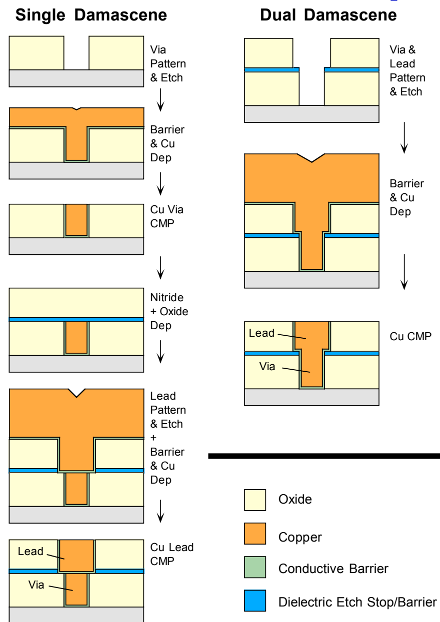
- Transition metals (Pd, Cr, Ti, Co, Ni, Pt) generally poor barriers, due to high reactivities to Cu <450˚*C*. Exception: Ta, Mo, W ... more thermally stable, but fail due to Cu diffusion through grain boundaries (polycrystalline films)
- Transition metal alloys: e.g., TiW. Can be deposited as amorphous films (stable up to 500˚C)
- Transition metal - compounds: Extensively used, e.g., TiN, TaN, WN.
- Amorphous ternary alloys: Very stable due to high crystallization temperatures (i.e., $Ta_{36}S_{14},N_{50}$, $Ti_{34}Si_{23}N_{43}$)
- Currently PVD (sputtering/evaporation is used primarily to deposit the barrier/liner, however, step coverage is a problem. ALD is being developed for barrier/liner application.



Interconnect Fabrication Options



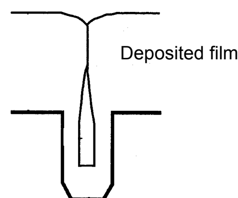
Cu Damascene Flow Options



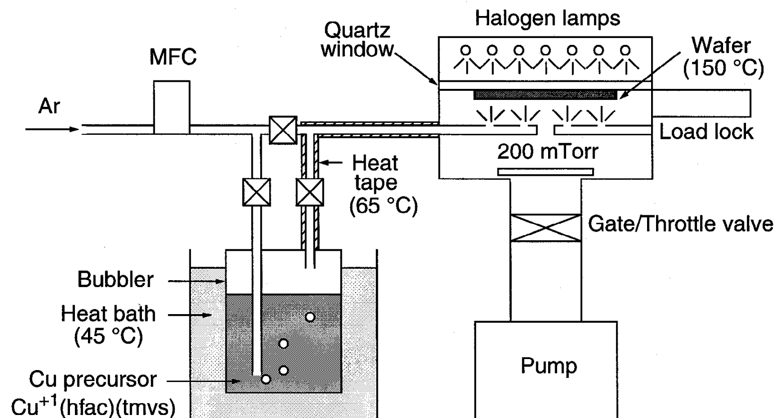
Deposition methods of Cu films: PVD

Various deposition methods for Cu metallization has been attempted :

- **Physical vapor deposition (PVD) : Evaporation, Sputtering**
  - conventional metal deposition technique: widely used for Al interconnects
  - produce Cu films with strong (111) texture and smooth surface, in general
  - poor step coverage: not tolerable for filling high-aspect ratio features



Deposition methods: CVD

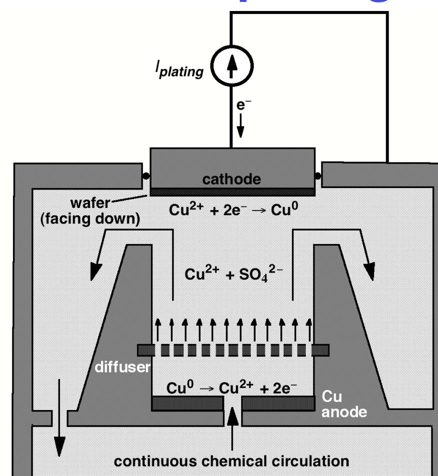


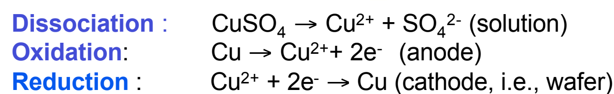
- conformal deposition with excellent step coverage in high-aspect ratio holes and vias
  - costly in processing and maintenance
  - generally produce Cu films with fine grain size, weak (111) texture and rough surface

Deposition methods: Electroplating

Copper electroplating Chemistry :

- Plating Bath : standard sulfuric acid copper sulfate bath (H_2SO_4, $CuSO_4$ solution)
- Additives to improve the film quality



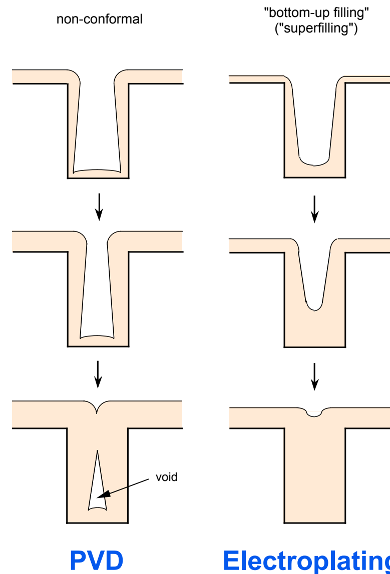


Dissociation : $CuSO_4 \rightarrow Cu^{2+} + SO_4^{2-}$ (solution)
Oxidation: $Cu \rightarrow Cu^{2+} + 2e^-$ (anode)
Reduction : $Cu^{2+} + 2e^- \rightarrow Cu$ (cathode, i.e., wafer)

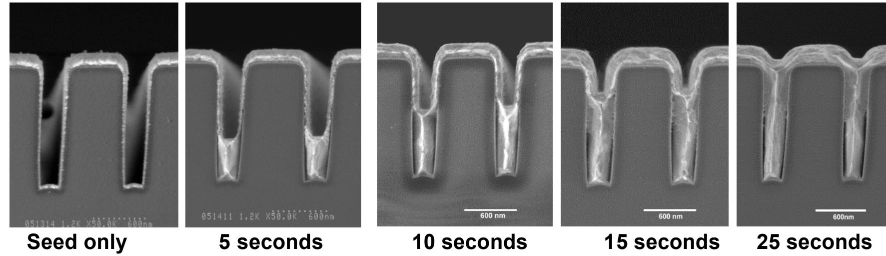
Why Cu Electroplating?

- **Electrochemical deposition (EVD)**
  - Good step coverage and filling capability comparable to CVD process (0.25 μm)
  - Compatible with low-K dielectrics
  - Generally produce strong (111) texture of Cu film
  - Produce much larger sized grain structure than any other deposition methods through self-annealing process

Trench Filling PVD vs. Electroplating of Cu



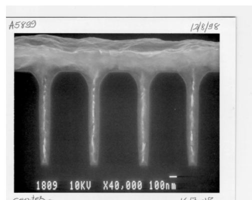
Plated Copper Fill Evolution



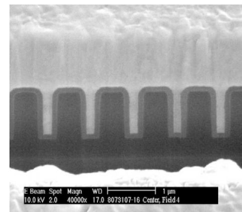
Seed only | 5 seconds | 10 seconds | 15 seconds | 25 seconds

Ref: Jonathan Reid, IITC, 1999

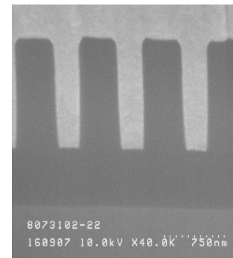
Trench Filling Capability of Cu Electroplating



0.13μ trenches



0.18μ vias



029μ vias

Ref: Jonathan Reid, IITC, 1999

Additives for Copper ECD

DEFINITION

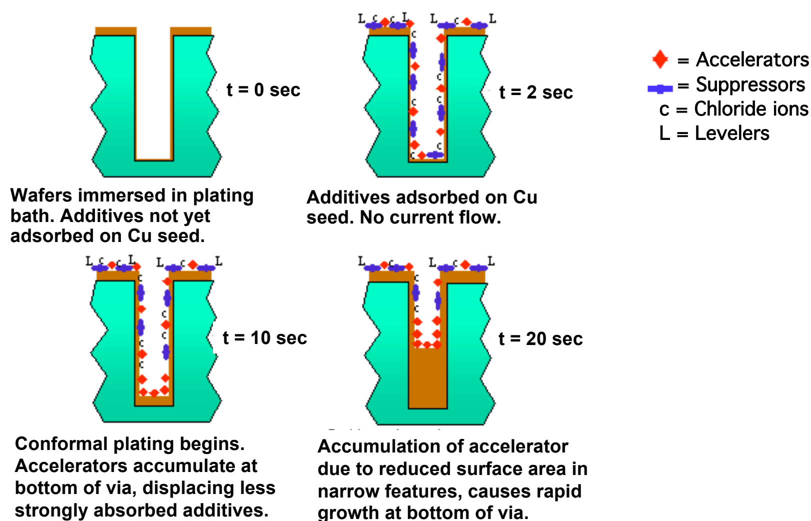
- Mixture of organic molecules and chloride ion which are adsorbed at the copper surface during plating to:
  - -- enhance thickness distribution and feature fill
  - -- control copper grain structure and thus ductility, hardness, stress, and surface smoothness

COMPONENTS

- Most commercial mixtures use 3 or more organic components and chloride ion which adsorb at the cathode during plating.

Brighteners (Accelerators) Levelers Carriers Chloride Suppressors

Mechanisms of Superconformal Cu plating



Ref: J. Reid et al., Solid St. Tech., 43, 86 (2000)
D. Josell et al., J. Electrochem. Soc., 148, C767 (2001)

Role of Additives

Brighteners (Accelerators)

- Adsorbs on copper metal during plating, participates in charge transfer reaction. Determines Cu growth characteristics with major impact on metallurgy

Levelers

- Reduce growth rate of copper at protrusions and edges to yield a smooth final deposit surface.
- Effectively increases polarization resistance at high growth areas by inhibiting growth to a degree proportional to mass transfer to localized sites

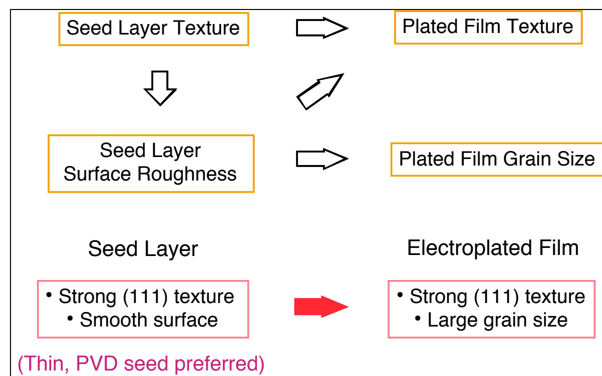
Carriers

- Carriers adsorbed during copper plating to form a relatively thick monolayer film at the cathode (wafer). Moderately polarizes Cu deposition by forming a barrier to diffusion of Cu^{2+} ions to the surface.

Chloride

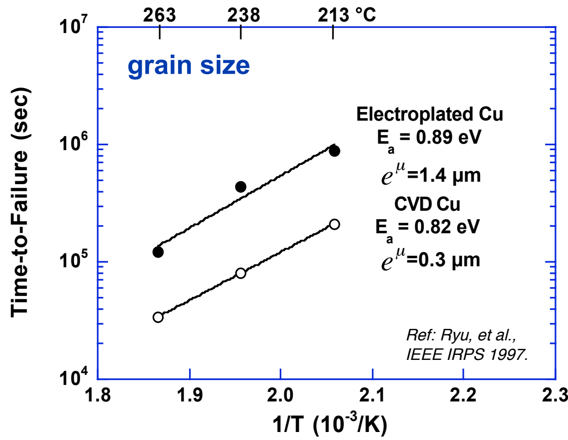
- Adsorbs at both cathode and anode.
- Accumulates in anode film and increases anode dissolution kinetics.
- Modifies adsorption properties of carrier to influence thickness distribution.

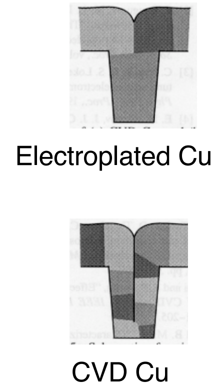
Effect of of the seed layer on the properties of the final Cu



- **Electroplating needs a seed layer of Cu as it does not occur at a dielectric surface.**
- **Properties of the final Cu layer critically depend upon the characteristics of the seed layer.**
- **The deposition of the seed layer can be done by PVD, CVD or ALD.**
- **Currently PVD is preferred, CVD and ALD being investigated**

Electromigration: CVD vs. Electroplating





Electroplated Cu

CVD Cu

Electroplated Cu has higher resistance to electromigration because of its grain structure

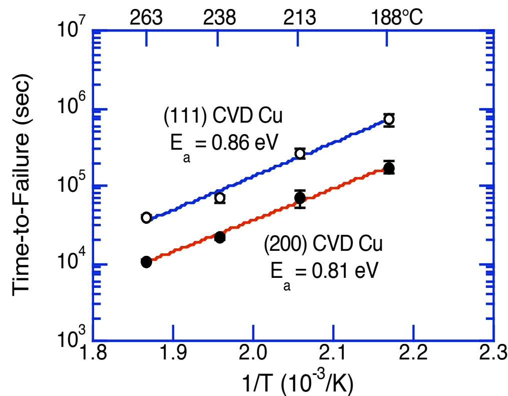
Film Microstructure vs. EM Time-to-Failure

- Empirical relationship (for Al & Al alloys)

$$MTF \propto \frac{e^{\mu}}{\sigma^2} \log\left[\frac{I_{(111)}}{I_{(200)}}\right]^3$$

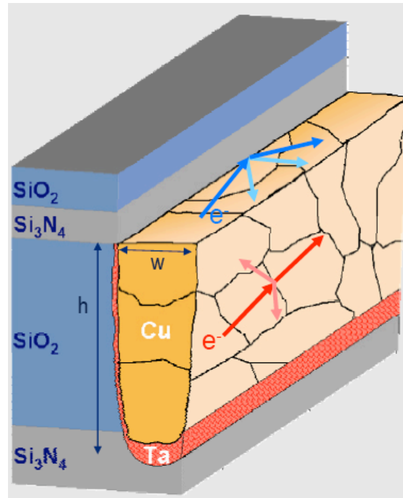
S. Vaidya et al.,
Thin Solid Films, Vol. 75, 253, 1981

- EM dependence on the microstructure of Cu films



Ref: Ryu, Loke, Nogami and Wong, IEEE IRPS 1997.

Cu Resistivity: Effect of Surface and Grain Boundary Scattering



Surface Scattering

Fuchs-Sondheimer model

$$\rho_{surf} = \rho(h, w, p, \lambda)$$

h, w: conductor height and width
p: specularity parameter
λ: electron mean free path

Grain Boundary Scattering

Mayadas-Shatzkes model

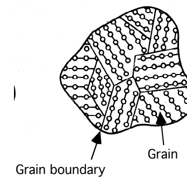
$$\rho_{g.b.} = \rho(d, R, \lambda)$$

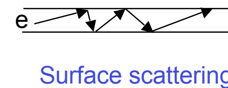
d: ave. grain boundary distance
R: Reflection coefficient at g.b.
λ: electron mean free path

W. Steinhögl et al., Phys. Rev. B66 (2002)

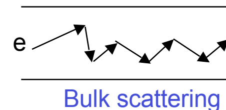
Thin Film Resistivity: Role of Carrier Scattering

- Effect of Electron Scattering
  - •Reduced mobility as dimensions decrease
    - ➢ Grain boundary scattering
    - ➢ Surface scattering
  - •Reduced mobility as chip temperature increases
    - ➢ Increased phonon scattering



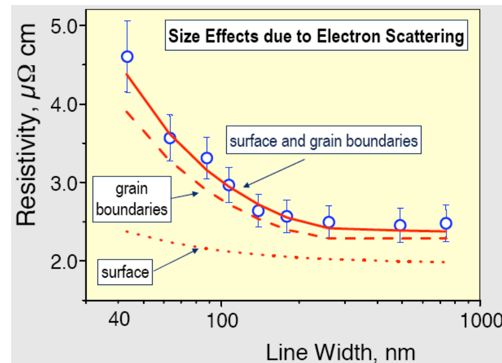


Surface scattering



Bulk scattering

Cu Resistivity: Effect of Line Width Scaling Due to Scattering

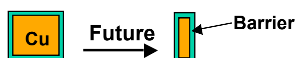


- ❑ **Resistivity increases as grain size decreases due to increase in density of grain boundaries which act as carrier scattering sites**
- ❑ **Resistivity increases as main conductor size decreases due to increased surface scattering**

W. Steinhögl et al., Phys. Rev. B66 (2002)

Cu Resistivity: Effect of Cu diffusion Barrier

- ❑Effect of Cu diffusion Barrier
  - Barriers have higher resistivity
  - Barriers can't be scaled below a minimum thickness
  - Consumes larger area as dimensions decrease
- ❑Resistivity of the composite wire is increased



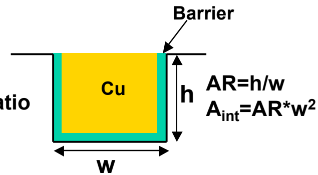
➢**Resistivity of metal wires could be much higher than bulk value**

Cu Resistivity: Integrated Model

Barrier Effect

$$\frac{\rho_b}{\rho_o} = \frac{1}{1 - \frac{A_b}{AR * w^2}}$$

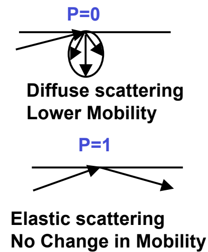
- Important parameter: A_b to A_{int} ratio
- ρ_b increase with A_b to A_{int} ratio
- Future: ratio may increase



Electron Surface Scattering Effect

$$\frac{\rho_s}{\rho_o} = \frac{1}{1 - \frac{3(1-P)\lambda_{mfp}}{2d}\int_1^{\infty}\left(\frac{1}{X^3} - \frac{1}{X^5}\right)\frac{1-e^{-kX}}{1-Pe^{-kX}}dX}$$

P: Fraction of electrons scattered elastically from the interface
k= d/ λ_{mfp}
λ_{mfp}: Bulk mean free path for electrons
d: Smallest dimension of the interconnect

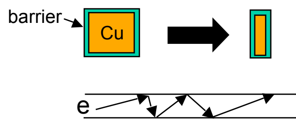


- Reduced electron mobility
  - Operational temperature
  - Copper/barrier interface quality
  - Dimensions decrease in tiers: local, semiglobal, global

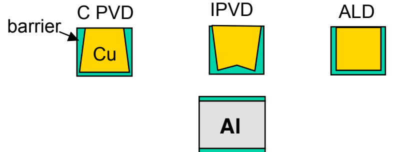
Kapur, McVittie & Saraswat, IEEE Trans. Electron Dev. April 2002

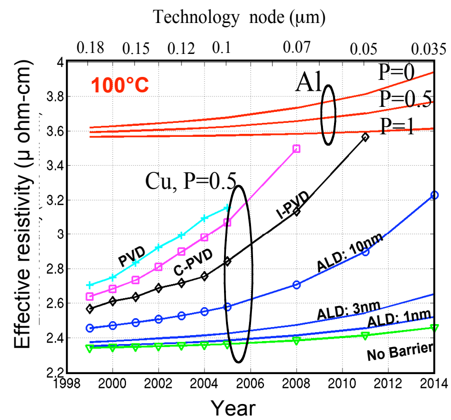
Cu Resistivity: Global Interconnects

Effect of Scaling



Effect of Barrier Technology

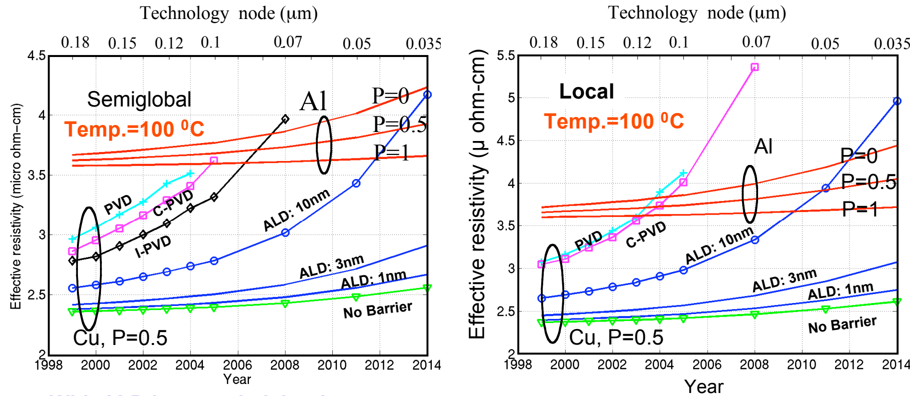




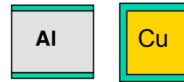
Kapur and Saraswat, IEEE TED, April 2002

- Barriers can't be scaled and have very high resistivity
- Surface electron scattering increases resistivity of scaled wires
- Real chips operate at higher temperatures

Semi-global & Local Interconnects

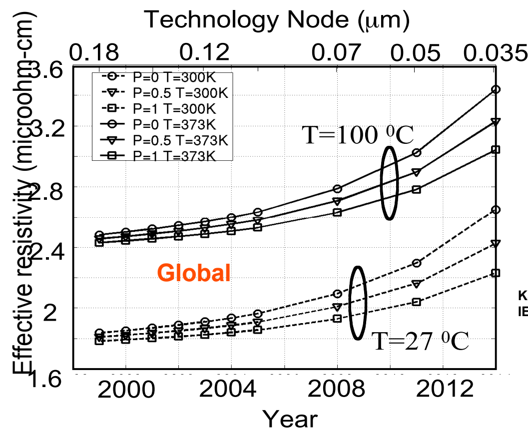


- With ALD least resistivity rise
- Al resistivity rises slower than Cu. Cross over with Cu resistivity possible
  - no 4 sided barrier, needs only thin TiN to improve reliability and as anti reflection coating
  - smaller λ_{mfp} => smaller k
  - But has reliability problem



Kapur, McVittie & Saraswat, IEEE Trans. Electron Dev. April 2002

Cu Resistivity: Effect of Chip Temperature



Kapur, McVittie & Saraswat
IEEE Trans. Electron Dev. April 2002

- Higher temperature ⇒ lower mobility ⇒ higher resistivity
- Realistic Values at 35 nm node: P=0.5, temp=100 ⁰C
  - local ~ 5 μΩ-cm
  - semi-global ~ 4.2 μΩ-cm
  - global ~ 3.2 μΩ-cm

Summary

- Interconnect scaling issues
- Thermal issues
- Electromigration
- Aluminum technology
- Copper technology