High-Performance Interconnects: An Integration Overview

ROBERT H. HAVEMANN, MEMBER, IEEE AND JAMES A. HUTCHBY, MEMBER, IEEE

Invited Paper

The Information Revolution and enabling era of silicon ultralarge-scale integration (ULSI) have spawned an ever-increasing level of functional integration on-chip, driving a need for greater circuit density and higher performance. While traditional transistor scaling has thus far met this challenge, interconnect scaling has become the performance-limiting factor for new designs. The increasing influence of interconnect parasitics on crosstalk noise and $R(L)C$ delay as well as electromigration and power dissipation concerns have stimulated the introduction of low-resistivity copper and low-permittivity (k) dielectrics to provide performance and reliability enhancement. Integration of these new materials into integrated circuit fabrication is a formidable task, requiring material, process, design, and packaging innovations. Additionally, entirely new technologies such as RF and optical interconnects may be required to address future global routing needs and sustain performance improvement.

Keywords—Aluminum metallization, ball grid array (BGA), bandwidth, bottom antireflection coating (BARC), chemical-mechanical planarization (CMP), code-division multiple access, coplanar waveguides, copper metallization, crosstalk, diffusion barrier, dual damascene, electrochemical deposition (ECD), electromigration, frequency-division multiple access (FDMA), global interconnects, IC packaging, interconnect, interlayer dielectric (ILD), International Technology Roadmap for Semiconductors (ITRS), intrametal dielectric (IMD), latency, local interconnects, low- k dielectrics, microstrip transmission line (MTL), Moore's law, optical interconnects, physical vapor deposition, RC delay, RC parasitics, RF interconnects, 3-D interconnects.

I. INTRODUCTION

Enhancements in integrated circuit (IC) density and performance have fueled the semiconductor industry and

resultant Information Revolution for over 40 years. The expected entitlement of periodic improvements in density (Moore's Law) and performance has, heretofore, been achieved through evolutionary device scaling and/or increase in chip size. For classical transistor scaling, device performance improves as gate length, gate dielectric thickness, and junction depth are scaled. In contrast, scaled chip wiring (interconnect) suffers from increased resistance due to a decrease in conductor cross-sectional area and may also suffer from increased capacitance if metal height is not reduced with conductor spacing. Thus, RC parasitics play an increasing role in overall chip performance as feature size scales, as shown in Fig. 1 [1]. As operating frequencies continue to spiral upward, parasitic inductive effects must also be considered.

Several recent analyses [2]–[7] have highlighted interconnect performance issues for future technology nodes specified by the ITRS [8]. A chief concern is the increasing latency or RC delay of global wiring. Since local and intermediate interconnects tend to scale in length, latency is dominated by global interconnects connecting large functional logic blocks, as illustrated in Fig. 2. Future increases in microprocessor chip size predicted by the ITRS [9] bring heightened concern, since interconnect latency is proportional to the square of length. While design solutions such as the use of repeaters (as shown in Fig. 1) or reverse scaling may mitigate latency in the near term, these approaches typically result in larger chip size and/or more levels of interconnect, leading to higher product cost.

Additional interconnect performance issues that have been identified include *crosstalk and noise*, particularly for local and intermediate wiring levels, *power dissipation*, and *power distribution*. Signal crosstalk is given by the ratio of line-to-line (sidewall) capacitance to total capacitance; power dissipation in interconnects is proportional to total capacitance, as is RC delay. Thus, it is important to simultaneously co-optimize the sidewall and total capacitance to insure that the best overall system performance is achieved.

Manuscript received August 10, 2000; revised February 18, 2001. This work was supported by International Sematech and the Semiconductor Research Corporation.

R. H. Havemann was with Texas Instruments Incorporated, Dallas TX 75243 USA. He is now with Novellus Systems Inc., San Jose, CA 95134 USA.

J. A. Hutchby is with the Semiconductor Research Corporation, Durham, NC 27703 USA.

Publisher Item Identifier S 0018-9219(01)04183-4.

Fig. 1. Gate and interconnect delay versus feature size. Interconnect delay versus feature size. Interconnect delay is shown for repeater spacings (L) of 3000 and 5000 μm .

Fig. 2. Comparison of length scaling for global versus local wires.

As transistor operating voltage continues to scale downward, interconnect crosstalk becomes increasingly important and noise levels must be reduced to avoid spurious transistor turn-on. Since crosstalk is dominated by interconnect sidewall capacitance (as is overall capacitance for minimum feature size as shown in Fig. 3), process-related solutions such as the use of thinner metallization and/or low- k dielectrics must be explored.

The interconnect scaling scenario shown in Fig. 4(b) illustrates how sidewall capacitance can be mitigated by reducing metal thickness, thereby avoiding any increase in crosstalk as conductor spacing decreases. However, for this approach resistance and current density in the wire increase with the square of the scaling factor, so RC delay and Joule heating increase, the latter raising reliability concerns. It is obvious that for this scaling approach to be effective in improving RC delay and crosstalk, a lower resistivity and higher reliability metal is needed; insertion of a lower permittivity (low- k) dielectric offers additional performance improvement.

The introduction of copper metallization served as an enabler for aggressive interconnect scaling due to its lower resistivity ($\sim 1.8 \mu\Omega\cdot\text{cm}$) as compared with traditional AlCu metallization ($\sim 3.3 \mu\Omega\cdot\text{cm}$) as well as improved reliability [10], [11]. Thus, for a fixed resistance per unit length, thinner

metal could be used for copper versus aluminum wiring and sidewall capacitance could be reduced. Later introduction of low- k dielectrics relieved sidewall capacitance [12]–[17] and provided more latitude in the optimization of RC, power, and crosstalk versus metal thickness and spacing.

The simulations shown in Fig. 5 highlight the respective performance advantages of a low- k dielectric and copper metallization in a typical microprocessor implementation [18]. Although aluminum/low- k competes well with copper/oxide (without comparing current density restrictions), the highest performance is achieved when copper and low- k are combined, as evidenced by the industry trend. The improved electromigration resistance of copper also allows higher current densities to be used in design, enabling further improvements in density and performance versus aluminum metallization.

Typical microprocessor designs utilize a hierarchical or “reverse scaling” metallization scheme (Fig. 6) where widely spaced “fat wires” are used on upper global interconnect and power levels to minimize RC delay and voltage drop. Maintaining power distribution at constant voltage through equipotential wires to all V_{dd} bias points requires increasingly lower resistance global wires as operating voltage continues to scale and switching frequencies increase. This need is being partially addressed by the introduction of ball-grid-array packaging technology that distributes individual power feeds across the chip, eliminating much of the need for lateral power distribution across chip. New packaging technologies will undoubtedly play an equally important role in alleviating power dissipation and system performance bottlenecks.

In order to meet future performance needs, the ITRS [8] predicts an acceleration in the need for new interconnect materials and processes. Table 1 highlights some of the key requirements for future technology nodes that will be discussed in the following sections. Of particular note is a need for increased current handling capability, lower permittivity dielectrics, and a reduction in metal barrier thickness. These changes, while extremely challenging, are to a certain extent evolutionary since traditional wiring technology will be employed. However, recent simulations [19] predict that in spite of these material changes the performance roadmap will not be met. Revolutionary approaches are needed to meet the performance challenge, and several new candidate interconnect technologies will be discussed in Section III.

II. HIGH-PERFORMANCE INTERCONNECTS

Over the past decade, the introduction of new materials and processes into the interconnect, or back-end-of-line (BEOL) portion of the IC process flow has become more the norm than the exception in the race for improved density and performance. Example innovations include: new chemical vapor deposition (CVD), physical vapor deposition (PVD) and electrochemical deposition (ECD) techniques for metals, novel dielectric and metal planarization techniques using chemical mechanical polishing (CMP) and new dielectric materials/processes for improved gap filling and/or reductions in permittivity (k).

Fig. 3. Components of parasitic capacitance versus feature size.

Fig. 4. Interconnect scaling scenarios for (a) fixed metal height and (b) fixed metal aspect ratio.

Fig. 5. Microprocessor performance as a function of feature size and interconnect technology (logic depth = 12 gates).

Initial changes to conventional aluminum metallization were driven by density and reliability concerns. Examples include the use of aluminum reflow for enhanced step coverage into high aspect ratio contacts or vias, and the subsequent introduction of CVD tungsten fill/etchback to form contact/via plugs. These improvements were necessary to provide reliable metal fill of the high aspect ratio contacts/vias that were a consequence of lithographic scaling. Likewise, dielectric CMP was implemented to improve the fidelity of high-resolution lithography by providing a more planar surface for imaging as depth of focus decreased

Line-to-line Capacitance = C_{L-L}
Line-to-ground Capacitance = C_{L-G}

with improved resolution. Planar dielectric surfaces also enhanced process margin and yield, since less overetch was required to clear metal filaments in forming tungsten plugs and aluminum leads. Later substitution of tungsten CMP for plasma etchback in tungsten plug formation provided additional yield enhancement and proved the viability of polishing inlaid metals (an ancient jewelry making process known as damascene) to form interconnect structures as illustrated in Fig. 7 [20]. Although subtractively etched aluminum alloys with damascene tungsten plugs is still the most predominate interconnect system, a rapid conversion to copper damascene is in progress driven by a need for higher performance and reliability.

A. Dual Damascene Copper

The success of metal CMP served as an enabler for the fabrication of copper interconnects, which had proven difficult to delineate by subtractive etch due to the limited number of volatile copper compounds. Copper deposition techniques (CVD, PVD, and ECD) were also developed to provide the necessary super-conformal filling of damascene structures, with ECD on a PVD copper seed layer and underlying PVD barrier metal emerging as the currently preferred production method. A dual damascene (DD) structure offers a further advantage in cost when compared with the single damascene or subtractive pattern/etch approach. In the dual damascene process, the conductor (trench) and via are formed prior to deposition of the metal barrier/Cu seed/Cu fill as shown in Fig. 8. Thus, only one metal fill and one metal CMP step are required for each level of interconnect, resulting in lower process cost as compared with the single damascene process. The dual damascene approach also provides lower via resistance and improved reliability by: 1) reducing the number of interfaces in the via (one bottom interface for DD Cu versus a top and bottom interface for single damascene Cu or Al with W plugs) and 2) providing full wire/via overlap at the top of the via (although overlap of the via with underlying metal is still subject to misalignment error). The disadvantages of a dual damascene approach include higher aspect ratios for etch/fill and more complicated integration schemes.

Several different dual damascene integration schemes have been demonstrated, but all approaches can generally

Typical Chip Cross Section

Fig. 6. Typical MPU interconnect cross section illustrating hierarchical scaling of Cu damascene.

be categorized as “via first” or “trench first” depending on which pattern is initially delineated. A comparison of the generic buried via first, via first and trench first approaches is illustrated in Fig. 9. In the buried via approach, the via level dielectric, or interlayer dielectric (ILD) and an etch stop layer (typically silicon nitride or silicon carbide for inorganic ILDs and oxide for organic ILDs) are sequentially deposited, followed by pattern and etch of the via into the etch stop layer. Following photoresist removal, the metal level dielectric, or intrametal dielectric (IMD) is deposited and patterned for trench delineation. The subsequent trench etch is extended to the underlying metal level through the via opening, while the etch stop layer maintains the trench bottom. The etch stop layer is removed from the bottom of the trench during the final etch step, which simultaneously clears the dielectric barrier from the bottom of the via. The chief advantage of the buried via approach is that all patterning is done on planar surfaces; major disadvantages include the need for an etch stop layer (which increases sidewall capacitance), the need for high etch selectivity to the etch stop layer and susceptibility to partial via definition if trench and via are misaligned. Partial vias present a potential reliability issue and, thus, this integration scheme should be avoided unless ample alignment tolerance is provided in the product design.

The ILD and IMD, with intervening etch stop layer (if desired), are deposited sequentially when using the via first or trench first approach, and the major difference between these integration schemes lies in the sequence of pattern and etch. In the via first approach, a high aspect ratio (HAR) etch is required to form vias prior to trench pattern. In subsequent trench patterning, the via is typically filled with a bottom antireflection coating (BARC) and/or photoresist to protect the dielectric barrier at the bottom of the via and prevent Cu exposure during trench etch (see Fig. 10). Removal of the BARC/photoresist plug after trench etch requires aggressive cleaning procedures which may damage low- k dielectrics. In the trench first approach, the via is patterned on the etched trench, which may present significant topography as shown in Fig. 9. In case of misalignment, partial vias can only be avoided by extended overetch to ensure that the full ILD/IMD thickness is cleared, which taxes etch selectivity to the via etch stop layer (not protected by a BARC as in the case of a via first approach).

Recently a fourth integration approach, the “top dual hardmask” approach shown in Fig. 11 [21], has been demonstrated [13]. In the top dual hardmask approach, the trench and via patterns are replicated in two different hardmask materials rather than in the IMD or ILD. Thus, photoresist can be removed prior to dual damascene trench etch, thereby

Table 1

(a) Near-Term MPU Technology Requirements (ITRS) and (b) Long-Term MPU Technology Requirements

Year of First Product Shipment	2000	2001	2002	2003	2004	2005
DRAM Half Pitch (2000 Litho ITRS)	150	130	115	100	90	80
MPU Half Pitch (2000 Litho ITRS)	180	150	130	115	100	90
Number of metal levels + extra levels for ground planes & SOC needs	6-7	7	7-8 + 2	8 + 2	8 + 2	8-9 + 2
Interlevel metal bulk dielectric constant	2.9	2.7	2.7	2.0	2.0	1.3
Interlevel metal effective dielectric constant	3.5-4.0	2.9-3.5	2.9-3.5	2.2-2.9	2.2-2.9	1.6-2.2
Conductor effective resistivity of Cu wiring ($\mu\text{ohm-cm}$)	2.2	2.2	2.2	2.2	2.2	2.2
Cu Barrier/Cladding thickness (nm)	16	14	13	12	11	10
Total Interconnect Length (m)	12632	14654	18624	21546	25249	31659
Reliability (FITs/m X 10E-3)	0.40	0.34	0.27	0.23	0.20	0.16

- Solutions exist
- Solutions being pursued
- No known manufacturable solutions

(a)

Year of First Product Shipment	2008	2011	2014
DRAM Half Pitch (2000 Litho ITRS)	60	40	30
MPU Half Pitch (2000 Litho ITRS)	70	50	35
Number of metal levels + extra levels for ground planes & SOC needs	9 + 3	9-10 + 4	10 + 4
Interlevel metal bulk dielectric constant	1.3	< 1.3	1.1
Interlevel metal effective dielectric constant	1.6	< 1.6	< 1.3
Conductor effective resistivity of Cu wiring ($\mu\text{ohm-cm}$)	2.2	< 1.8	< 1.8
Cu Barrier/Cladding thickness (nm)	7	5	4
Total Interconnect Length (m)	61730	91532	148835
Reliability (FITs/m X 10E-3)	0.10	0.05	0.03

- Solutions exist
- Solutions being pursued
- No known manufacturable solutions

(b)

minimizing exposure of the underlying IMD to potential plasma or chemical damage. The dual hardmask scheme also

can provide reasonably planar topography for patterning, with exact mask thickness depending on etch selectivity.

Fig. 7. Comparison of subtractive etch process (aluminum) with damascene process flow (copper).

Good etch selectivity between the hardmask materials and the IMD is the critical enabler for this approach. Therefore, organic IMDs with inorganic hardmask combinations such as nitride/oxide tend to be more easily integrated.

B. Low- k Dielectrics

Numerous low- k organic and inorganic materials spanning a wide range of dielectric constants, from air ($k = 1$) to fluorinated oxides ($k \sim 3.6$) have been explored for use in interconnect systems (see Table 2). However, only a limited number have been introduced into production (predominantly with aluminum metallization) due to integration and reliability issues. Integration and reliability issues that have impeded implementation of low- k dielectrics include thermally or mechanically induced cracking or adhesion loss, poor mechanical strength, moisture absorption, time-dependent behavior, chemical interactions (especially those which may occur during photolithography, etch/clean and dielectric/metal deposition), low electrical breakdown, and poor thermal conductivity. Relative permittivities of less than ~ 2.5 are generally achieved by the introduction of porosity, which further reduces mechanical strength and (for the predominant open pore systems) may increase moisture/chemical adsorption as well. While early demonstration of copper and porous low- k integration provides encouragement [22], co-optimization of material, process and integration architecture will be necessary for successful manufacturing implementation.

Still, the performance advantage of low- k dielectrics previously highlighted in Fig. 5 is clear, and is further underscored in Fig. 12 for the case of a dielectric with $k = 2$, representing an approximate 50% reduction in permittivity compared with standard plasma oxide ($k \sim 4.1$). Insertion of

Fig. 8. Cu damascene flow options.

the low- k dielectric between the metal leads results in a significant reduction in RC delay, extending the performance enhancement curve for at least one technology generation. Likewise, use of a homogeneous low- k provides further improvement, though less dramatic due to the dominant side-wall capacitance component.

Fig. 9. Dual damascene integration schemes.

Fig. 10. Cu/low k reliability failure mechanisms.

Generally, three types of dielectric structures (Fig. 13) have been utilized for low- k dielectric insertion in copper damascene architectures. Lowest overall capacitance is achieved by the first structure [Fig. 13(a)], where the conductor is embedded in a homogeneous low- k dielectric and no etch stop layer is used beneath the conductor. Initial trench depth is controlled by a timed etch, and some variation in depth with feature size or location on the wafer is expected. Insertion of an etch stop layer beneath the trench, as shown in Fig. 13(c), improves trench depth control but leads to slightly higher capacitance, since commonly used etch stop materials (silicon nitride, silicon carbide) exhibit higher permittivity than typical low- k dielectrics or silicon oxide. Final conductor thickness for all structures shown in Fig. 13 is impacted by CMP erosion and dishing (for wide leads).

In the third structure, shown in Fig. 13(b), two different dielectric layers are used (not counting etch stop layers), one with lower permittivity than the other. The material with

the lower permittivity is “embedded” at the conductor/IMD level, while the second material is employed at the via/ILD level. Since low- k materials typically exhibit less mechanical strength and reduced thermal conductivity as compared with silicon oxide, the embedded low- k approach allows co-optimization of electrical, mechanical, and thermal requirements [23]. The embedded low- k approach is expected to become increasingly more important as porous low- k materials with reduced mechanical strength and thermal conductivity are introduced.

Although sidewall capacitance dominates at minimum feature sizes, it is important to optimize the IMD and ILD thicknesses at each metal level for overall system performance and reliability. Key performance considerations impacted by parasitic capacitance include signal delay, crosstalk, and power. As integrated circuits are scaled, the length of local or intermediate interconnect levels typically scale as well, so alleviating RC delay at these levels may be less important than reducing crosstalk. High-performance microprocessors are particularly susceptible to crosstalk noise due to increasing frequency and lower transistor threshold voltages. Since crosstalk is proportional to the ratio of sidewall capacitance to total capacitance, this ratio must be minimized, and structures that offer lower overall capacitance [Fig. 13(a)] may not be the best choice. However, to minimize RC delay and power, lower overall capacitance is generally preferred, and the increased vertical capacitance of wider global interconnects must be taken into account.

Another factor that must be considered in choosing a dielectric architecture is the aspect ratio of the dual

Fig. 11. Top dual hardmask with trench first approach.

Table 2
Example Low- k Dielectric Materials

Material	κ (measured in the out-of-plane direction at ≤ 1 MHz)	Deposition Method
Fluorinated Silicate Glass (FSG or SiOF)	3.2 – 3.6	CVD
Polyimides	3 – 3.5	Spin-on
Hydrogen Silsesquioxane (HSQ)	2.8 – 3.0	Spin-on
Methyl Silsesquioxane (MSQ)	~ 2.7	Spin-on
Methylated Silica	2.7 – 3.0	CVD
Fluorinated Polyimides	2.5 – 3.0	Spin-on
Poly (arylethers)	2.7 – 2.9	Spin-on
Thermoset Polymers	~2.6	Spin-on
Parylenes (including co-polymers)	2.2 – 2.6	CVD
Fluorinated Amorphous Carbon (α -C:F)	2.1 – 2.5	CVD
PTFE (Teflon)	~1.9	Spin-on
Porous Inorganics (Xerogels, Templated Silica)	1.8 – 2.2	Spin-on
Porous Organics	<2.2	Spin-on

damascene structure. Higher dual damascene aspect ratios challenge etch, clean, and metal deposition processes and may require new process technology development. Thus, it is important to include aspect ratio considerations in the

overall performance tradeoff analysis. Design-in reliability analysis can also be used to identify heat dissipation issues in low- k dielectrics. The thermal modeling simulations in Fig. 14 highlight the increased temperature seen on upper

Fig. 12. Impact of low- k on interconnect performance.

levels of metal due to the poor thermal conductivity of low- k dielectrics, which is typically less than one third that of oxide [24]. Joule heating in turn accelerates electromigration in metal leads, and more effective cooling (from the substrate/package) is needed to maintain interconnect reliability. Alternatively, the embedded structure [Fig. 13(b)] can be used to provide a lower overall thermal conductivity for the multilayer dielectric stack, as shown in Fig. 14 for the case of an oxide ILD [23].

While copper conductors alleviate Joule heating effects through improved reliability performance, integration of low- k dielectrics with copper brings new integration concerns such as copper CMP on fragile low- k materials and degradation of low- k properties by etch and clean chemistries. These integration challenges become formidable as more and more porosity is introduced in the low- k dielectric to meet the ITRS permittivity goals. Bilayer oxide/low- k dielectric schemes may be required to enhance the mechanical strength and heat dissipation of future low- k dielectric systems, and novel packaging techniques will also likely be needed to minimize stress and optimize thermal cooling.

A final, but important integration consideration for low- k dielectrics is compatibility with the packaging environment. Although the flip chip (bumping) approach tends to dominate high-end products that are currently targeted for low- k dielectrics, wire bonding of chips containing low- k dielectrics is also likely to be needed as copper/low- k technology becomes pervasive. Fig. 15 offers a comparison of bump and wire bond challenges. For ball bond, compressive forces will severely test low- k materials, which typically have poor mechanical strength as compared with oxide. In contrast, bumping will apply shear stress to the multilayer dielectric stack, taxing the adhesion of dielectric and metal interfaces. Significant improvement in packaging technology and/or novel low- k integration schemes [such as the embedded approach shown in Fig. 13(b)] will be needed to overcome these challenges. Early evaluation of low- k dielectrics in the packaging environment, including mechanical evaluation of bonding and bumping as well as

the prerequisite reliability testing (thermal cycling, HAST, etc.) is an essential part of the product development process.

C. Copper Reliability

Copper metallization offers significant performance and reliability improvement but presents numerous integration and reliability challenges. Since copper readily diffuses into silicon and most dielectrics, copper leads must be encapsulated with metallic (such as Ta, TaN) and dielectric (such as SiN, SiC) diffusion barriers to prevent corrosion and electrical leakage between adjacent metal leads. Copper diffusion is also greatly enhanced by electric fields imposed between adjacent leads during device operation ($\sim 1 \times 10^5$ V/cm), and absolute barrier integrity is crucial to long term device reliability. Thus it is important to optimize dielectric etch/clean, chemical mechanical planarization, copper/barrier metal deposition processes and dielectric barrier deposition (see Fig. 16) to produce chemically and mechanically stable interfaces.

As metal width and intrinsic barrier thickness decrease with scaling, copper containment becomes increasingly more problematic. Surface roughness, such as may be encountered on etched porous low- k dielectrics, brings additional concerns. New CVD and atomic layer CVD (ALCVD) metal films such as WN, TiSiN, and TaN are under investigation as potential thin barrier solutions.

Copper, unlike aluminum, does not have a self-passivation layer. Exposed copper surfaces will continue to oxidize, leading to poor barrier adhesion and high resistance unless preventive measures and/or adequate cleaning are employed to produce chemically and mechanically stable interfaces. The electromigration behavior of copper also differs from aluminum in that surface diffusion tends to dominate over grain boundary diffusion, especially for narrow lines exhibiting bamboo grain structure [25]. This difference may be one reason preliminary data shows deterioration of copper reliability at smaller feature sizes [25].

Copper resistivity has also been projected to increase dramatically with smaller feature size due to electron scattering from grain boundaries and conductor walls [26]. While no degradation in the performance of current generation global interconnects ($\sim 2 \mu\text{m}$ conductor width) has been noted at low temperatures (-160°C) where the electron mean free path is increased [5], more study is needed to characterize scattering behavior. As feature size continues to shrink, ultrathin barriers or self-passivation techniques and improved grain size and texture control will likely be needed to optimize the effective resistivity of copper. Further study is also needed to verify the reliability performance of sub-100-nm wires and implement metallurgical improvements if necessary.

III. ALTERNATIVE INTERCONNECT APPROACHES

The bandwidth for data transmission (or communication) on global interconnect lines, either on a single chip or between chips along a substrate or board, is decreasing as integrated circuit technology is scaled to the future technology

Fig. 13. Typical IMD/ILD architectures.

nodes. For intrachip interconnects, bandwidth is decreasing due to a migration to smaller dimensions and a concomitant increase in clock frequency. (On-chip interconnect lines are RC dominated not LC; LC lines are limited by onset of skin resistance and have lower bandwidth than RC lines. Pure LC lines are probably not going to be important for some time to come). For interchip data communication, bandwidth is decreasing due to the relatively long time delays of package ball grid array (BGA) interconnects and the slow scale-up in number of input-outputs (I/Os) with respect to on-chip bandwidth.

The use of reverse scaling techniques, optimally spaced repeater amplifiers, and, perhaps, active equalization techniques [27] for intrachip global wires will mitigate global interconnect latency for the near term, but alternative solutions will still be needed for the advanced nodes extending to and beyond 35 nm. Furthermore, delays due to package and board-level connections must also be taken into account when transmitting signals between chips. Overall system delay involves a *hierarchy* of interconnects, each delaying the signal by increasing amounts. In the long term new design (e.g., microarchitectures such as asynchronous block functions) or technology solutions (e.g., guided RF using coplanar waveguides, free space RF, optical interconnects) will be needed to overcome the performance limitations of traditional global interconnects. Alternative technologies for global interconnects should meet the following goals: 1) they should provide both intrachip and interchip global interconnect without any penalty in latency for going off chip (i.e., eliminate the traditional hierarchical approach) and 2) they should substantially reduce the latency or delay of signal transmission, provide adequate signal bandwidth for future needs, and reduce cross coupling noise and power dissipation. Alternative global interconnect approaches

Fig. 14. Thermal issues for low- κ materials.

proposed thus far include: 1) optical interconnect; 2) RF interconnect; and 3) three-dimensional (3-D) integration technology. These approaches are briefly discussed and compared below.

A. Optical Interconnects

Optical interconnect technologies have long been considered as attractive alternatives to providing both interchip

Fig. 15. Packaging issues in Cu/low k .

Fig. 16. Dual damascene integration concerns.

and, perhaps eventually, intrachip replacement technology for metal/dielectric global interconnects. Proposed optical approaches can be grouped into guided wave and free space. Guided wave optics involves the use of waveguides to contain the optical signals within a board, package, or on a chip. Free-space optics utilizes diffractive optics and conventional lenses or microlens arrays to guide single or multiple parallel optical beams in free space. Fig. 17 shows one example of a free-space optical interconnect system that uses both refractive lenses with either a diffractive or reflective optical distribution surface.

Compared to electrical wires, optical technology offers fundamental advantages to global interconnects, given that the technology can be realized in a simple, cost effective im-

plementation. Miller [28], [29] shows that the bandwidth of electrical interconnects is $\sim A/l^2$, where A is the cross section area of the interconnect and l is the length, and is *independent* of 3-D scaling of the wires. The use of repeater amplifiers helps to increase the electrical bandwidth, but these amplifiers are not conveniently available to off-chip interconnects. Also, off-chip electrical interconnects are much longer than on-chip wires, thus causing the off-chip interconnects to limit the system bandwidths. Optical interconnects, however, are not bandwidth limited in this way, although they are limited by the propagation delays of optoelectronic components such as transmitters, modulators, and receivers. Further, the signal propagation velocity of electrical interconnects tends to be 10%–30% of the speed of light, c , whereas the optical

Fig. 17. Optical chip-to-chip interconnect packaging concept. (Source: D. A. B. Miller [28])

propagation velocity for guided waves tends to be $\sim(1/3)c$. The signal propagation velocity for free-space optics is approximately c , with the latency again being limited only by the optoelectronic components including the transmitters or modulators and the receiver circuits. For these and other reasons, optical interconnects are most attractive as off-chip or package/board applications. Furthermore, optical interconnects used for off-chip and on-chip clock and signal distribution have similar bandwidths and latency, and they, therefore, eliminate the hierarchical constraints imposed by off-chip electrical interconnects, i.e., the lower bandwidth and longer delay times.

Optical interconnects must overcome some rather difficult fundamental and technological challenges before they will find application even in off-chip applications. The first issue, particularly for on-chip guided wave optical interconnects, is the relative size of optical components (particularly waveguides and photo-receiver circuits) required. For this reason, guided wave optical interconnects may require separate active layers in the vertical dimension with via interconnect to the functional blocks to support the required optoelectronic components. A second issue may be realization of an acceptable error rate for the optical data links. Obtaining an acceptable error rate will require a tradeoff between the optical signal power versus the use of error correction techniques. An on-chip optical interconnect technology may require either impractical high levels of optical signal power or area intensive error correction circuits. The latter, again, can be achieved perhaps in a separate set of active interconnect layers.

Regarding technological challenges, active optoelectronic components (sources, modulators, and detectors) will most likely be III–V compound semiconductor devices. While some of these components can be fabricated in silicon, they exhibit quite serious and fundamental performance challenges. These challenges include low photodetector quantum efficiency and extremely low external quantum efficiency for light emitters. Similarly, further development of electromechanical optical components for use in free space optical interconnects also is required. Optical interconnects suffer additional disadvantages, some of which are rather fundamental and others are more technological. Power dissipation for receivers, and, to a lesser extent, transmitters can be prohibitively large. However, there is growing evidence that the power required per optical channel, i.e., one transmitter (or modulator) and one receiver connected via free-space may dissipate less than 6 mW of power [30] with

circuits that are quite small (e.g., $17 \times 18 \mu\text{m}^2$ in area). Other issues with optical interconnects are the technologies for fabricating III–V devices on silicon. Heteroepitaxial growth of III–V vertical-cavity surface-emitting lasers (VCSELs) on silicon CMOS circuits is a very difficult technology limited by reliability concerns. However, solder bonding technologies are available for attaching III–V lasers, modulators, and detectors on silicon circuits.

B. RF Interconnects

Radio frequency or wireless interconnect technologies only recently have been considered as viable candidates for either on-chip or, more likely, for off-chip interconnects replacing metal/dielectric global wires. This new approach has become possible because of the confluence of wireless technologies for communications applications with high-frequency silicon technologies. The cutoff frequencies of these advanced silicon technologies approach values sufficient to provide adequate data bandwidths in packages and, perhaps, on the chip. As with optical, RF technology is divided into the categories of free-space transmission and guided-wave transmission. The approach involving free-space transmission is focused upon demonstration of a 24-GHz wireless clock distribution system in CMOS technology with both an on-chip clock transmitter and, alternatively, with an off-chip external clock transmitter. The 24-GHz clock frequency will be divided down to obtain the required clock data rate [31], [32].

The approach employing guided waves uses on-chip transceivers driving capacitive, near-field couplers to feed the signals into a coplanar waveguide (CPW) or a microstrip transmission line (MTL) [33], [34]. As shown in Fig. 18, this CPW or MTL “base station” is located on another substrate placed directly above the CMOS chips in a multiple-chip package and is used to transmit the signals to all of the receiver nodes. A novel feature distinguishing this approach is the use of code division multiple access (CDMA) and frequency division multiple access (FDMA) to obtain up to 100 channels in a 100-GHz carrier connecting multiple transmitting and receiving nodes all coupled to the same CPW/MTL “base station.” Using local area network (LAN) communication techniques applied to microsystems applications, this micro-LAN (M-LAN) approach will provide high-speed, low-loss intrachip clock/signal distribution among multiple block functions on a chip, or, more likely, among multiple chips in a package.

Fig. 18. ULSI chips communicate with each other through a miniature wireless LAN inside an MCM package. (Source: M. F. Chang [33], [34])

Compared to global electrical wires or to BGA signal distribution in a package, RF interconnects potentially offer several advantages. First, circuits can be synchronized over much larger areas because both approaches transmit signals three to ten times faster for guided wave or free-space transmission, respectively, compared to global wires or to BGA package interconnects. In addition, the bandwidth of the RF approaches, much like optical interconnects, is only limited by the bandwidths of the transmitting and receiving components, and not by the transmission medium, as is the case for global wires. Also, the crosstalk between channels should be much improved, particularly for the approach using FDMA and CDMA communication techniques. Furthermore, the signal multiplexing capability of the M-LAN approach should reduce the actual number of I/O ports going off-chip and the M-LAN communications techniques can provide new flexibility to reconfigure the interconnect system simply by changing the CDMA codes. As with the optical interconnect approaches, RF wireless interconnect eliminates the hierarchical propagation delay or latency problems differentiating on-chip interconnect delays from the much longer off-chip BGA delays. On-chip and off-chip signal delays for wireless should be comparable and much improved over package delays associated with BGA package interconnects.

RF interconnects are a very new approach for intrachip and interchip interconnects, although the techniques proposed are well developed for wireless communications applications. Similarly, all of the required silicon technologies exist, albeit the very high cutoff frequencies expected for the 100-nm nodes and below will be needed to provide sufficient capacity of the RF interconnect systems. However, RF interconnect approaches also face the same fundamental issues related to component (transmitter, waveguide,

antenna, receiver) size and error correction noted in the previous discussion of optical interconnects.

RF interconnect has additional difficult challenges to overcome before becoming a viable candidate to replace global wires and/or BGA package interconnects. First, for package applications, the RF implementation must be cost competitive with BGA and must support the required form factors. Further, the power dissipated by RF interconnect support circuits must be equal to or less than the power dissipated by the global interconnect wires and BGA, and the silicon area consumed by these RF circuits must be less than a few $100 \mu\text{m}^2$. Another issue is the area required by a coupling capacitor, $\sim 600 \mu\text{m}^2$, is approaching the size of the balls in a BGA package. This raises the question of how such a large capacitance impacts interconnect delay time. Also, the RF power dissipation cannot add a significant amount of heat to an already heavy thermal load. Finally, similar to optical interconnects, RF interconnect systems will likely require adaptation of new system architectures to fully exploit the capabilities of RF interconnects.

C. 3-D Integration

Another approach to addressing the problem of global wires dominating clock delay is to reduce the number and the average lengths of the longest global wires. 3-D integration of active transistor layers or, as an intermediate step, placement of the clock/signal and power/ground wires on opposite sides of a chip has been shown to reduce the number and average length of two-dimensional (2-D) global wires by providing shorter “vertical” paths for connection. A 3-D approach has also been shown to reduce overall chip area when designs are interconnect-limited.

3-D integration also offers some attractive advantages related to system performance and enabling of new system architectures. First, it can extend the performance of high-speed transistors to technology nodes where the global wires otherwise are expected to present serious frequency limitations to advanced CMOS. Second, for systems-on-a-chip (SOC) applications, 3-D integration may provide the means to integrate dissimilar technologies (digital, memory, analog, RF, etc.) in the same cube (offering many of the wiring delay advantages of 2-D integration) but on different active layers. For example, power hungry digital circuits could be located on the bottom layer adjacent to the heat sink and lower-power/higher-voltage analog circuits on the top active layer. 3-D approaches could also enable integration of huge amounts of cache memory on top of a high performance microprocessor chip.

The recent introduction of several new process technologies may for the first time offer viable manufacturable processes for 3-D integration of CMOS. Perhaps the most important of these is a SOI CMOS integrated circuit manufacturing process recently announced by IBM [35]. Other new processes include low-temperature wafer bonding and layer separation technologies [36], [37] sophisticated techniques for epitaxial growth of selectively positioned layers and islands of silicon [38], [39] and chemical-mechanical polishing to obtain planar surfaces. These processes

Fig. 19. Three approaches to fabricating 3-D circuits: (a) Saraswat, (b) Neudeck, and (c) Antoniadis. (Source: K. Saraswat [28], [29])

collectively raise 3-D integration of CMOS to the realm of possibility.

Several different schemes have been proposed for implementing 3-D integration for the advanced technology nodes. These approaches range from simply locating interconnect metal on both sides of single die or active layer (e.g., clock/signal on the top side and power/ground on the back side [40], [41]) to fabrication of vertical CMOS gates with the P(N)MOS transistor placed on top of the N(P)MOS transistor [38], [39]. A variety of schemes call for attaching die to one another using wafer bonding combined with layer removal technologies [40], [41]. The die can be attached “top-to-top” (facilitating heat removal through the back of each of two active transistor layers) or “top-to-back” (facilitating use of three or four active layers in single stack). Fig. 19 illustrates three of these approaches.

Complex and difficult challenges remain, however, including management of thermal dissipation from interior stacked active layers, the need for 3-D routing and placement tools, development of new systems architectures to exploit 3-D integration, etc. Furthermore, there are diminishing returns for adding more than three or four active layers to a 3-D chip. For this reason, including more than four active layers would provide no further savings in active chip area needed to realize a system function or, therefore, in cost per transistor or function. The main near term benefit of 3-D integration may be the performance enhancements of global interconnect wires. Potentially, the biggest win

for 3-D integration may be as an enabler for new systems architectures.

D. Migration to Alternate Interconnect Technologies

A major question for each of the alternative interconnect technologies is how their bandwidth will scale with the increasing on-chip bandwidth of CMOS technology nodes. This question needs further analysis for all the approaches proposed, although preliminary analysis suggests that optical interconnects will keep pace with the upward scaling on-chip bandwidth [28], [29]. Another issue related to exploiting these new approaches is the maturity and manufacturing readiness of the required fabrication processes. Global wires with repeaters have been in use starting with the 0.25- μm node, and the active equalization techniques can be readily implemented with currently available CMOS technology. The RF M-LAN capacitively coupled CPW/MTL and direct broadcast techniques also use CMOS technology, although obtaining sufficient bandwidth capacity may require availability of the 100-nm technology node. Realization of optical interconnects, however, will likely require introduction of III–V technologies for the active components (lasers, modulators, photodetectors) and free-space optical components (diffractive, refractive and reflective gratings, lens, mirrors, etc.).

Daly [42] pointed out the growing dominance of data communications as *the* scarce resource in future packaged microelectronics systems, and proposed new systems architectural

approaches for relieving this problem. A technology-centric scheme for addressing the data communications issue within a multichip package is to completely separate the functions of global data communications from other systems functions. This can be done by introducing a separate data communications chip into the multichip package [33], [34]. This data communications chip could contain all of the global interconnect or data communications infrastructure (transmission media and support circuits) and would be used as a board within the multichip package to which the other systems chips are flip-chip bonded. Further, this data communications chip could provide a degree of intelligence by integrating interconnect switches allowing reconfiguration of the system. Finally, data communications by optical transmission could be eventually integrated into the data communications chip.

A plausible migration path for interconnect or data communications technologies could be to first develop the communications chip using global wires integrated with their support circuits (repeaters and active equalization circuits). If warranted, the RF M-LAN and/or direct broadcast approaches can be implemented followed eventually with the optical transmission technologies.

IV. CONCLUSION

The ever-increasing density, performance, and reliability requirements of ULSI circuits create significant process integration challenges for future interconnect systems. New materials such as copper metallization and low- k dielectrics have been introduced to meet the performance challenge. While new materials may provide interim relief, their continued rapid introduction, as emphasized by the ITRS, brings considerable risk and fails to satisfy long-term technology needs. The bandwidth for data transmission (or communication) on global interconnect wires either on a single chip or between chips along a substrate or board is decreasing as integrated circuit technology is scaled to the future technology nodes. While new system architectures may mitigate this crisis, alternative global interconnect schemes must also be explored. Several novel interconnect approaches that show promise include optical, RF, and 3-D interconnect technologies. Each of these technologies is also fraught with significant challenges, but hold the promise of higher bandwidth and continuing performance improvement.

ACKNOWLEDGMENT

The authors would like to thank their colleagues at International Sematech, Texas Instruments, SRC, Stanford University, and UCLA for their technical contributions to this overview.

REFERENCES

- [1] S. P. Jeng, M.-C. Chang, and R. H. Havemann, "Process integration and manufacturing issues for high performance interconnect," in *MRS Symp. Proc. Adv. Metallization for Devices and Circuits*, 1994, pp. 25–31.
- [2] M. Bohr, "Interconnect scaling—The real limiter to high performance ULSI," in *Tech. Dig. IEEE Int. Electron Devices Meeting*, 1995, pp. 241–244.
- [3] K. Rahmat, O. S. Nakagawa, S.-Y. Oh, J. Moll, and W. T. Lynch, "A scaling scheme for interconnect in deep-submicron processes," in *Tech. Dig. IEEE Int. Electron Devices Meeting*, 1995, pp. 245–248.
- [4] K. Yamashita and S. Odanaka, "Impact of crosstalk on delay time and a hierarchy of interconnects," in *Tech. Dig. IEEE Int. Electron Devices Meeting*, 1998, pp. 291–294.
- [5] A. Deutsch, H. Harrer, C. W. Surovic, G. Hellner, D. C. Edelstein, R. D. Goldblatt, G. A. Biery, N. A. Greco, D. M. Foster, E. Crabbe, L. T. Su, and P. W. Coteus, "Functional high-speed characterization and modeling of a six-layer copper wiring structure and performance comparison with aluminum on-chip interconnections," in *Tech. Dig. IEEE Int. Electron Devices Meeting*, 1998, pp. 295–298.
- [6] S. Takahashi, M. Eda, and Y. Hayashi, "Interconnect design strategy: Structures, repeaters and materials toward 0.1 μm ULSI's with a giga-hertz clock operation," in *Tech. Dig. IEEE Int. Electron Devices Meeting*, 1998, pp. 833–836.
- [7] R. Venkatesan, J. Davis, K. Bowman, and J. Meindl, "Optimal repeater insertion for n -tier multilevel interconnect," in *Tech. Dig. IEEE Int. Electron Devices Meeting*, 2000, pp. 132–134.
- [8] "Interconnect," in *Int. Tech. Roadmap for Semiconductors: International Sematech*, 2000, ch. 7.
- [9] "Overall roadmap technology characteristics," in *Int. Tech. Roadmap for Semiconductors: International Sematech*, 2000, ch. 1.
- [10] D. Edelstein, J. Heidenreich, R. Goldblatt, W. Cote, C. Uzoh, N. Lustig, P. Roper, T. McDevitt, W. Motsiff, A. Simon, J. Dukovic, R. Wachnik, H. Rathore, R. Schulz, L. Su, S. Luce, and J. Slattery, "Full copper wiring in a sub-0.25 μm CMOS ULSI technology," in *Tech. Dig. IEEE Int. Electron Devices Meeting*, 1997, pp. 773–776.
- [11] S. Venkatesan, A. V. Gelatos, V. Misra, B. Smithe, R. Islam, J. Cope, B. Wilson, D. Tuttle, R. Cardwell, S. Anderson, M. Angyal, R. Bajaj, C. Capasso, P. Crabtree, S. Das, J. Farkas, S. Filipiak, B. Fiordalice, M. Freeman, P. V. Gilbert, M. Herrick, A. Jain, H. Kawasaki, C. Kiing, J. Klein, T. Lii, K. Reid, T. Saarinen, C. Simpson, T. Sparks, P. Tsui, R. Venkatraman, D. Watts, E. J. Weitzman, R. Woodruff, I. Yang, N. Bhat, G. Hamilton, and Y. Yu, "A high performance 1.8 V, 0.20 μm CMOS technology with copper metallization," in *Tech. Dig. IEEE Int. Electron Devices Meeting*, 1997, pp. 769–772.
- [12] S. Crowder, S. Greco, H. Ng, E. Barth, K. Beyer, G. Biery, J. Connolly, C. DeWan, R. Ferguson, X. Chen, M. Hargrove, E. Nowak, P. McLaughlin, R. Purtell, R. Logan, J. Oberschmidt, A. Ray, D. Ryan, K. Tallman, T. Wagner, V. McGahay, E. Crabbe, P. Agnello, R. Goldblatt, L. Su, and B. Davari, "A 0.18 μm high-performance logic technology," in *Symp. VLSI Tech. Dig. Tech. Papers*, 1999, pp. 105–106.
- [13] R. D. Goldblatt, B. Agarwal, M. B. Anand, E. P. Barth, G. A. Biery, Z. G. Chen, S. Cohen, J. B. Connolly, A. Cowley, T. Dalton, S. K. Das, C. R. Davis, A. Deutsch, C. De Wan, D. C. Edelstein, P. A. Emmi, C. G. Faltermeier, J. A. Fitzsimmons, J. Hedrick, J. E. Heidenreich, C. K. Hu, J. P. Hummel, P. Jones, E. Kaltalioglu, B. E. Kastner, M. Krishnan, W. F. Landers, E. Liniger, J. Liu, N. E. Lustig, S. Malhotra, D. K. Manger, V. McGahay, R. Mih, H. A. Nye, S. Purushothaman, H. A. Rathore, S. C. Seo, T. M. Shaw, A. H. Simon, T. A. Spooner, M. Stetter, R. A. Wachnik, and J. G. Ryan, "A high performance 0.13 μm copper BEOL technology with low- k dielectric," in *Tech Dig. IEEE Int. Interconnect Tech. Conf.*, 2000, pp. 261–263.
- [14] Y. Takao, H. Kudo, J. Mitani, Y. Kotani, S. Yamaguchi, K. Yoshie, M. Kawano, T. Nagano, I. Yamamura, M. Uematsu, N. Nagashima, and S. Kadamura, "A 0.11 μm CMOS technology with copper and very-low- k interconnects for high-performance system-on-a-chip cores," in *Tech Dig. IEEE Int. Interconnect Tech. Conf.*, 2000, pp. 559–562.
- [15] K. K. Young, S. Y. Wu, C. C. Wu, C. H. Wang, C. T. Lin, J. Y. Cheng, M. Chiang, S. H. Chen, T. C. Lo, Y. S. Chen, J. H. Chen, L. J. Chen, S. Y. Hou, J. J. Liaw, T. E. Chang, C. S. Hou, J. Shih, S. M. Jeng, H. C. Hsieh, Y. Ku, T. Yen, H. Tao, L. C. Chao, S. Shue, S. M. Jang, T. C. Ong, C. H. Yu, M. S. Liang, C. H. Diaz, and J. Y. C. Sun, "A 0.13 μm CMOS technology with 193 nm lithography and Cu/low- k for high performance applications," in *Tech Dig. IEEE Int. Interconnect Tech. Conf.*, 2000, pp. 563–566.
- [16] S. Tyagi, M. Alavi, R. Bigwood, T. Bramblett, J. Brandenburg, W. Chen, B. Crew, M. Hussein, P. Jacob, C. Kenyon, C. Lo, B. McIntyre, Z. Ma, P. Moon, P. Nguyen, L. Rumaner, R. Schweinfurth, S. Sivakumar, M. Stettler, S. Thompson, B. Tufts, J. Xu, S. Yang, and M. Bohr, "A 130 nm generation logic technology featuring 70 nm transistors, dual V_T transistors and 6 layers of interconnects," in *Tech Dig. IEEE Int. Interconnect Tech. Conf.*, 2000, pp. 567–570.

- [17] A. Perera, B. Smith, N. Cave, M. Sureddin, S. Chheda, R. Singh, R. Islam, J. Chang, S.-C. Song, A. Sultan, S. Crown, V. Kolagunta, S. Shah, M. Celik, D. Wu, K. C. Yu, R. Fox, S. Park, C. Simpson, D. Eades, S. Gonzales, C. Thomas, J. Sturtevant, D. Bonser, N. Benavides, M. Thompson, V. Sheth, J. Fretwell, S. Kim, N. Ramani, K. Green, M. Moosa, P. Besser, Y. Solomentsev, D. Denning, M. Friedemann, B. Baker, R. Chowdhury, S. Ufmani, K. Strozewski, R. Carter, J. Reiss, M. Olivares, B. Ho, T. Lii, T. Sparks, T. Stephens, M. Schaller, C. Goldberg, K. Junker, D. Wristers, J. Alvis, B. Melnick, and S. Venkatesan, "A versatile 0.13 μm CMOS platform technology supporting high performance and low power applications," in *Tech Dig. IEEE Int. Interconnect Tech. Conf.*, 2000, pp. 571–574.
- [18] P. Fisher and R. Nesbitt, "The test of time. Clock-cycle estimation and test challenges for future microprocessors," *IEEE Circuits Devices Mag.*, pp. 37–44, Mar. 1998.
- [19] R. Ho and M. Horowitz, *Int. Tech. Roadmap for Semiconductors*, 1999, p. 165. Fig. 27 of Interconnect Chapter.
- [20] M.-F. Chou, W. L. Guthrie, and F. B. Kaufman, "Method of forming fine conductive lines, patterns and connectors," 4 702 792, Oct. 27, 1987.
- [21] D. T. Price and R. J. Gutmann, "Comparison of dual-damascene strategies for copper interconnects with polymer IMDs," in *Proc. Adv. Metallization Conf.*, 1998, pp. 653–659.
- [22] E. Zielinski, S. Russell, R. List, A. Wilson, C. Jin, K. Newton, J. Lu, T. Hurd, W. Hsu, V. Cordasco, M. Gopikanth, V. Korhuit, W. Lee, G. Cerny, N. Russell, P. Smith, S. O'Brien, and R. Havemann, "Damascene integration of copper and ultra-low- k xerogel for high performance interconnects," in *Tech. Dig. IEEE Int. Electron Devices Meeting*, 1997, pp. 936–938.
- [23] W.-Y. Shih, M.-C. Chang, R. H. Havemann, and J. Levine, "Implications and solutions for Joule heating in high performance interconnects incorporating low- k dielectrics," in *Symp. VLSI Tech. Dig. Tech. Papers*, 1997, pp. 83–84.
- [24] C. Jin, L. Ting, K. Taylor, T. Seha, and J. D. Luttmer, "Thermal conductivity measurements and low dielectric constant films," in *Proc. 2nd DUMIC*, 1996, p. 21.
- [25] C.-K. Hu, R. Rosenberg, H. S. Rathore, D. B. Nguyen, and B. Agarwala, "Scaling effect on electromigration in on-chip Cu wiring," in *Tech Dig. IEEE Int. Interconnect Tech. Conf.*, 1999, pp. 267–269.
- [26] T. S. Kuan, C. K. Inoki, G. S. Oehrlein, K. Rose, Y.-P. Zhao, G.-C. Wang, S. M. Rossnagel, and C. Cabral, "Fabrication and performance limits of sub-0.1 micrometer Cu interconnects," *Mat. Res. Soc. Symp. Proc.*, vol. 612, no. D7.1.1, 2000.
- [27] W. J. Daly and J. Poulton, "Transmitter equalization for 4-Gbps signaling," *IEEE Micro*, p. 48, Jan./Feb. 1997.
- [28] D. A. B. Miller, "On-chip and chip-to-chip optical interconnects—Status and prospects," in *Interconnect Technology Beyond the Roadmap*, K. C. Saraswat, Ed: SRC/SEMATECH/MARCO White Paper, May 22, 1999.
- [29] —, "Rationale and challenges for optical interconnects to electronic chips," *Proc. IEEE*, vol. 88, pp. 728–749, June 2000.
- [30] A. Krishnomoorthy, A. L. Lentine, K. W. Goossen, J. A. Walker, T. K. Woodward, J. E. Ford, G. F. Aplin, L. A. D'Asaro, S. P. Hui, B. Tseng, R. Leibenguth, D. D. Kossives, D. Dahringer, L. M. F. Chirovsky, and D. A. B. Miller, "3-D integration of MQW modulators over active submicron CMOS circuits: 375 Mb/s transimpedance receiver-transmitter circuit," *IEEE Photon. Technol. Lett.*, vol. 7, pp. 1288–1290, 1995.
- [31] B. A. Floyd and K. K. O, "The projected power consumption of a wireless clock distribution system and comparison to conventional systems," in *Tech Dig. IEEE Int. Interconnect Tech. Conf.*, San Francisco, CA, June 1999, pp. 248–251.
- [32] B. A. Floyd, K. Kim, and K. K. O, "Wireless interconnection in a CMOS IC with integrated antennas," *ISSCC Dig. Tech. Papers*, pp. 328–329, 2000.
- [33] M. F. Chang, "RF/Wireless interconnect for inter- and intra-chip communications," in *Interconnect Technology Beyond the Roadmap*, K. C. Saraswat, Ed: SRC/SEMATECH/MARCO White Paper, May 22, 1999.
- [34] M. F. Chang, V. Roychowdhury, L. Y. Zhang, S. Zhou, Z. Wang, Y. Wu, P. Ma, C. Lin, and Z. Kang, "Multi-I/O and reconfigurable RF/wireless interconnect based on near field capacitive coupling and multiple access techniques," in *Tech. Dig. IEEE Int. Interconnect Tech. Conf.*, 2000, pp. 21–22.
- [35] IBM, "SOI technology to boost IBM servers," *Electron. News*, May 29, 2000.
- [36] Q.-Y. Tong and U. Goesele, *Semiconductor Wafer Bonding: Science and Technology*. New York: Wiley, 1999.
- [37] —, "Wafer bonding and layer splitting for microsystems," *Adv. Mater.*, vol. 17, 1999.
- [38] S. Pae, T. Su, J. P. Denton, and G. W. Neudeck, "Multiple layers of silicon-on-insulator islands fabrication by selective epitaxial growth," *IEEE Electron Device Lett.*, vol. 20, pp. 194–196, May 1999.
- [39] G. W. Neudeck, S. Pae, J. P. Denton, and T.-c. Su, "Multiple layers of silicon-on-insulator (SOI) for nanostructure devices," *J. Vac. Sci. Technol. B*, vol. 17, pp. 994–998, May/June 1999.
- [40] A. Rahman, D. Antoniadis, and A. Agarwal, "Study of 3-D integration of high performance logic," in *SRC/SEMATECH/MARCO Workshop, Interconnects for Systems on a Chip*, Stanford Univ., May 22, 1999.
- [41] A. Rahman and R. Reif, "System-level performance evaluation of three-dimensional integrated circuits," *IEEE Trans. VLSI Syst.*, vol. 8, pp. 671–678, Dec. 2000.
- [42] W. J. Daly, "Interconnect-limited VLSI architecture," in *Tech Dig. IEEE Int. Interconnect Tech. Conf.*, 1999, pp. 15–17.

Robert (Bob) Havemann (Member, IEEE) received the B.S. and M.S. degrees in electrical engineering from Rice University, followed by a Ph.D. in electrical engineering from the University of Colorado in 1974.

He is currently Vice President of Research and Development at Novellus Systems, where his responsibilities include the development of novel process and equipment technologies for integrated circuit fabrication. Prior to joining Novellus, he enjoyed a long career at Texas

Instruments (TI), where as a TI Fellow he contributed to the development of numerous scaled device technologies including NMOS, bipolar, CMOS, BiCMOS and advanced interconnects. While at TI, he also recently completed an assignment at International Sematech as Program Manager for Interconnect Module Integration. He is a cofounder of the EDS supported International Interconnect Technology Conference (IITC), and served as General Chair for three years. He currently serves as local arrangements co-chair on the VLSI Technology Symposium committee. His professional contributions to date include 61 issued patents and over 100 publications in the field of microelectronics.

Dr. Havemann is a longstanding member of the AVS.

James A. Hutchby (Member, IEEE) received the Bachelor of electrical engineering degree from Auburn University in 1964, and the Master of electrical engineering and Ph.D. in electrical engineering degrees in 1966 and 1969, respectively.

He is currently Director of Nanostructure and Integration Sciences with the Semiconductor Research Corporation. In this position he is supporting university programs addressing Advanced Devices and Technologies (ADT),

Packaging and Interconnect and Factory Sciences issues. Activities in ADT comprehend research in both advanced and traditional CMOS structures and technologies, modeling and simulation programs, and novel device programs. Activities in Packaging and Interconnect (PI) comprehend materials, systems and modeling/simulation work related to a variety of new ball grid array flip chip packaging technologies. The PI research also includes new systems and strategies for providing global interconnect (inter and intra-chip) of clock, signal, power and ground. The Factory Sciences activities are focused on factory operations modeling and simulation. Prior to joining SRC, he was the Director of the Center for Semiconductor Research (CSR) at the Research Triangle Institute. He has served as the General Chair and Technical Program Chair of numerous conferences, including the IEEE IEDM, GaAs IC Symposium, and the Workshop on Compound Semiconductor Materials and Devices. He has also served on the program committees in various capacities on the IEEE Cornell Advanced Microelectronics Conference, International GaAs Manufacturing Technology Conference, and the IEEE Photovoltaics Conference. He has published over 100 contributed and invited papers in scientific journals and conferences, and was a member of the IEEE Electron Devices Society Advisory Committee for two terms (six years).

Dr. Hutchby recently received the IEEE Third Millennium Medal.