Integrated circuit isolation technologies

Illustration of various leakage paths and corresponding design rules to be considered when designing an isolation structure

Isolation pitch trends

![Graph showing isolation pitch trends](image)

P. Fazan, Micron, IEDM-93

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<tbody>
<tr>
<td>DRAM pitch (nm)</td>
<td>360</td>
<td>260</td>
<td>200</td>
<td>140</td>
<td>100</td>
<td>70</td>
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<tr>
<td>Minimum MPU Feature Size (nm)</td>
<td>140</td>
<td>85</td>
<td>65</td>
<td>45</td>
<td>30</td>
<td>20</td>
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ITRS Projections for the future

With decreasing feature size the requirement on allowed isolation area becomes stringent.
Isolation Techniques

- Diffusion isolation with reverse biased diodes.
  - Historically used for bipolar
  - Currently used to isolate NMOS from PMOS through a well

- Oxide isolation
  - Used in early days of MOS
  - Field can't be implanted for parasitic transistor \( V_t \) control
  - Step height is too much
• Local oxidation of silicon (LOCOS)
  - Main method used today in a variety of forms e.g., semi-recessed LOCOS, fully-recessed LOCOS, SWAMI, poly-buffered LOCOS.

  Grow $\text{SiO}_2$, deposit $\text{Si}_3\text{N}_4$

  Pattern, Field implant

  Grow field oxide

  Strip nitride, pad-oxide

  Local Oxidation of Silicon (LOCOS) process sequence

  - 0.6 $\mu$m pitch: LOCOS limit if thick (>300 nm) field oxides are required. 0.4 $\mu$m pitch with recessed LOCOS (200 nm field oxide) has been demonstrated (K. Shibahara et al. IEDM-94, p. 639). Below these dimensions LOCOS based technology may not be used.

• Trench isolation
  - Cutting edge technology today
**Fully-recessed and semi-recessed LOCOS**

![Diagram of LOCOS structures](image)

Illustration of the difference in shape and topography in a semi-recessed and fully-recessed LOCOS structure obtained by etching Si prior to oxidation.

![TEM image](image)

**TEM of Conventional semi-recessed LOCOS**
2D effects in thermal oxidation of Si


Typical experimental result from Kao, et.al. Silicon wafers were plasma etched to produce a variety of shaped structures including the cylinder illustrated in the top drawing. These structures were oxidized and the oxide thickness was measured. The drawing at the right labels the structure shown experimentally on the left. The oxide is thinner on both concave and convex corners than it is on flat regions.
Typical experimental data after Kao. The oxide thickness is plotted versus the radius of curvature of the structure being oxidized. For each temperature, about 500 nm of oxide was grown on a flat surface ($1/r = 0$). These results are for $\text{H}_2\text{O}$ oxidations. Similar results were found for $\text{O}_2$. Note the retardation of the oxidation for sharp corners (more than a factor of 2 in some cases).

Several physical mechanisms are important in understanding these results.

**2D Oxidant Diffusion:**
In corner regions and other shaped structures, oxidant transport to the Si/\text{SiO}_2 interface is a 2D or perhaps even 3D transport problem. Since the oxide is amorphous, the diffusion coefficients of $\text{O}_2$ or $\text{H}_2\text{O}$ should not be direction dependent, but numerical techniques are generally required to solve the diffusion equation in multiple dimensions.

Diffusion of oxidants in cylindrical structures. (a) shows the convex surface of a Si cylinder during oxidation. Because of the wider exposure to the ambient, the concentration of the oxidant is higher in the convex case than it is for a flat surface. The opposite is true for the concave surface, such as a hole etched in the silicon as shown in (b).
Isolation

- Expected oxide thickness convex > planar > concave
- Experiment shows planar > convex > concave
- 2-D Diffusion alone can't explain the thinning effects at both concave and convex shaped corners, although it does play some role in it.

**Stress due to volume expansion:**
Oxide layers formed on silicon are under significant compressive stress. This stress is due to the volume expansion that takes place during oxidation and to the difference in thermal expansion coefficients of Si and SiO$_2$ which causes additional stress when the wafers are cooled from the oxidation temperature back to room temperature. On shaped silicon surfaces, these stresses can be much larger than they would be on a flat surface simply because the volume expansion is dimensionally confined on shaped structures. Such stresses could in principle affect both oxidant transport through the SiO$_2$ and the interface reaction at the Si/SiO$_2$ interface.

New oxide growth at the interface pushes out the old oxide. The incompressibility of the oxide dictates that the volume of the old oxide be conserved during the viscous deformation.
Stress Effects from Non Planar Deformation

There is a normal stress for both convex and concave surfaces; in the bulk of the oxide. The pressure, is tensile for the convex structure in (a) and compressive for the concave structure in (b).

To model these stress effects, Kao et. al. suggested the following modifications to the parameters usually used in the linear parabolic model.

\[
k_S(\text{stress}) = k_S \exp\left(-\frac{\sigma_n V_R}{kT}\right) \exp\left(-\frac{\sigma_t V_T}{kT}\right)
\]

\[
D(\text{stress}) = D \exp\left(-\frac{(P)(V_D)}{kT}\right)
\]

\[
C^*(\text{stress}) = C^* \exp\left(-\frac{(P)(V_S)}{kT}\right)
\]

where \(k_S\) is the normal interface reaction rate, \(\sigma_n\) is the stress normal to the growing interface, \(\sigma_t\) is the stress tangential to the growing interface, \(D\) is the normal oxidant diffusivity (at 1 Atm), \(C^*\) is the normal oxidant solubility and \(P\) is the hydrostatic pressure in the growing oxide. \(V_R, V_T, V_D\) and \(V_S\) are considered to be stress dependent activation volumes and should be regarded as fitting parameters. They are used in the SUPREM IV implementation of this model.

The final oxide parameter that is needed to calculate growth on shaped surfaces, is the oxide viscosity. \(\text{SiO}_2\) is a glass and can relax some of the stresses that build up during oxidation by viscoelastic flow. In fact, the stresses that can build up during oxidation are so large, that the oxide viscosity itself needs to be modeled as a function of stress. A relationship of the following form has been found to produce good agreement with experiment

\[
\eta(\text{stress}) = \eta(T) \frac{\sigma_S V_C / 2kT}{\sinh(\sigma_S V_C / 2kT)}
\]

where \(\eta(T)\) is the stress free, temperature dependent, oxide viscosity, \(\sigma_S\) is the shear stress in the oxide, and \(V_C\) is again a fitting parameter.
Viscosity vs. temperature for oxide grown in H$_2$O. (Ref: Kao, et al.)

- Viscosity is a function of oxide growth temperature, oxidation ambient and stress
- Appreciable viscous flow above ~ 950°C
- Viscous flow results in stress reduction and hence influences the shape of LOCOS structures

**Idealized LOCOS structure**

Recessed LOCOS process in which the silicon is etched prior to LOCOS to produce a final planar surface. The "bird's beak" produced at the boundaries of such structures is not illustrated here.
Realistic LOCOS structure

Simulation of a recessed LOCOS isolation structure using the ATHENA simulator. The initial structure (top left) is formed by depositing a $\text{SiO}_2/\text{Si}_3\text{N}_4$ structure followed by etching of this stack on the left side. The silicon is then etched to form a recessed oxide and the structure is oxidized for 90 min at 1000°C in $\text{H}_2\text{O}$. The time evolution of the bird’s head shape during the oxidation is shown in the simulations. (Ref: Plummer’s book)

**LOCOS structure parameters dependence on process parameters**

Parameters describing the bird’s beak in a semi-recessed LOCOS and the bird’s beak and bird’s head in a fully recessed LOCOS structure.
Bird’s beak length dependence on nitride and pad oxide thickness in a semi-recessed LOCOS. The field oxide was grown at 1000°C to a thickness of approximately 600nm.

Bird’s beak height dependence on nitride and pad oxide thickness in a semi-recessed LOCOS. The field oxide was grown at 1000°C to a thickness of approximately 600nm.
**Problems in scaling of LOCOS type isolation structures**

The Kooi or “white ribbon” effect is due to the nitridation of the silicon surface under the nitride mask edge. This can result in local thinning of gate oxide. The local nitride can be removed by additional oxidation and etch.

**Forces in Local Oxidation of Silicon**

Simulated LOCOS structures with contours of constant compressive stress (0, 10, 50, 100, and 500 MPa). No recess, 100 nm nitride

Simulated LOCOS structures with contours of constant compressive stress (0, 10, 50, 100, and 500 MPa). 150 nm recess, 200 nm nitride
Average compressive stress in edge region along <111> for the different LOCOS isolation structures.

Stress ↑ as  
- nitride thickness ↑
- recess thickness ↑
- pad oxide thickness ↓
- oxidation temperature ↓

Example of an oxidation simulation showing the effects of including stress effects in oxidation using the ATHENA simulator. A 20 nm SiO₂ pad oxide is first grown and a 150 nm Si₃N₄ layer is then deposited. The nitride is then etched on the left side of each structure. A 90 minute 1000°C H₂O oxidation was then performed. In the simulation on the left, no stress dependent parameters
were included in the simulation. Stress dependent parameters were included in the simulation on the right. (Ref: Plummer’s Book)

**Effect of stress on physical and electrical properties**

**Band gap narrowing**
When a crystal is mechanically deformed, the crystal symmetry and the lattice spacings are altered and hence the energy bands change. The change in band gap can cause change in intrinsic carrier concentration. This can result in increased junction leakage.

**Crystal defect formation**
If the stress exceeds the yield stress, defects can form resulting in further increase in leakage.

Calculated influence of a pure hydrostatic and a uniaxial compressive stress along a <111> direction on the intrinsic carrier concentration.
Perimeter generation current as a function of compressive “elastic” stress near the LOCOS edge in gated diodes.

Field oxide thinning with scaling

Scanning electron microscope of the field oxide thinning problem. A conventional LOCOS structure with 10 nm pad oxide and 150 nm nitride was used in this experiment. The field oxidation was carried out in steam at 1000 °C for 70 sec.
Relative amount of field oxide thinning for a conventional LOCOS structure (10nm pad oxide and 150 nm nitride) and a PBL (10 nm pad oxide, 50 nm poly and 150 nm nitride) structure. Field oxidation was done in a steam ambient at 1000 °C for 70’.

**Pad oxide punchthrough and end-of-line encroachment**

SEM micrographs of LOCOS structures after nitride removal and pad oxide etch, showing the silicon substrate (black area) and the extent of the bird’s beak in the length and width direction of the mask.
SUPREM-IV simulation of the oxidant concentration at the SiO2-Si interface of a LOCOS structure as a function of oxidation temperature. The simulated LOCOS structure consisted of a 15 nm pad oxide and 154 nm nitride. The final field oxide thickness was approximately 350nm in all cases.

**Advanced LOCOS Techniques**

To minimize the problems of the conventional LOCOS techniques several advanced LOCOS techniques have been developed.

Schematic representation of the poly buffered LOCOS isolation structure, before and after field oxidation.
Simulation of an advanced isolation structure (the SWAMI process originally developed by Hewlett-Packard), using the ATHENA simulator. The structure prior to oxidation is on the top left. This structure is formed by depositing an oxide followed by a thick Si$_3$N$_4$ layer, both of which are etched away on the left side. A silicon etch on the left side is then followed by a second oxide and nitride deposition. These layers are then etched away on the far left side, leaving the thin SiO$_2$/Si$_3$N$_4$ stack covering the sidewall of the silicon. A 450 min H$_2$O oxidation at 1000°C is then performed which results in the structure on the top right. An experimental structure fabricated with a similar process flow is shown on the bottom right. The stress levels in the SiO$_2$ are shown at the end of the oxidation on the bottom left.

(a) Nitride or poly spacer

(b) Nitride or polysilicon

Schematic representation of nitride or poly spacer LOCOS (a) and Nitride-Clad or PELOX (b) before field oxidation
Schematic representation of the shallow and deep trench structures for inter-device and inter-well isolation respectively. After etching and re-oxidizing the trench sidewalls, they are filled with a deposited dielectric and planarized.

Fabrication sequence of shallow trench isolation (STI):

1. Silicon Etch
   - Photore sist
   - Silicon Nitride

2. Thermal Oxidation

3. Oxide Fill
   - Oxide

4. Planarization
Oxide Fill for Trench Isolation

PECVD

- Poor gap fill (key hole)
- Anisotropic properties of SiO$_2$
- Needs high T anneal to improve properties
- High T anneal increases stress

High Density Plasma CVD

- Excellent gap fill (no key hole)
- Isotropic excellent properties of SiO$_2$
- No anneal needed
Chemical-Mechanical Polishing (CMP) for Planarization

CMP Equipment

Close-up of wafer/pad interface:

After ECR CVD oxide deposition

After CMP
Effect of post thermal processing

Stress due to anneal
An anneal is generally done after deposition of the oxide in the trench to improve the quality of the oxide and the oxide/silicon interface. This anneal grows a thin film of oxide at the oxide/silicon interface. The new oxide induces stress.

First order model description of strain generation in STI structures due to oxidation.
Compressive stress in the silicon mesa as a function of active area length, $L_{Si}$, oxide thickness (5, 10, 15, 20 nm) and oxidation temperature. The STI length, $L_{SiO_2}$, was 0.18 $\mu$m in all cases.

Compressive stress in the silicon mesa as a function of active area (mesa) and STI length for an oxide of 10 nm grown at 1000 °C.
Pisces simulations of diode leakage current as a function of uniform compressive stress along the x direction. A slowly decaying stress with depth is assumed in this case (decay length of 10 micron).
Stress-induced leakage increase, normalized to the stress free current as a function of STI active device pitch and reoxidation temperature. Lower temperatures will result in higher stress and almost certainly lead to defect formation in scaled STI structures.

Leakage current per cell as a function of DRAM generation. To reduce power requirements associated with refreshing data, long retention times (64-250 mSec.) necessitate lower leakage currents (S. Asai, Hitachi)
Requirements for trench etching

Sharp corners
High E field
High leakage

Rounded corners
Lower E field
Lower leakage

Rounded corners require
- better dry etching and
- higher temperature thermal oxidation.

higher temperature thermal oxidation reduces the stress and gives more rounded corners. Both these effects reduce the leakage.
TSUPREM Simulations of stress for 1000°C and 1075°C


(left) 50 nm wide MOSFETs isolated by 200 nm-wide polysilicon-filled trenches (right) 100 nm wide MOSFETs isolated by 200 nm-wide SiO₂-filled trench (Ref: Krucias, et al. Cornell Univ.)