Interconnections: Silicidesc

1. Source/Drain Junctions

\[ R_{\text{total}} = R_{\text{ch}} + R_{\text{parasitic}} \]
\[ R_{\text{parasitic}} = R_{\text{extension}} + R_{\text{extrinsic}} \]
\[ R_{\text{extension}} = R_{d'} + R_{s'} \]
\[ R_{\text{extrinsic}} = R_d + R_s + 2R_c \]

2. MOS Gate Electrode

As channel length is scaled, gate resistance increases. Gate electrode is also used as an interconnect layer in many applications. As channel length is scaled, gate resistance increases.
To minimize parasitic resistance we use silicide for:

1. Polycide gate (silicide on polysilicon)
2. Salicide (self aligned silicide) on source-drain
3. Local interconnection between devices, e.g., between source/drain diffusion of one device to gate of another in a SRAM cell.

Why use silicides?

- Low resistance
- Good process compatibility with Si, e.g., ability to withstand high temperatures, oxidizing ambients, various chemical cleans used during processing.
- Little or no electromigration
- Easy to dry etch
- Good contacts to other materials.

But these are many problems in integrating silicides in an IC as we will see later in this chapter.

Properties of silicides

Preferred silicides for the applications outlined earlier are WSi$_2$, TiSi$_2$, NiSi and CoSi$_2$ because of their overall excellent properties.
<table>
<thead>
<tr>
<th>Silicide</th>
<th>Thin film resistivity (µΩcm)</th>
<th>Sintering temp (°C)</th>
<th>Stable on Si up to (°C)</th>
<th>Reaction with Al at (°C)</th>
<th>nm of Si consumed per nm of metal</th>
<th>nm of resulting silicide per nm of metal</th>
<th>Barrier height to n-Si (eV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PtSi</td>
<td>28-35</td>
<td>250-400</td>
<td>~750</td>
<td>250</td>
<td>1.12</td>
<td>1.97</td>
<td>0.84</td>
</tr>
<tr>
<td>TiSi₂ (C54)</td>
<td>13-16</td>
<td>700-900</td>
<td>~900</td>
<td>450</td>
<td>2.27</td>
<td>2.51</td>
<td>0.58</td>
</tr>
<tr>
<td>TiSi₂ (C49)</td>
<td>60-70</td>
<td>500-700</td>
<td></td>
<td></td>
<td>2.27</td>
<td>2.51</td>
<td></td>
</tr>
<tr>
<td>Co₂Si</td>
<td>~70</td>
<td>300-500</td>
<td></td>
<td></td>
<td>0.91</td>
<td>1.47</td>
<td></td>
</tr>
<tr>
<td>CoSi</td>
<td>100-150</td>
<td>400-600</td>
<td></td>
<td></td>
<td>1.82</td>
<td>2.02</td>
<td></td>
</tr>
<tr>
<td>CoSi₂</td>
<td>14-20</td>
<td>600-800</td>
<td>~950</td>
<td>400</td>
<td>3.64</td>
<td>3.52</td>
<td>0.65</td>
</tr>
<tr>
<td>NiSi</td>
<td>14-20</td>
<td>400-600</td>
<td>~650</td>
<td></td>
<td>1.83</td>
<td>2.34</td>
<td></td>
</tr>
<tr>
<td>NiSi₂</td>
<td>40-50</td>
<td>600-800</td>
<td></td>
<td></td>
<td>3.65</td>
<td>3.63</td>
<td>0.66</td>
</tr>
<tr>
<td>WSi₂</td>
<td>30-70</td>
<td>1000</td>
<td>~1000</td>
<td>500</td>
<td>2.53</td>
<td>2.58</td>
<td>0.67</td>
</tr>
<tr>
<td>MoSi₂</td>
<td>40-100</td>
<td>800-1000</td>
<td>~1000</td>
<td>500</td>
<td>2.56</td>
<td>2.59</td>
<td>0.64</td>
</tr>
<tr>
<td>TaSi₂</td>
<td>35-55</td>
<td>800-1000</td>
<td>~1000</td>
<td>500</td>
<td>2.21</td>
<td>2.41</td>
<td>0.59</td>
</tr>
</tbody>
</table>

### Ternary Phase Diagrams

Ternary Phase Diagrams are good indicators of stability. Existence of a *tie line* indicates that the system is stable and a reaction will not take place.
Silicide Formation Techniques

1. Metal deposition on Si and formation by thermal heating, laser irradiation or ion beam mixing.
   - Sensitive to interface cleanliness and heavy doping
   - Selective silicidation on Si possible
   - Widely used for silicides of Pt, Pd, Co, Ti

Salicide (self-aligned silicide) process

Simultaneous silicidation of polysilicon gate, source and drain regions. TiSi$_2$ is extensively used for this process. NiSi and CoSi$_2$ are beginning to be used.
2. Co-evaporation (E-gun) of metal and Si

- Poor process control
- Poor step coverage
- Good tool for research but not used in manufacturing

3. Sputtering from a composite target

- Possibility of high level of contaminants (C, O, Na, Ar)
- Poor step coverage
- Used for MoSi$_2$ and WSi$_2$
4. Cosputtering from two targets of metal and Si

- Poor step coverage
- Questionable process control
- Good tool for research but not used in manufacturing

5. CVD

- Good process control for manufacturability
- Clean microcrystalline films with excellent step coverage
- Available for only WSi$_2$
Effect of Thermal Processing on Silicide properties

In all the silicide formation schemes detailed above, it is usually necessary to subject the silicide to further thermal processing, either to form the silicide or enhance the grain size. In particular, for CVD and deposited silicides (as opposed to thermally formed silicides), grain size can be enhanced substantially by annealing.

![TEM of WSi_2 films as deposited by CVD and after annealing](image)


This example is for CVD WSi_2 but is applicable to other silicides.
- As deposited films are amorphous or microcrystalline
- Upon annealing grains grow
- Higher temperature and longer time give bigger grains
- Possible phase change

Effect of Annealing on Resistivity
- As deposited films have high resistivity because they are amorphous or microcrystalline and therefore carrier mobility is low
- Upon annealing grains grow and therefore resistivity decreases
- Higher temperature and longer time give bigger grains and thus lower resistivity
  \[\Rightarrow\] correlation with grain growth
Resistivity of $WSi_2$ films as deposited by CVD and after annealing.


Physical Stress in Silicides

Annealing may result in substantial stress in the silicide. In addition, there may also be internal stress in the silicide due to the deposition conditions. Since silicides are typically close to junctions, and mechanical stress has been found to alter electrical properties of devices, an examination of this issue is important. Stress may be caused by:

- Internal stress controlled by deposition parameters
- Difference in thermal expansion rates of Si and silicide
- Contaminants in silicide
- Structure and composition of the silicide film

- Stress in polycide gates can cause gate shorts, cracks, lifting
- Need a buffer layer of poly-Si to maintain reliability
Stress can be minimized by making Si rich silicide films.

Stress can be generated due to structural changes.
Effect of Contaminants

Contamination severely changes the properties of silicides. An effect of oxygen contamination on the properties of TaSi$_2$ films is shown below.

Electrical resistivity $\rho$, stress $\Delta\sigma_{\text{dep}}$ after deposition, stress change $\Delta\sigma_{\text{sint}}$ during sintering and etch rate $R_{\text{etch}}$ in CF$_4$ of evaporated TaSi$_2$ films as a function of increasing O$_2$ partial pressure in the residual gas. All values are normalized to those obtained without additional O$_2$, marked with a suffix “0”.
Thermal Oxidation of Silicides

During fabrication the silicides are exposed to thermal oxidation. It is very important that they be able to withstand oxidation steps without deterioration in their properties.

\[
\text{Si} + O_2 \rightarrow \text{SiO}_2
\]

- Diffusion of Si should be established before starting oxidation.
- Contaminants reduce Si diffusivity.

\[
\text{MSi}_2 + O_2 \rightarrow M_xO_y + \text{SiO}_2
\]

Oxides of Mo and W are volatile. Ta and Ti react with underlying SiO\textsubscript{2}.

C can stabilize metal rich phases (W\textsubscript{5}Si\textsubscript{3}, Mo\textsubscript{5}Si\textsubscript{3}).

\[
\text{WSi}_2 + O_2 \rightarrow \text{SiO}_2 + W_5\text{Si}_3
\]
All silicides show similar oxidation rates
• Silicides oxidize faster than Si

**Oxidation Rate Constants**

The mechanism of oxidation can be easily understood using Deal-Grove type oxidation model commonly used for Si:

$$\frac{X_0^2}{B} + \frac{X_0}{B/A} = t + \tau$$

By fitting the oxidation data to the Deal-Grove equation the linear and parabolic rate constants, B/A and B, respectively, can be calculated.
Parabolic rate constant B is about the same as for Si. Linear rate constant B/A is much higher than for Si. This can be understood by studying oxidation kinetics.

\[
\frac{X_0^2}{B} + \frac{X_0}{B/A} = t + \tau
\]

\[
B = 2 \cdot C^* \cdot \frac{D_{ox}}{N_1}
\]

\[
\frac{B}{A} = \frac{C^*}{N_1} \left( \frac{1}{h} + \frac{C^* \cdot \Delta x}{k^* \cdot D_{Si}} + \frac{1}{k_1 \cdot k^*} \right)
\]

If \( D_{Si} \) is large, then this reduces to:

\[
\frac{B}{A} = \frac{C^* \cdot k_1 \cdot k^*}{N_1}
\]
k* is partition coefficient of Si between Si and MSi

C* is concentration of oxidant in SiO

C₀ is concentration of oxidant at SiO₂ surface

D_{ox} is diffusivity of oxidant in SiO₂ = 5E-10 cm²/sec for H₂O and 5E-9 cm²/sec for O₂

D_{si} is diffusivity of Si and MSi = 1E-7 cm²/sec.

⇒ D_{si} is much higher than D_{ox}

⇒ Rate limiting step is diffusivity of oxidant in SiO₂, therefore B is the same as that for oxidation of Si

⇒ B/A is much higher for silicides because it is easier to break a Si bond at the silicide/Si interface than at the Si/Si interface

Dopant Redistribution in Silicide/Silicon

Silicides are polycrystalline by nature with large density of grain boundaries. There are a large number of defects in grain boundaries. As a result the diffusity in silicides is very high. Dopant from Si can readily redistribute into a silicide.
In a polycide structure the outdiffusion of dopant from source/drain region to the silicide causes reduction in surface doping density leading to increase in contact resistance.

**ISSUES**
- Dopant diffusion in silicide and silicon
- Segregation at interfaces and grain boundaries
- Solubility in silicide and silicon
- Compound formation and precipitation

**Effect of Dopant Redistribution/Diffusion at the Polycide Gate Silicide/Si Interface ⇒ Change in Poly-Si Gate Workfunction**
Dopant originally in poly-Si redistributes into the silicide. This changes the gate Fermi level. The change in workfunction leads to change in $V_T$ shift.

Measurement of Diffusity in Silicides

Since the diffusity in silicides is very high it is very difficult to measure a vertical dopant profile in a thin film of silicide as the dopant readily redistributes into a homogeneous profile. At normal temperatures the diffusion distance is tens of microns. It is possible to obtain a lateral profile in a thin film but is difficult to measure it. In the test structure shown below the presence of the dopant at the silicide/Si interface can be detected by observing the transition from Schottky to Ohmic. By varying the silicide arm length and estimate doping at the end of the arm by measuring I-V characteristics the diffusion extent can be measured.

$$N(x,t) = N_0 \text{erfc} \left( \frac{x}{2\sqrt{Dt}} \right)$$
As N increases, the barrier height decreases and the effective barrier thickness decreases. This results in a net increase in total current. Hence the current is function of the doping density, and the dopant diffusion can be monitored electrically. Current in a Schottky contact is very sensitive to doping density. Therefore arrival of the dopant from the reservoir can be precisely detected. Using the constant source diffusion equation the diffusivity can be calculated.
\[ N(x, t) = N_0 \text{erfc} \left( \frac{x}{2\sqrt{Dt}} \right) \]

Where \( N_0 \) is the dopant concentration in the reservoir and \( x \) is the lateral distance from the reservoir. Knowing the arm length, it is therefore possible to determine the doping from the current.


These values are MUCH higher than those in Si. Dopants diffusion in polycrystalline silicides is:
- 5 - 6 orders of magnitude higher than in single crystal silicon
- 3 - 4 orders of magnitude higher than in polycrystalline silicon

PROBLEMS:
- \( \text{N}^+/\text{P}^+ \) spacing as the dopant can intermix
- Contact resistance can change
- \( V_T \) shift can occur

**Problem with Salicide Technology: TiSi\textsubscript{2} Scalability**

**Trends in Salicide Technology**

In the last two handouts, we studied about two important technologies – shallow junctions and contacts. As identified in the latter, self-aligned silicides (salicides) are used for reducing the parasitic resistances associated with shallow source / drain junction. Continued scaling of MOS devices has resulted in the need for advances in silicide technology as well. In this section technological trends in salicides are reviewed.

**P-N Junction Currents Modified Due to Metal Induced Traps**
Unfortunately, metals used in silicides form trap locations fairly deep within the Si bandgap making them rather efficient generation – recombination centers. For example, from your EE216 notes, you know.

<table>
<thead>
<tr>
<th>Impurity</th>
<th>Level(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ti</td>
<td>E_c-0.21, E_v+0.34</td>
</tr>
<tr>
<td>Pt</td>
<td>E_c-0.25, E_v+0.3, E_v+0.36</td>
</tr>
<tr>
<td>Pd</td>
<td>E_v+0.34</td>
</tr>
</tbody>
</table>

One of the interesting implications of this is that leakage current increases as the trap moves close to midgap. This is why the refractory metals typically used in silicides tend to cause degradation in leakage current; they are much closer to the midgap than typical dopants such as B and As.

Thus, all these traps are reasonably active, and result in a substantial leakage current in reverse-biased diodes. We can perform a simple analysis based on first principles to illustrate this:

**Implications of silicide scaling**

**Silicon consumption and shallow junctions – the driving force for evolution in salicide technology**

The dominant salicides in use today are TiSi₂ and CoSi₂. For commercial quarter-micron devices, with junction depths of approximately 200nm, these work quite well, though there is in fact some junction leakage associated with the use of these salicides. However, as junctions are scaled further, Ti and Co salicides become impractical.
To understand why this is the case, we first need to consider the effect of silicide encroachment into the junction.

<table>
<thead>
<tr>
<th>Silicide</th>
<th>Si consumed per nm of metal (nm)</th>
<th>Resulting silicide per nm of metal (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TiSi$_2$ (C54)</td>
<td>2.27</td>
<td>2.51</td>
</tr>
<tr>
<td>CoSi$_2$</td>
<td>3.64</td>
<td>3.52</td>
</tr>
<tr>
<td>NiSi</td>
<td>1.83</td>
<td>2.34</td>
</tr>
</tbody>
</table>

Metallic for salicide formation are almost always sputtered. Technological limitations restrict the minimum film thickness for most sputtered films to approximately 20-30nm. Now, the different silicides have different silicon consumption ratios.

This represents an absolute minimum on junction depth. An additional buffer is typically required due to the spiking that extends far below the silicide interface. To make shallower junctions, therefore, it is necessary to use a silicide with a lower silicon consumption ratio, i.e. Ni silicide.

**Linewidth scaling: another driving force for technological evolution of salicides**

**Titanium Silicide**

Titanium salicide was the dominant salicide technology for many years. As devices were scaled into the deep-submicron regime, however, a new limitation of the use of TiSi$_2$ emerged. Low resistance TiSi$_2$ is formed through a phase transformation from C49 (60-90 $\mu\Omega$-cm) to C54 (14-18 $\mu\Omega$-cm). Unfortunately, this transformation becomes extremely difficult for thin lines, and hence, this Ti lines have higher resistances than desirable.

This problem is essentially unique to TiSi$_2$; linewidth effects in other silicides are much less dramatic. Therefore, this was the driving force for the transition from Ti to Co, despite the fact that Co has a higher Si consumption ratio.
Titanium silicide is probably still the most widely used silicide. Since it suffers from linewidth effects and has a relatively high silicon consumption ratio, it is losing favor for deep-submicron applications.

<table>
<thead>
<tr>
<th>Silicide</th>
<th>Thin film resistivity ($\mu\Omega$cm)</th>
<th>Si consumed per nm of metal (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TiSi$_2$ (C54)</td>
<td>13-16</td>
<td>2.27</td>
</tr>
<tr>
<td>TiSi$_2$ (C49)</td>
<td>60-70</td>
<td>2.27</td>
</tr>
</tbody>
</table>

**Cobalt Silicide**

Cobalt silicide is currently very popular as a replacement for Ti salicide, as it has lower temperature requirement and doesn’t suffer from linewidth effects significantly. Unfortunately, its Si consumption ratio is similar to that of Ti, and it also has worse thermal stability. By adding a cap of Ti, however, the stability can be improved, and this is therefore a common implementation technology.

**Nickel Silicide**

Nickel Silicide is currently being researched extensively as a replacement for current silicides due to its lower Si consumption ratio and processing temperatures. Unfortunately, it has poor stability above 700°C. This may restrict its use to processes with low back-end temperature excursions. With the advent of low-K dielectrics, however, this may not be an issue.
**Transport Mechanism in Silicide Formation**

![Silicide formation reaction at top](image)

- If silicon is dominant diffuser, lateral encroachment of the silicide over the oxide spacer can occur causing bridging.

- A barrier needs to be created over the spacer

**How to Avoid Bridging**

- Anneal in an inert ambient
- Only TiSi₂ formation
Salicide process with TiN as a local interconnect

• Anneal in an ambient containing nitrogen
• Simultaneous formation of TiSi₂ and TiN
• TiN acts as a barrier to Si diffusion over the spacer

Salicide process to obtain:
1. TiSi₂ on top of polysilicon gate
2. TiSi₂ on top of source and drain
3. TiN as a local interconnect.