Stanford EE380
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Title: Title: The Future of Hardware Technologies for Computing: N3XT 3D MOSAIC, Illusion Scaleup, Co-Design

Abstract:
The computation demands of 21st-century abundant-data applications (e.g., AI/Machine Learning) far exceed the capabilities of today's computing systems. For example, a Dream AI Chip would ideally co-locate all memory and compute on a single chip, quickly accessible at low energy. Such Dream Chips aren't realizable today. Computing systems instead use large off-chip memory and spend enormous time and energy shuttling data back-and-forth.

The next leap in computing performance requires the next leap in integration. Just as integrated circuits brought together discrete components, this next level of integration must seamlessly fuse disparate parts of a system – e.g., compute, memory, inter-chip connections – synergistically for large energy and execution time benefits. We present this vision through transformative NanoSystems realized using ultra-dense (e.g., monolithic) 3D integration of logic and memory – the N3XT approach. To scale with growing problem sizes, new Illusion systems orchestrate multiple N3XT 3D chips -- the N3XT 3D MOSAIC -- creating an illusion of a Dream Chip with near-Dream energy and throughput. Beyond existing cloud-based training, we demonstrate the first non-volatile chips for accurate edge AI training (and inference) through new incremental training algorithms that are aware of underlying non-volatile memory technology constraints. Several hardware prototypes demonstrate the large benefits of such NanoSystems. These results represent collaborative work by multiple faculty, student, and research collaborators worldwide.

Biography:
Subhasish Mitra is Professor of Electrical Engineering and of Computer Science at Stanford University. He directs the Stanford Robust Systems Group, leads the Computation Focus Area of the Stanford SystemX Alliance, and is a member of the Wu Tsai Neurosciences Institute. His research ranges across Robust Computing, NanoSystems, Electronic Design Automation (EDA), and Neurosciences. Results from his research group have influenced almost every contemporary electronic system, and have inspired significant government and research initiatives in multiple countries. He has held several international academic appointments — the Carnot Chair of Excellence in NanoSystems at CEA-LETI in France, Invited Professor at EPFL in Switzerland, and Visiting Professor at the University of Tokyo in Japan. Prof. Mitra also has consulted for major technology companies including Cisco, Google, Intel, Samsung, and Xilinx.

In the field of Robust Computing, he has created many key approaches for circuit failure prediction, on-line diagnostics, QED system validation, soft error resilience, and X-Compact test compression. Their adoption by industry is growing rapidly, in markets ranging from cloud computing to automotive systems. His X-Compact approach has proven essential for cost-effective manufacturing and high-quality testing of almost all 21st century systems, enabling billions of dollars in cost savings.

With his students and collaborators, he demonstrated the first carbon nanotube computer. They also demonstrated the first 3D NanoSystem with computation immersed in data storage. These received wide recognition: cover of NATURE, Research Highlight to the US Congress by the NSF, and highlight as "important scientific breakthrough" by global news organizations.

Prof. Mitra's honors include the Newton Technical Impact Award in EDA (test-of-time honor by ACM SIGDA and IEEE CEDA), the University Researcher Award (by the Semiconductor Industry Association and Semiconductor Research Corporation to recognize lifetime research contributions), the Intel Achievement Award (Intel’s highest honor), and the US Presidential Early Career Award. He and his students have published over 10 award-winning papers across 5 topic areas (technology, circuits, EDA, test, verification) at major venues including the Design Automation Conference, International Solid-State Circuits Conference, International Test Conference, Symposium on VLSI Technology, and Formal Methods in Computer-Aided Design. Stanford undergraduates have honored him several times "for being important to them." He is an ACM Fellow and an IEEE Fellow.