Design of Clock Distribution in High Performance Processors

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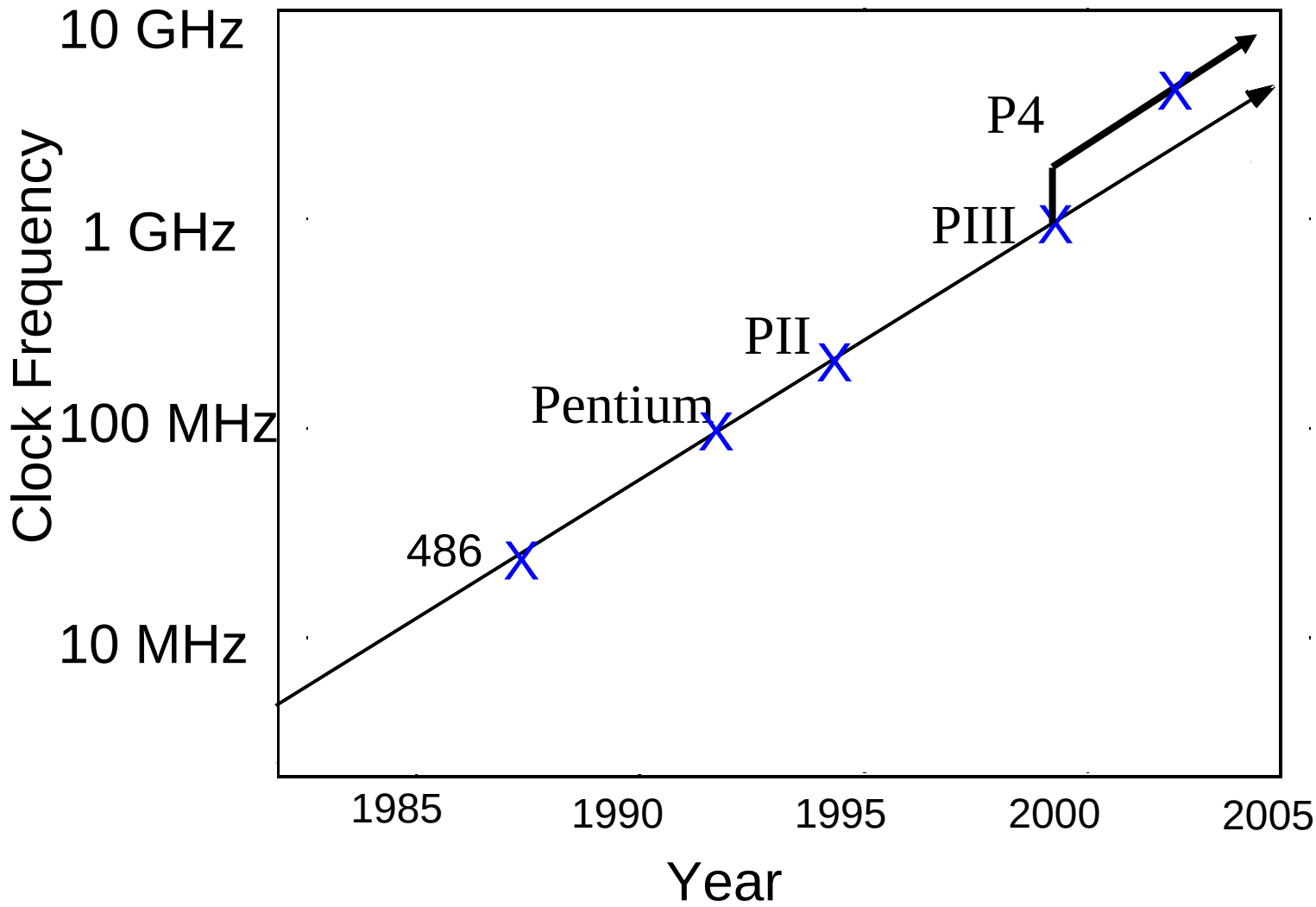
Desktop Clock Frequency Trend



Outline

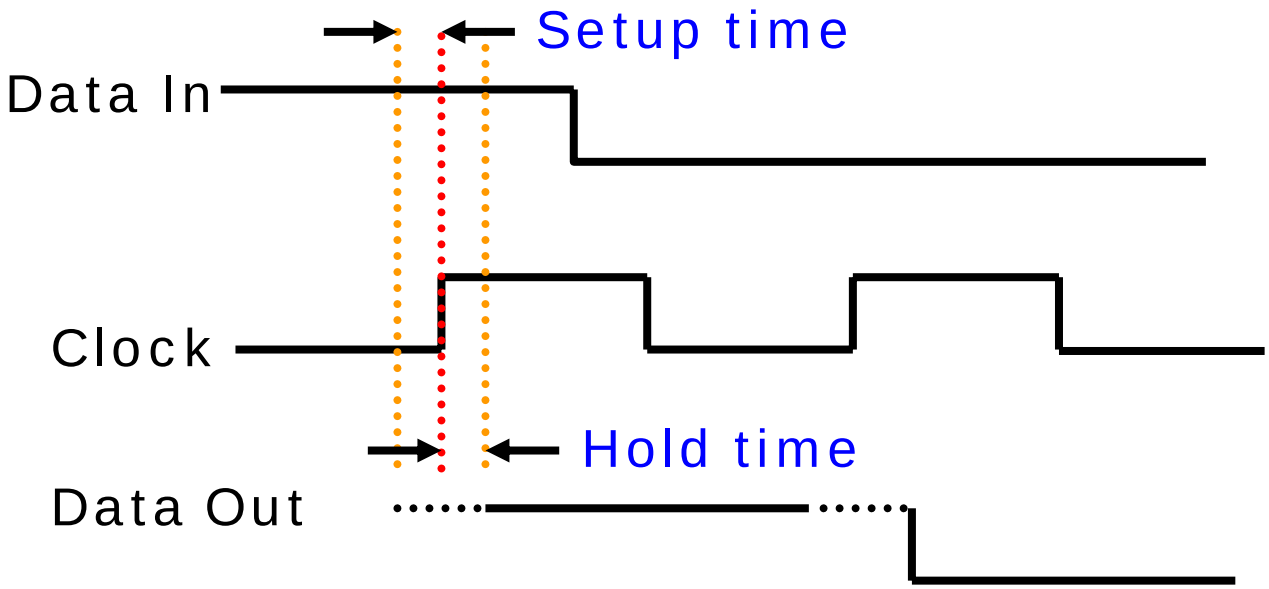
- Introduction to Synchronous Logic and clock distribution
- Manufacturing effects
- Early history of clocking: 80486, Pentium and Pentium II
- Itanium active deskewing clock distribution
- Pentium4 clock distribution
- Montecito (Itanium family next gen.) clock distribution
- Summary

Synchronous Logic

- Logic progresses at a rate controlled by the clock
  - Retiming removes the effects of different logic and wire delays
  - Slows down signals that arrive too fast
- Requires a state element
  - Latch stores Input when clock is low
  - Flip-Flop stores Input when clock rises
- Requires a precise clock
- Enables CPU pipelining and high through-put CPUs

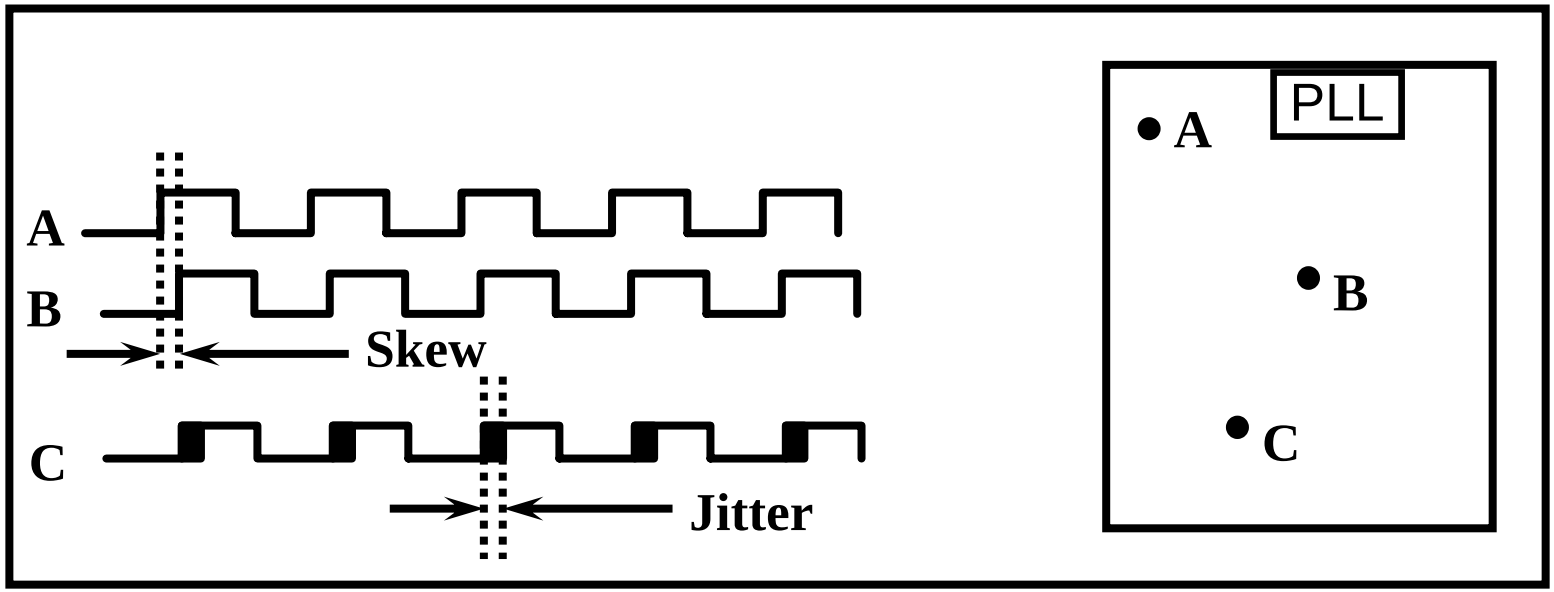
Flip-Flop: Set-up and Hold Times

- **Setup Time:**
  - time before the clock signal, that a data signal must be valid in order to be stored.
- **Hold Time:**
  - time after the clock signal, that a data signal must be valid in order to be stored.

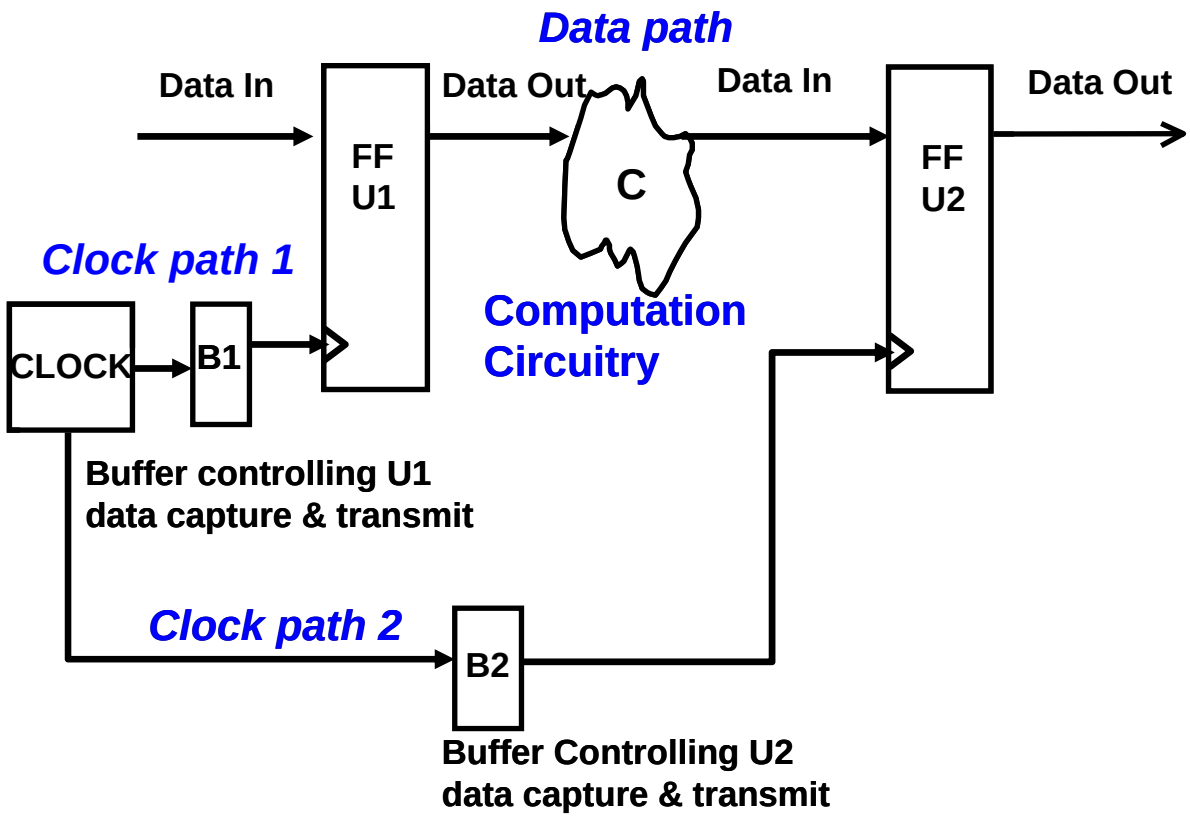


The Clock Distribution Problem

- Deliver the clock signal from the source (PLL) to all the receivers with the best timing precision.
- CLOCK SKEW is the inaccuracy of the same clock edge arriving at various locations in the chip (*spatial separation*)
- CLOCK JITTER is the inaccuracy of consecutive clock edges arriving at the same location (*temporal separation*)

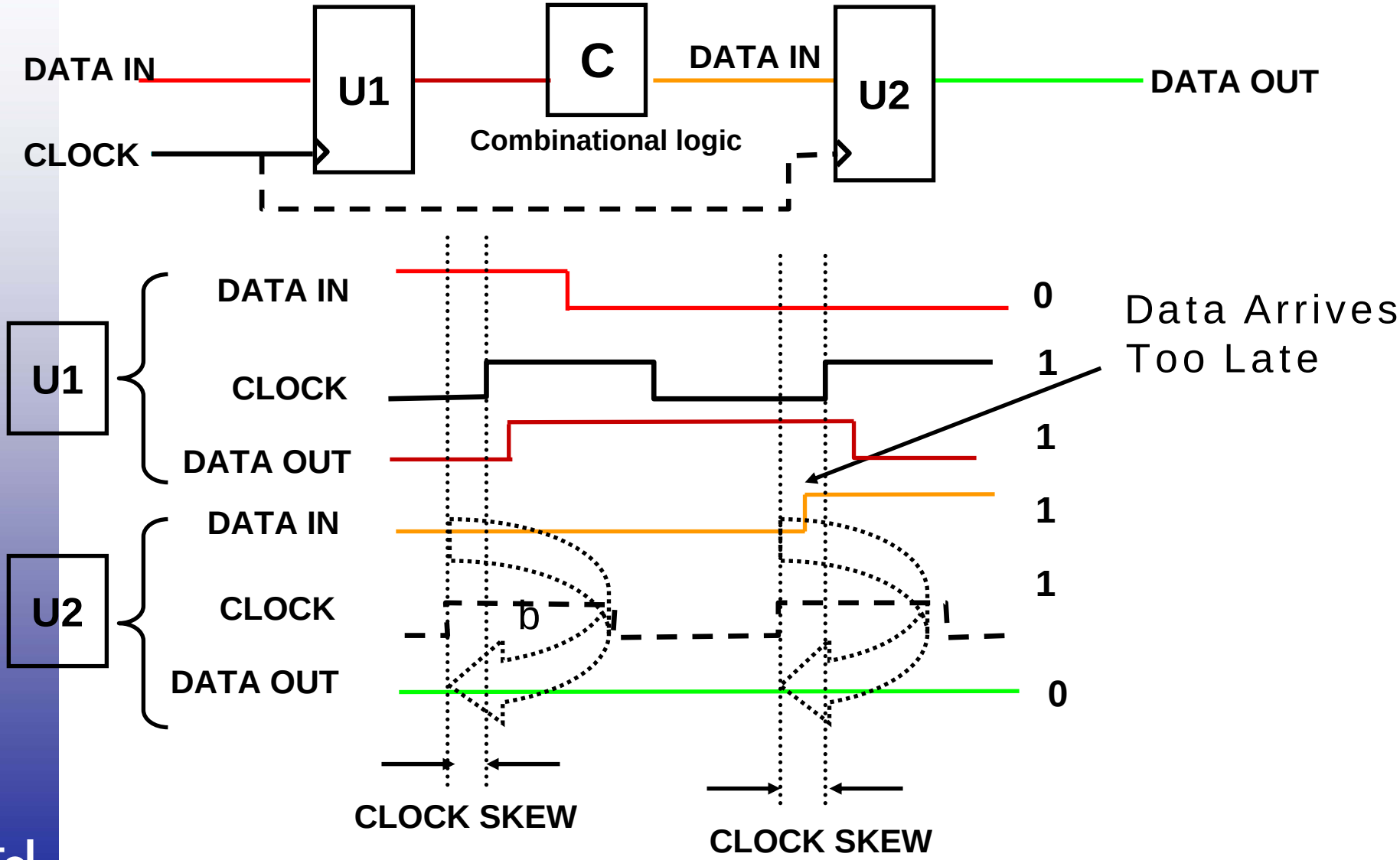


Clock and Logic Structure & Operation

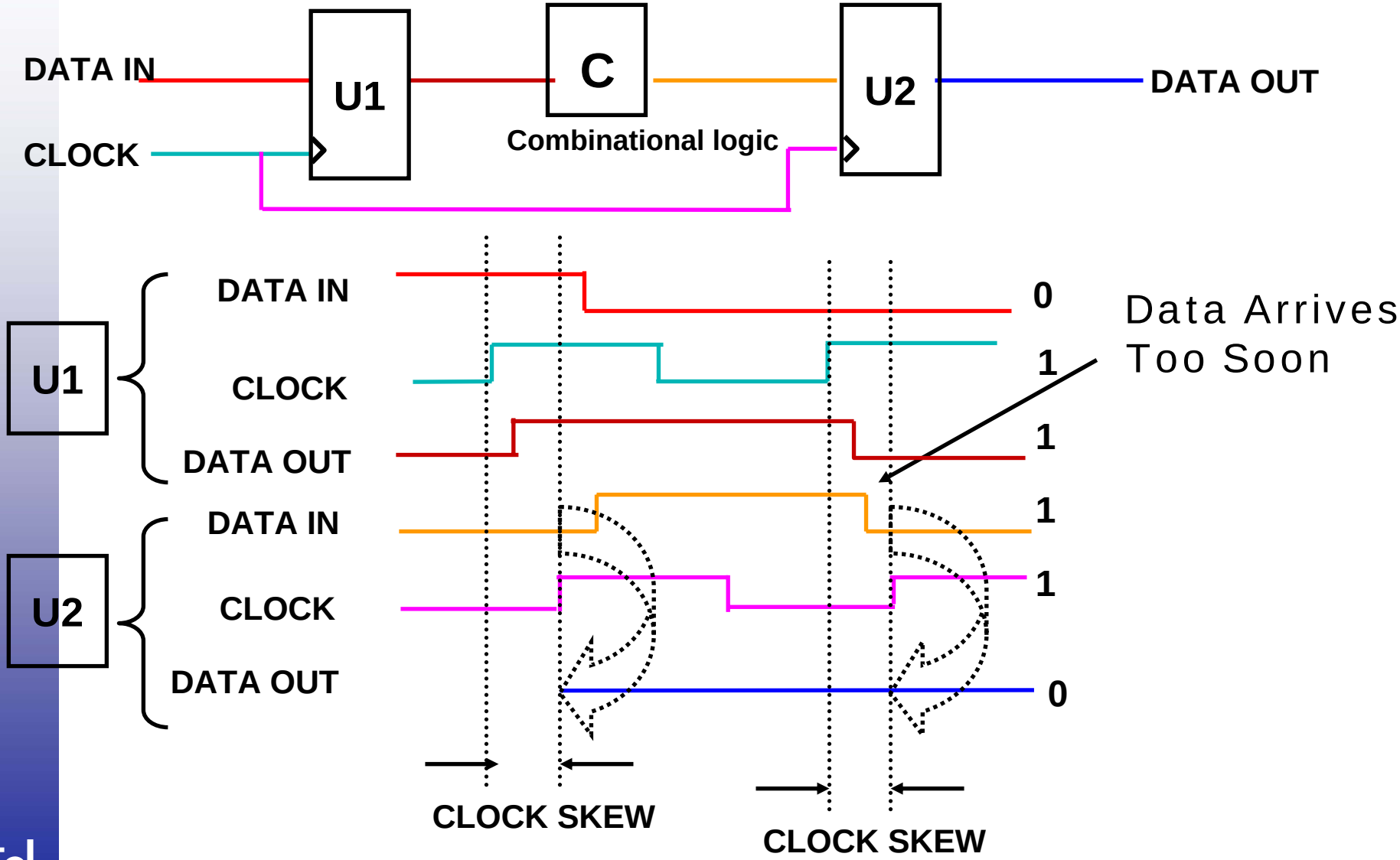


Clock Delay 1 = delay from Clock to the Clock input of U1.
Clock Delay 2 = delay from Clock to the Clock input of U2.
Clock Skew = Clock Delay 2 – Clock Delay 1 (should be zero).

SETUP violation: Data arrives at U2 too late, and doesn't get captured by U2 clock cycle.



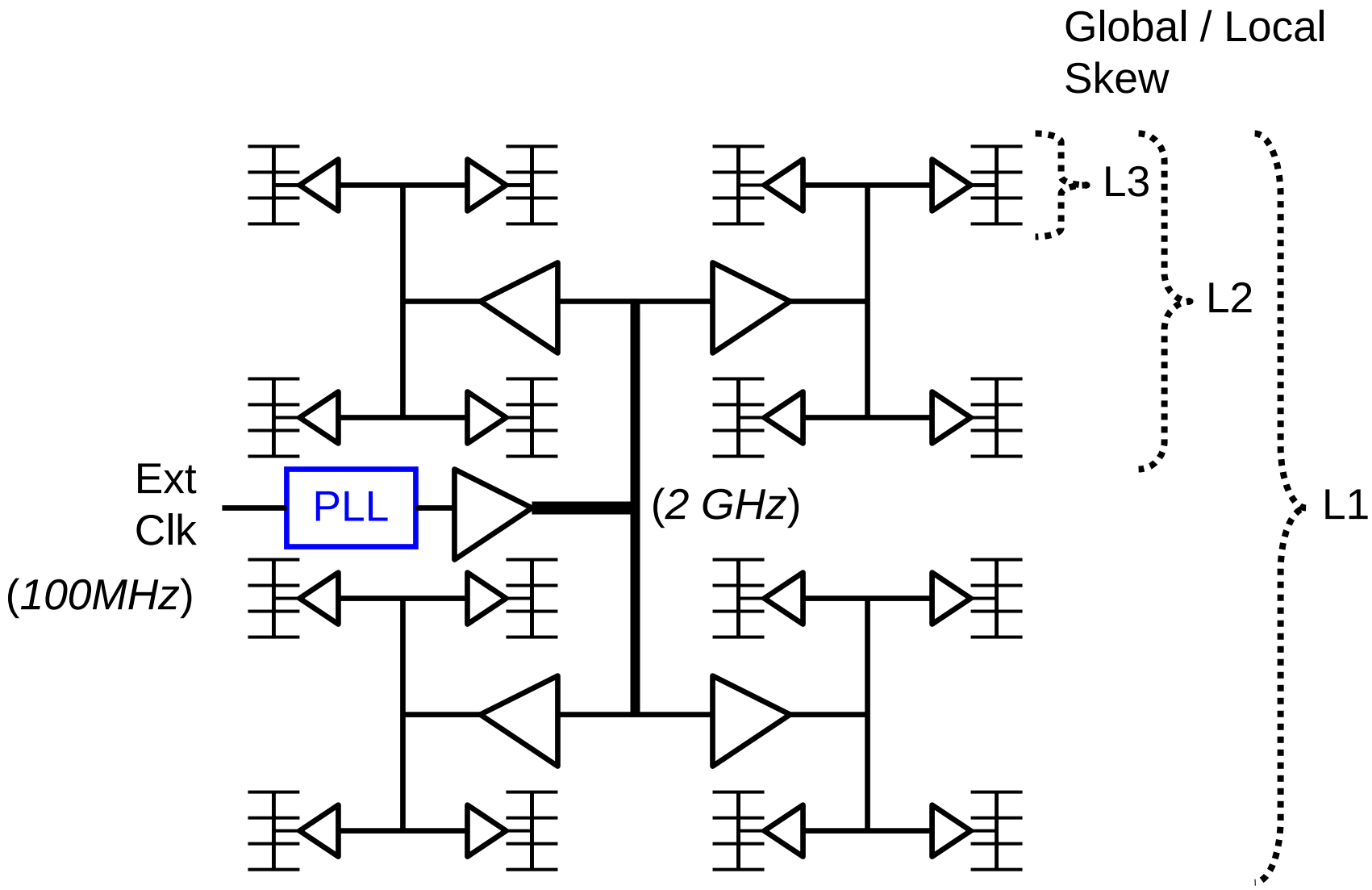
HOLD violation: Data arrives at U2 too soon, not held long enough to be captured by U2 clock cycle.



Challenges for Microprocessor Clock Design

- Rapid increases in Core Clock Frequencies
  - 1991: 100 MHz (0.8mm)
  - 1997: 400 MHz (0.35mm)
  - 2001: 2.0GHz (0.13mm)
  - 2005: 3.8GHz (90nm)
- Increasing Clock Load
  - as indicated by total transistors/die
  - 1991: 1.2 million transistors (0.8mm)
  - 1997: 7.5 million transistors (0.35mm)
  - 2001: 42 million transistors (0.13mm)
  - 2005: 1.7 billion transistor (90nm)
- Worsening within-die process variations
  - Lithography and Etch
  - Supply Noise
  - Hot Spots

Clock Distribution H-Tree (2 level)



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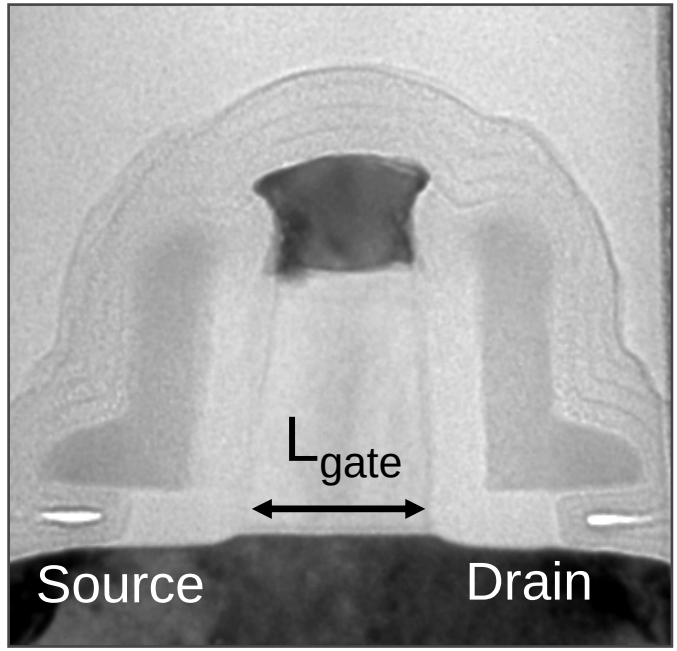
Poly Gate Transistor Length Variation Sources

- Long-range Within-die
  - Stepper lens aberrations
- Proximity effects (systematic)
  - Nest or isolated
- Random component
  - Stepper lens
  - Poly gate line edge roughness
  - Threshold voltage



Transistor V_{th} Variation Sources

- Die-to-die
- Random component
  - From Random Dopant Fluctuations f (W, L)
- Short channel component.
- Well and Halo doping

Vth Variation Model

- Model relates variability to device size:

$$\sigma(\Delta Vt) = C_1 + \frac{C_2}{\sqrt{WeZe}}$$

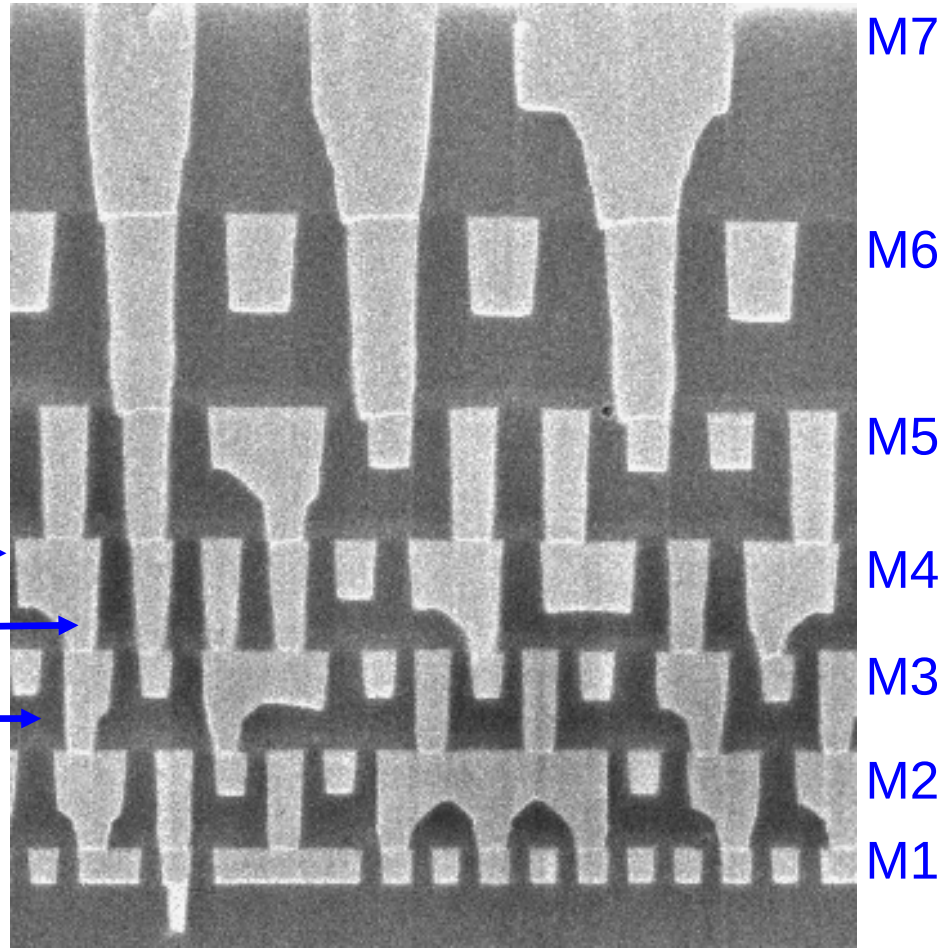
- Where W_e and L_e are the effective device width and length. C_1 and C_2 relate to some physical device parameters such as T_{ox}, junction depth, etc.

Interconnect Variability

- Conductor width and space
- Conductor Thickness
- Dielectric Thickness
- Inductance
  - needs to be analyzed and modeled for busses

Interconnect Variability

- Conductor Thickness
- Dielectric Thickness
- Power and Global Signal Inductance (needs to be analyzed and modeled)



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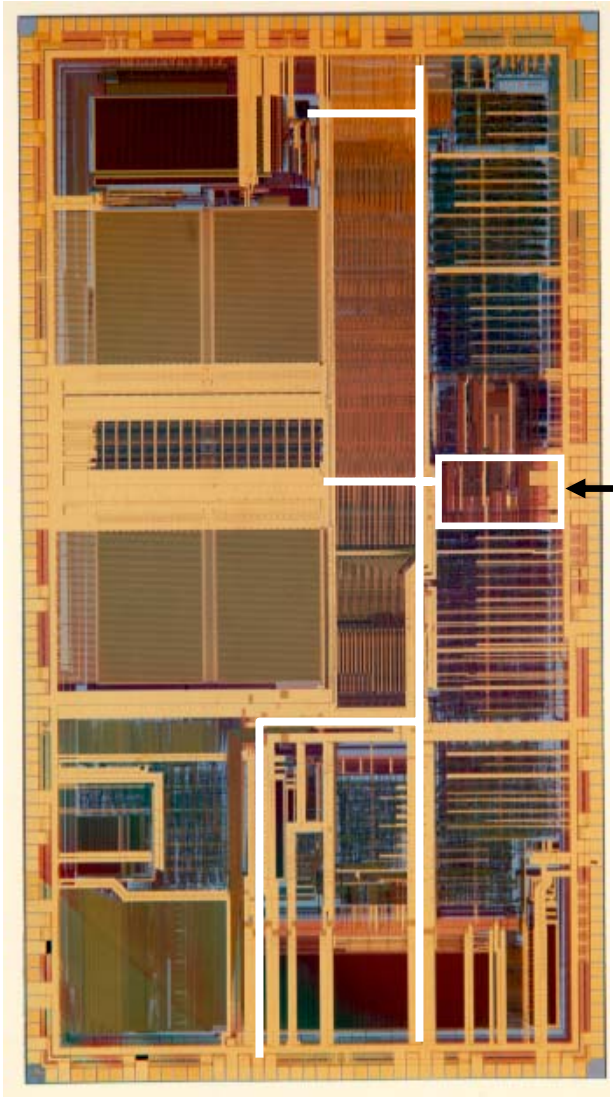
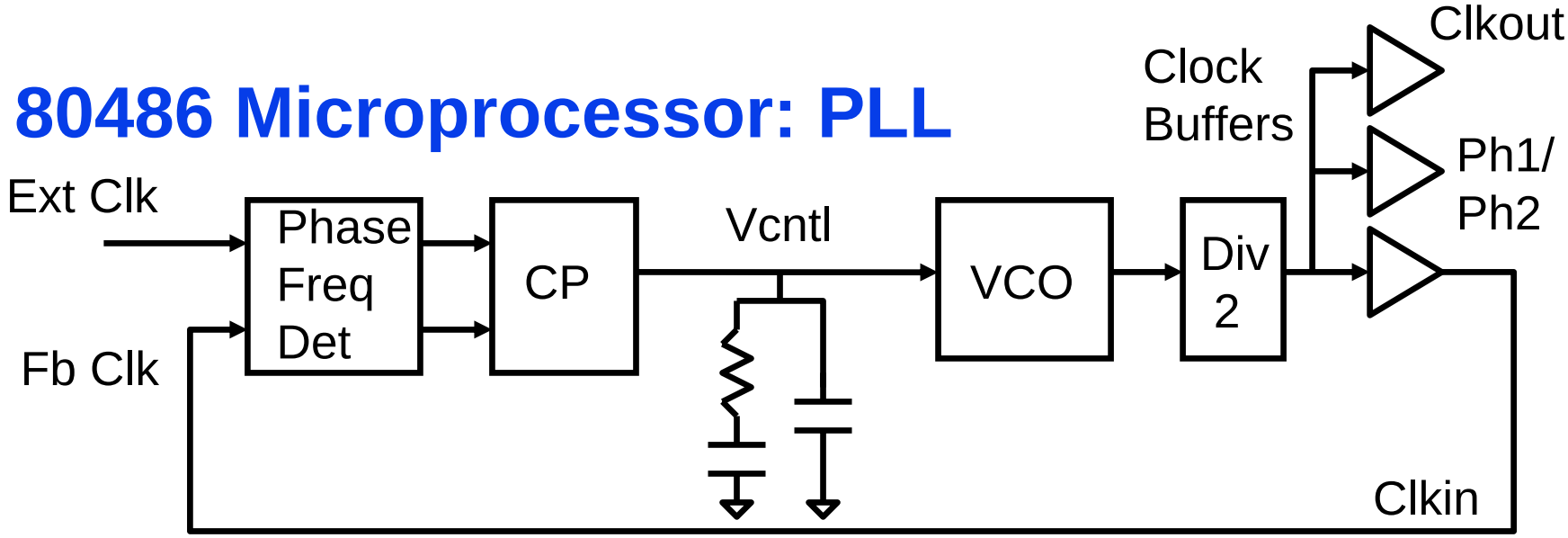
The 50MHz 80486 Microprocessor (1991)



- 3 Layer Metal
- 2 Phase Clocking
- RC clock skew
- On-chip PLL

80486 Microprocessor: PLL

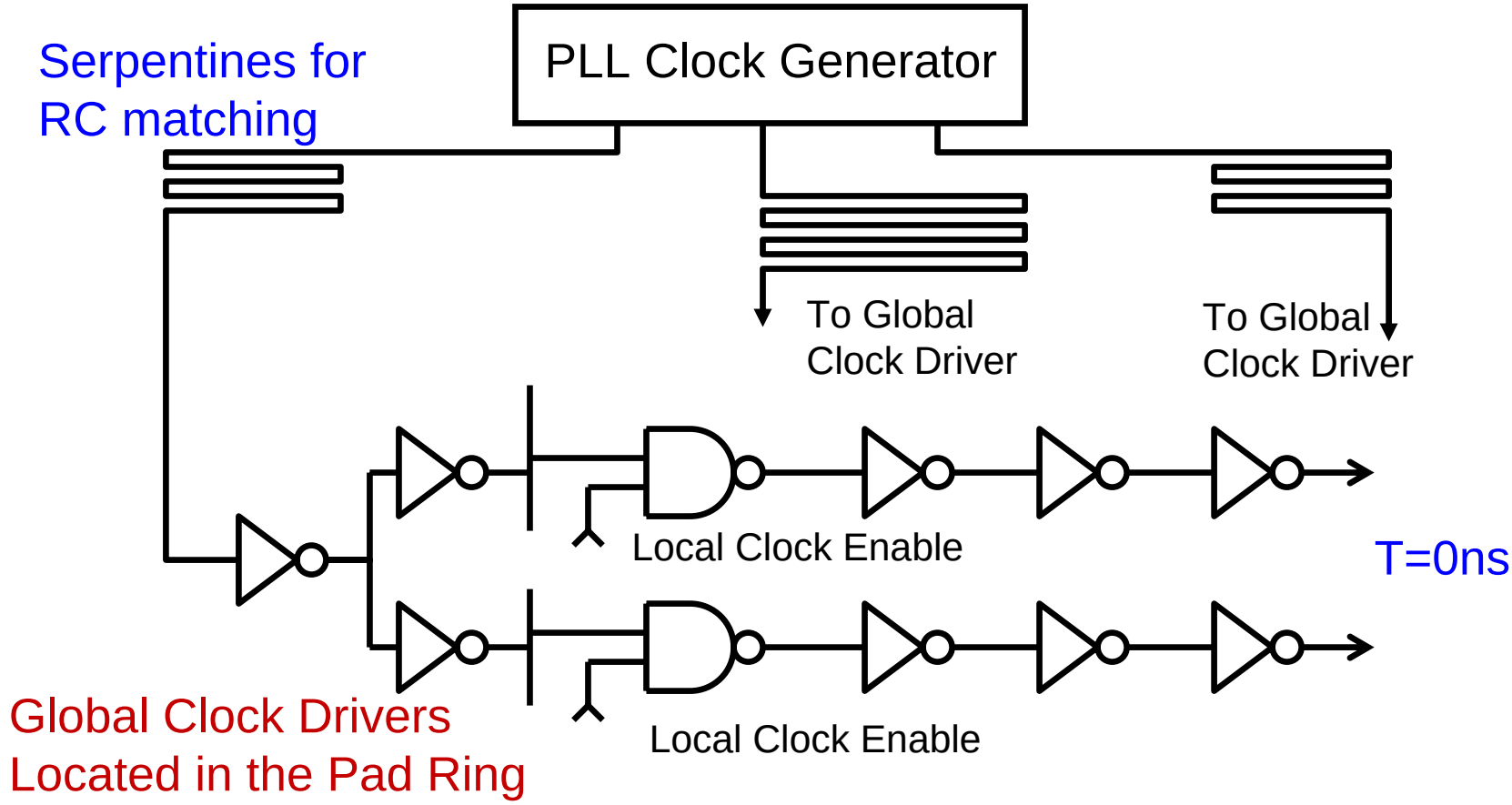


- 50% duty-cycle 2ϕ clocks, Clkin, Clkout compatible with prior gen.
- Internal Clock Skews Between Chips Reduced by ~2ns
- Enables 0-1ns Hold Time for frequency Scalability
- VCO Designed with: Wide Frequency Range (5-130MHz)
  Supply Voltage Noise Rejection

	Conventional	With PLL
Setup	3ns	1.5ns
Hold	2.5ns	1.0ns
Output Valid	9.0ns	7.5ns

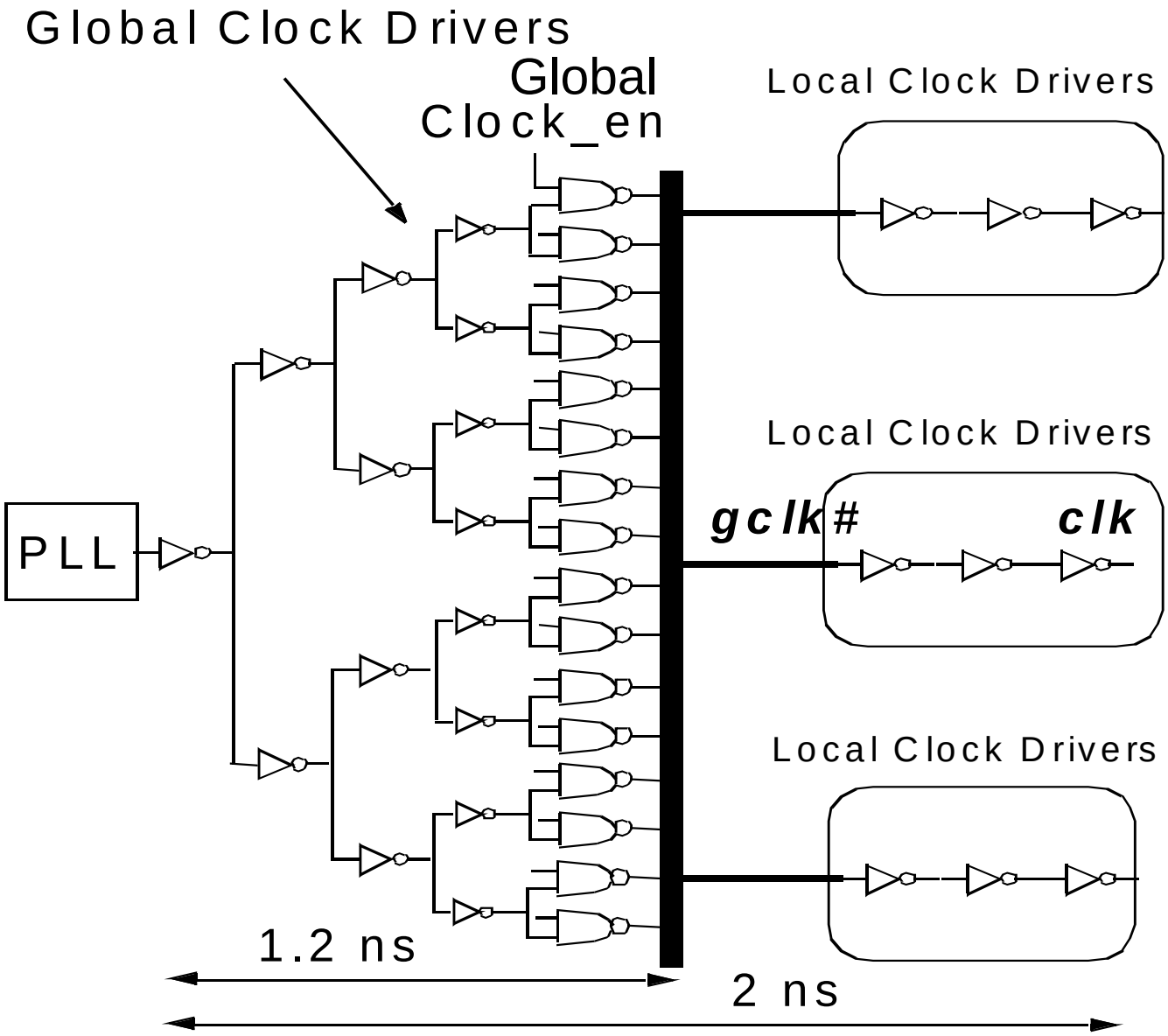
Pentium Microprocessor Clock Distribution

- Single 50% Duty-cycle Clock
- 66-133MHz Internal Frequency
- Internal clock freq. vs. External bus freq. Ratios of 2:1, 3:2, 1:1



Pentium II (P6) Microprocessor Clock Distribution

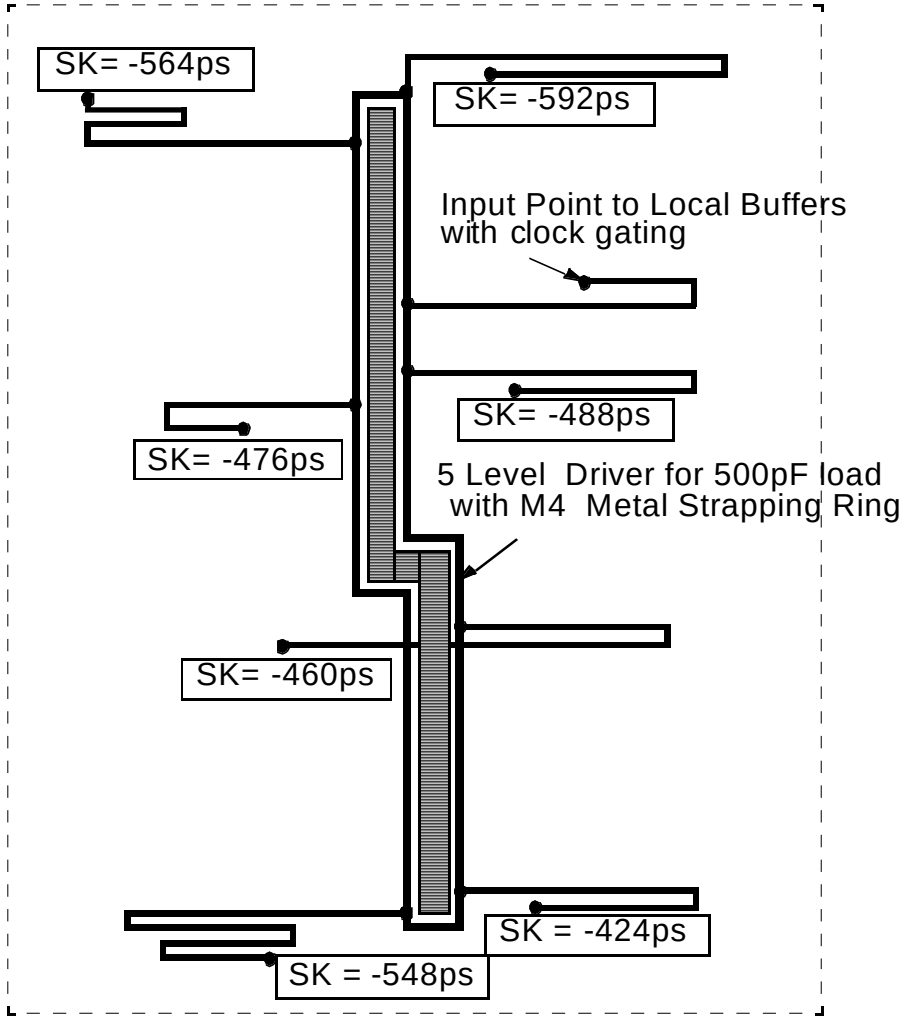
- Buffer Network designed for > 300 MHz
- Minimized the Propagation Delay
- Minimized Global Clock Skew
- Global Clock Power Down
- Supply di/dt noise reduction
  - Vdd / Vss decoupling capacitance
  - Minimize Vdd / Vss DC Resistance (IR drop)
  - Minimize Vdd / Vss AC Resistance and Inductance



Clock Distribution Network

Pentium II Global Clock Skew measured test chip results

- Floor Plan of measured skew
- SK = Skew relative to feedback point from local buffer
- Skew across M4 Global Distribution = 140ps



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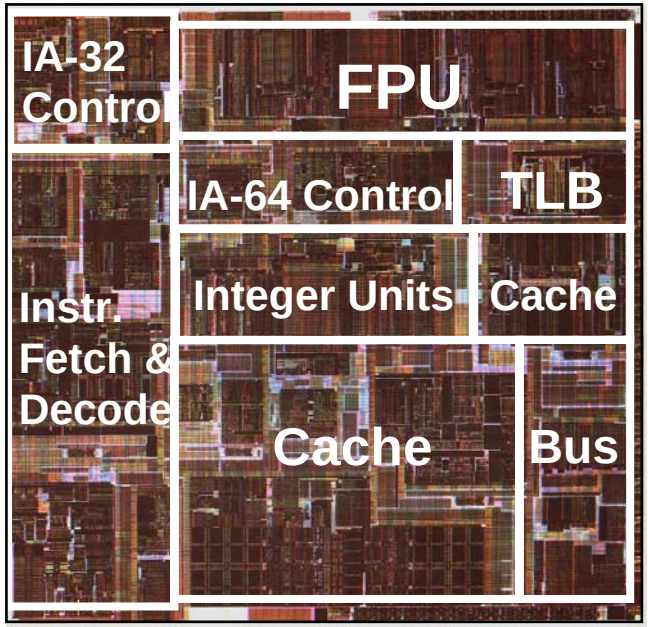
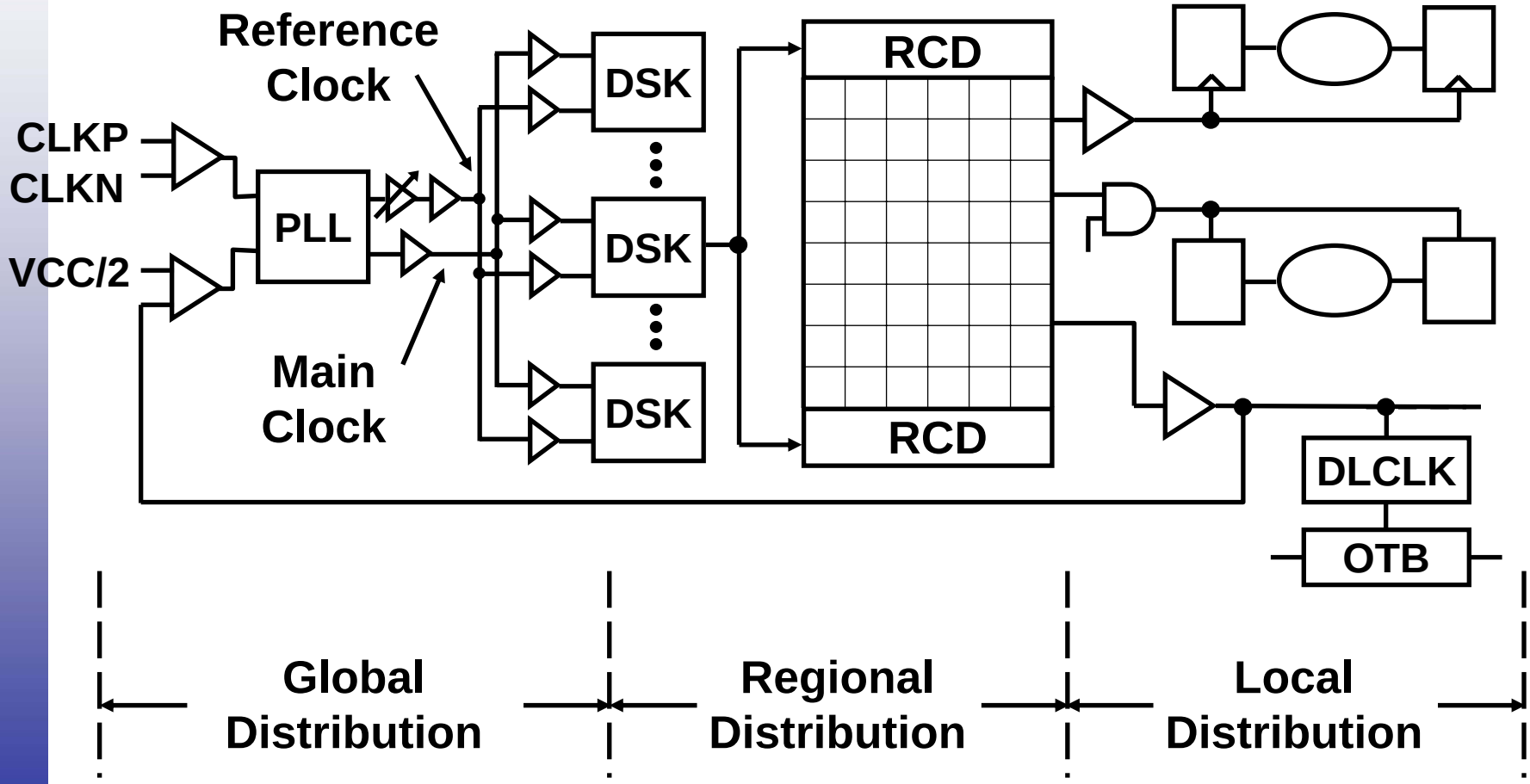
Itanium Processor Clocking



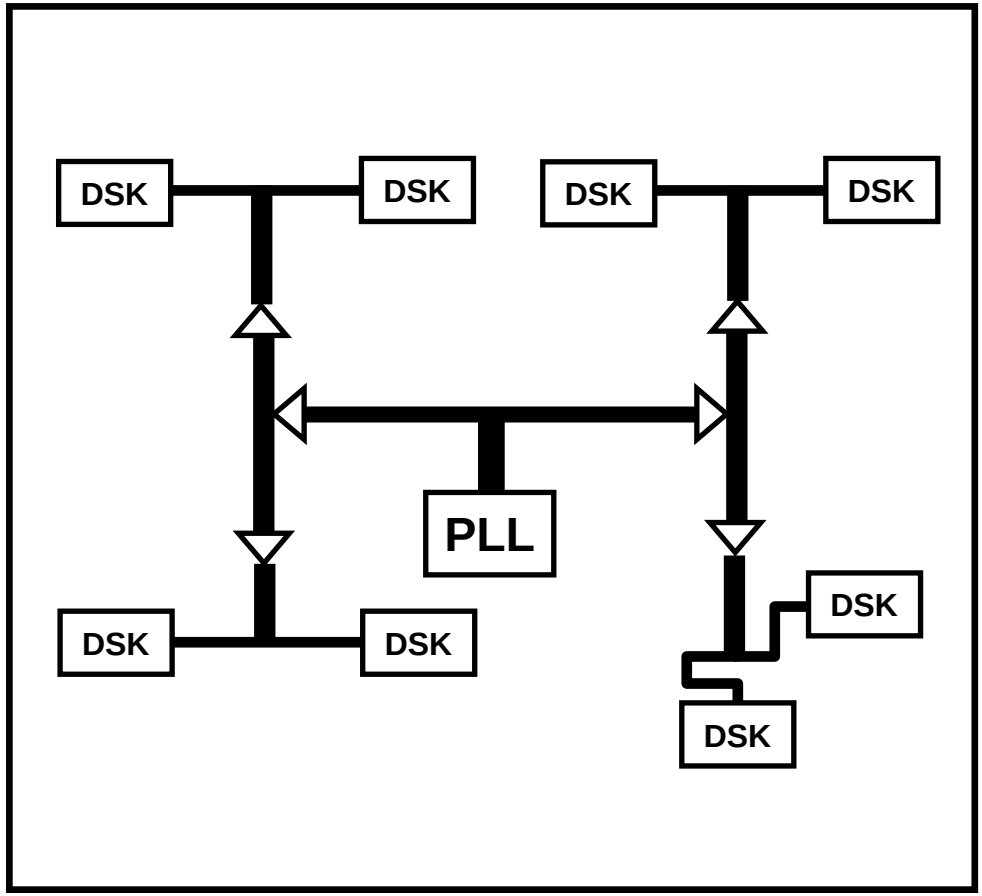
- IA-64 architecture
- 0.18µm CMOS
- 6 metal layers
- 25.4M transistors
- 800MHz frequency

Ref: S. Tam, S. Rusu, U. Desai, R. Kim, J. Zhang, I. Young JSSC Nov 2000

Clock Distribution Hierarchy

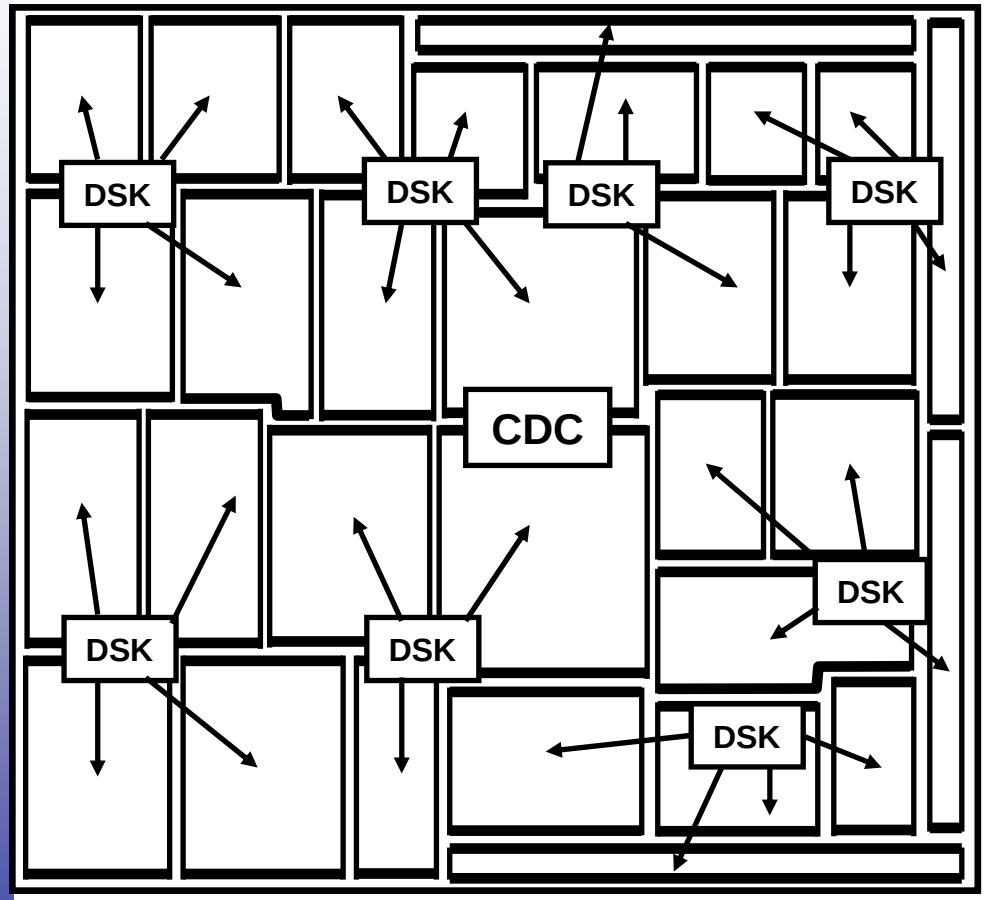


Itanium Global Clock Distribution



- Balanced H-tree routed in M5 and M6
- Lateral shielding
- Distributes both main and reference clock
- Optimized to account for inductive effects

Itanium Regional Clock Distribution

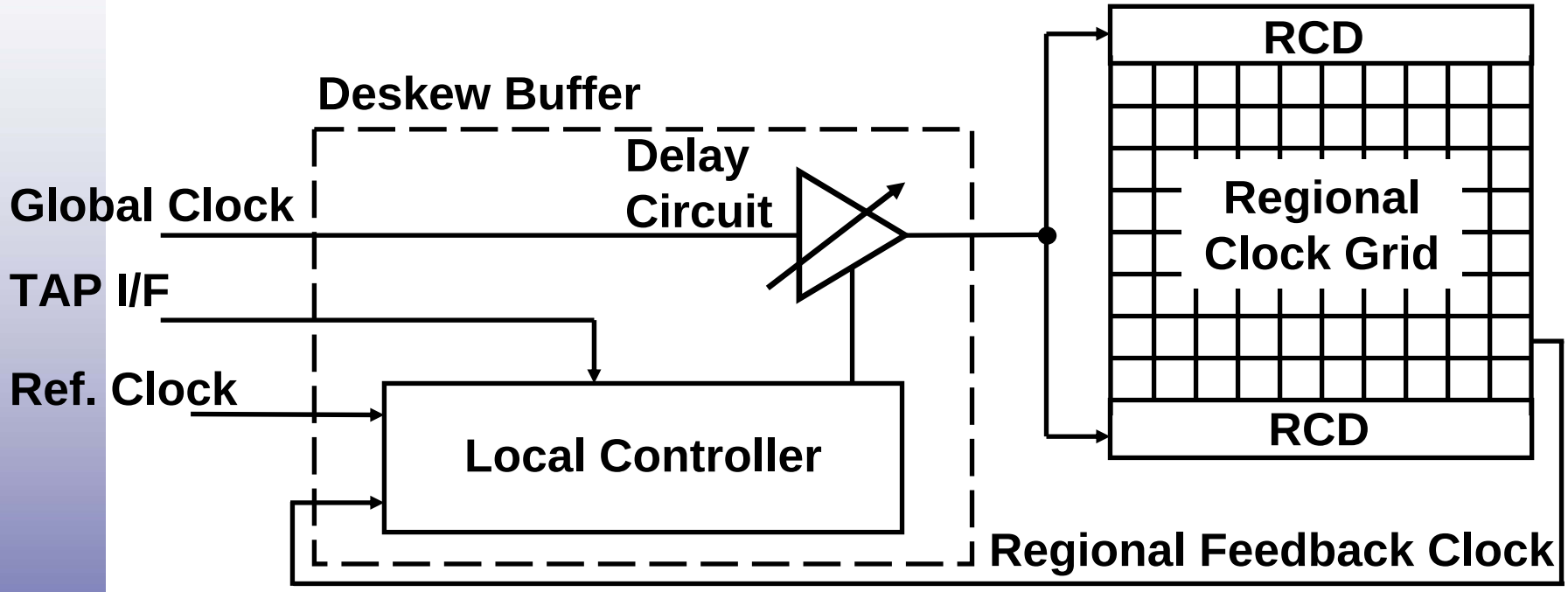


DSK = Cluster of 4 deskew buffers

CDC = Central Deskew Controller

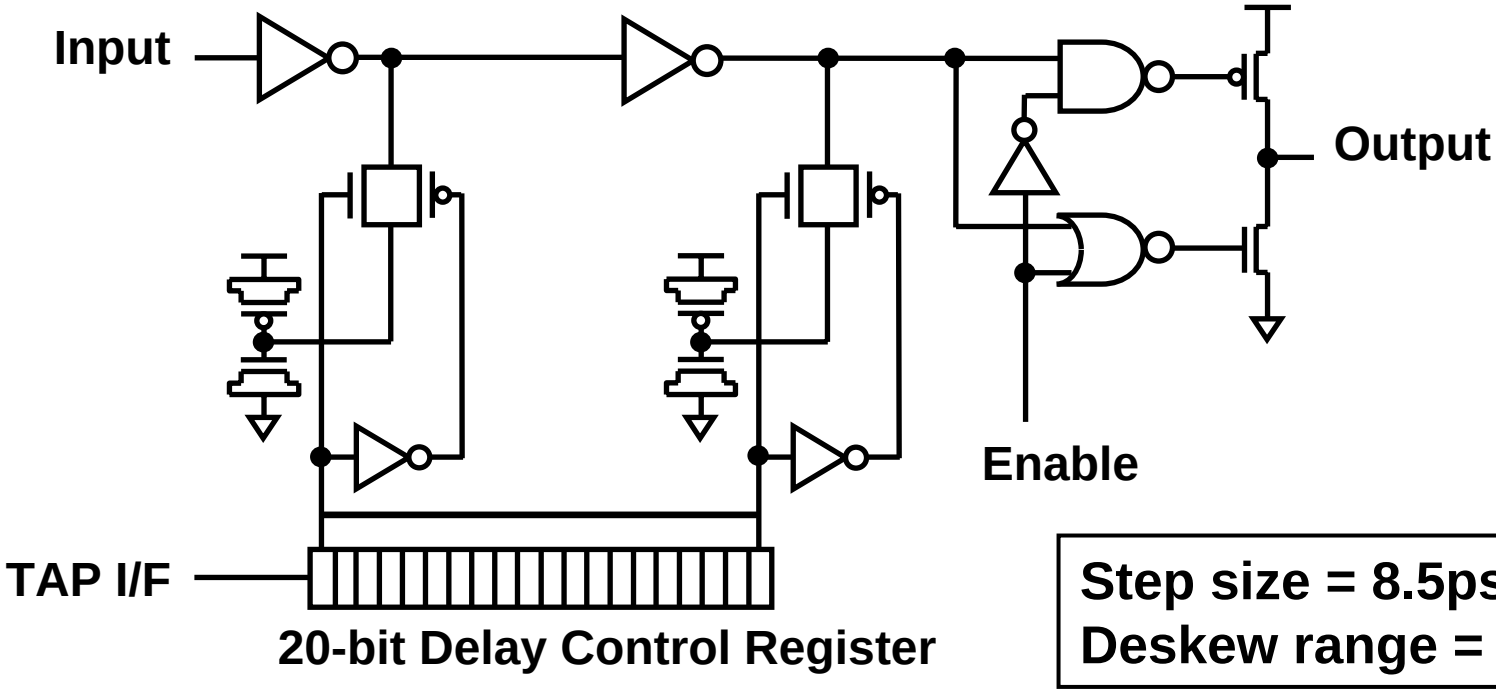
- **Distributed array of deskew buffers to reduce process related skew**
  - 8 deskew clusters each holding up to 4 buffers
- **Regional clock grids driven by modular Regional Clock Drivers**
  - M4-M5 grid tailored for the clock load density of the underlying block
  - Full support for scan and clock gating

Deskew Buffer: Block Diagram



- Deskew covers the entire clock distribution up to the input of the local clock buffer

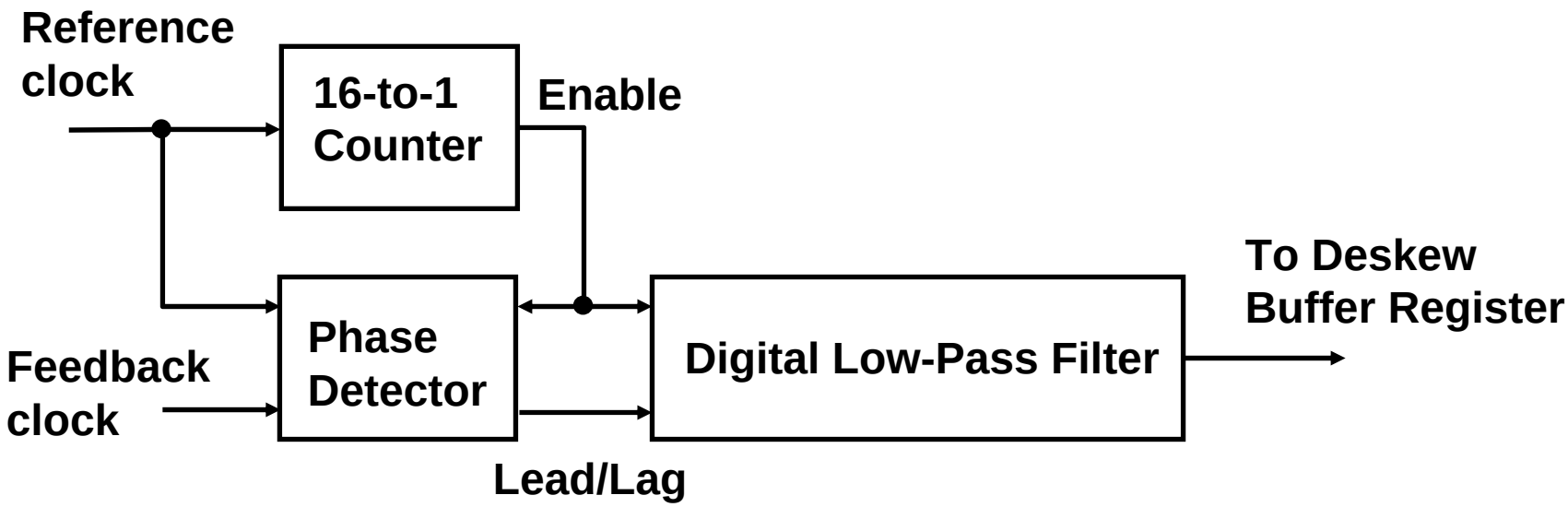
Deskew Buffer: Delay Circuit



Step size = 8.5ps
Deskew range = 170ps

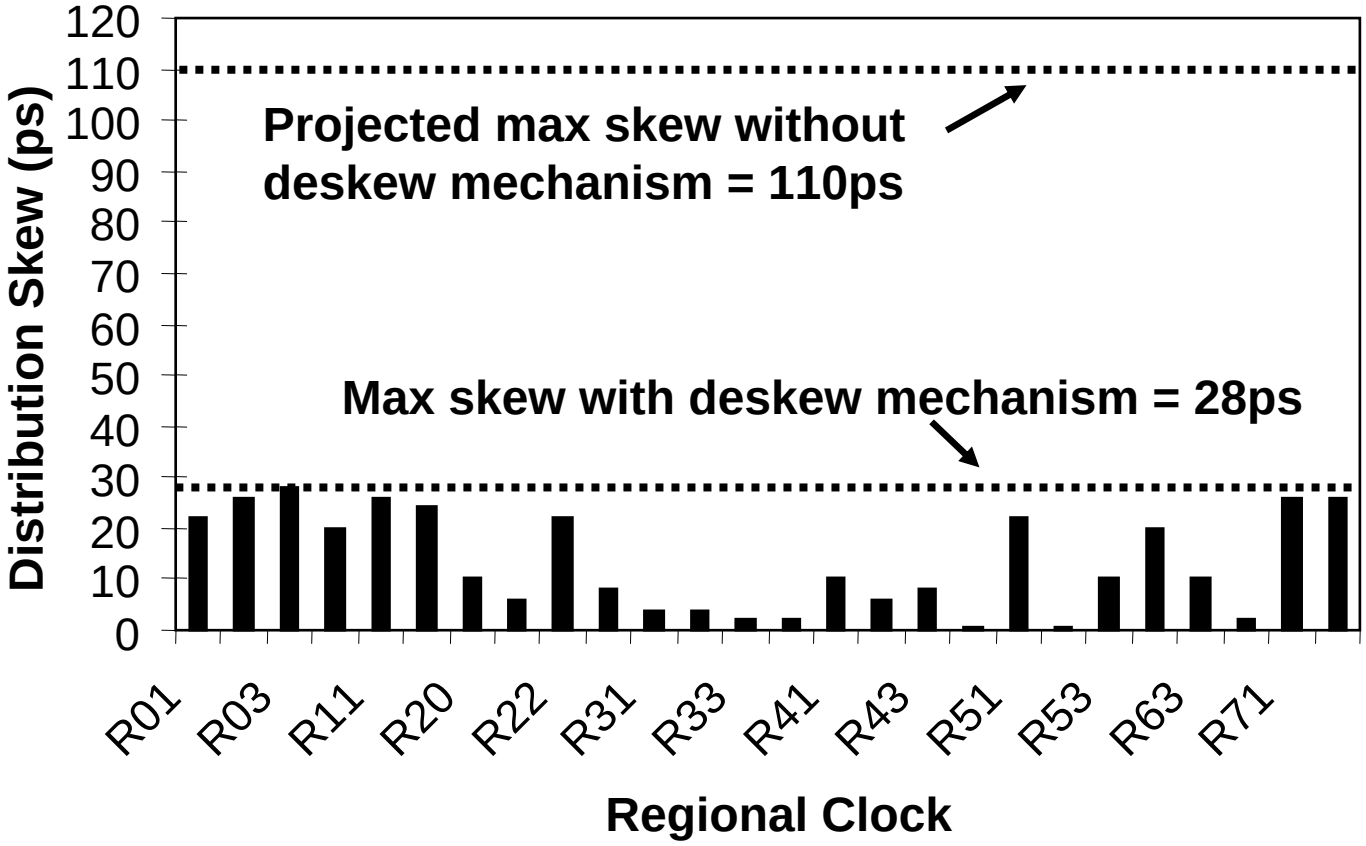
- **Small step size enables fine granularity skew control over a wide range**
- **TAP read/write access to Control Register enables faster timing debug and performance tuning**

Deskew Buffer: Local Controller

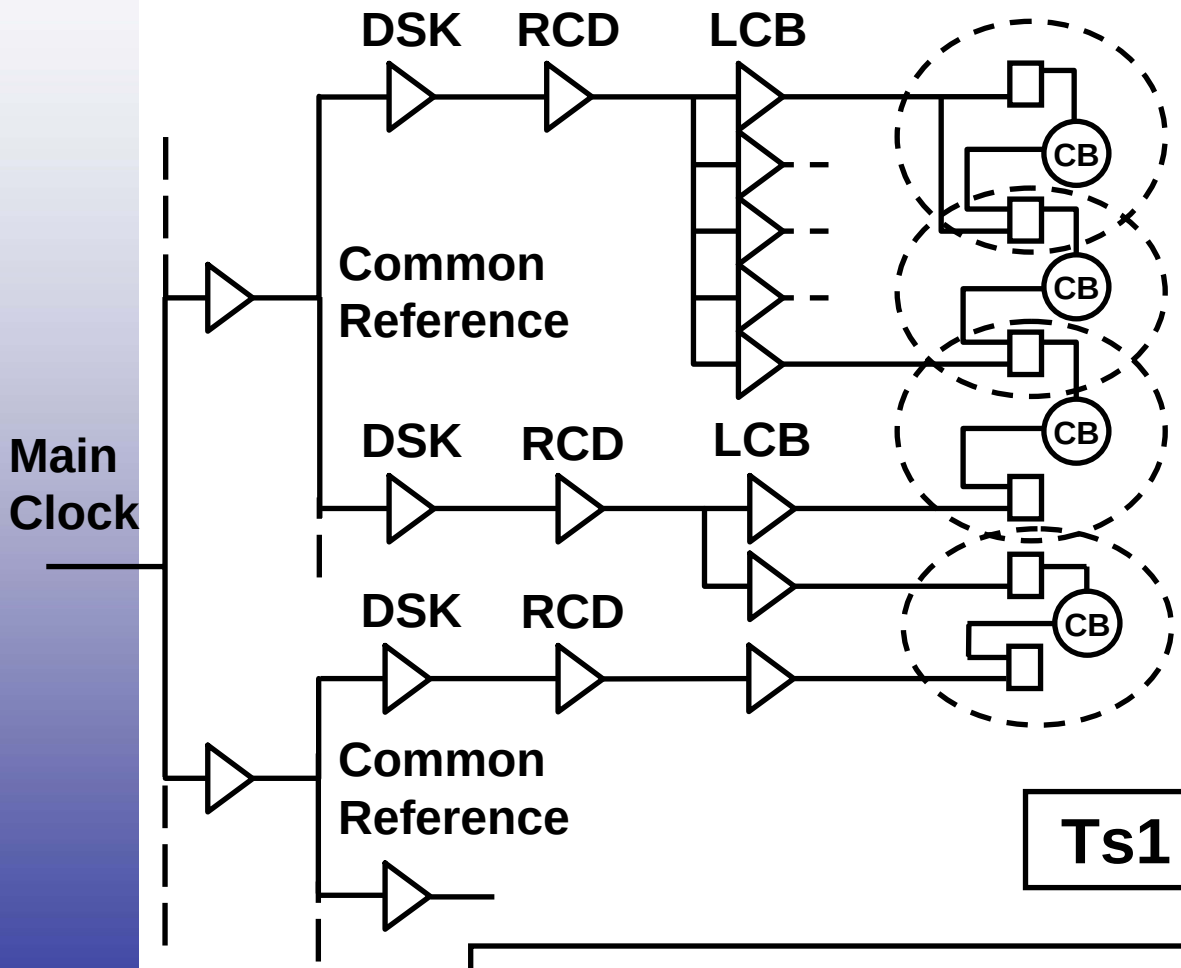


- Phase detector output sampled every 16 core cycles
- 6-tap digital low pass filter reduces comparison noise
- Local controller ensures stable deskew operation

Itanium Skew Measurements



Clock Skew Timing Budgets



Category	Skew Budget
Common LCB	Ts1
Common RCD	Ts2
Common Reference	Ts3
Common Main Clock	Ts4

Ts1 < Ts2 < Ts3 < Ts4

Multiple skew budgets minimize the skew penalty and enable timing optimization

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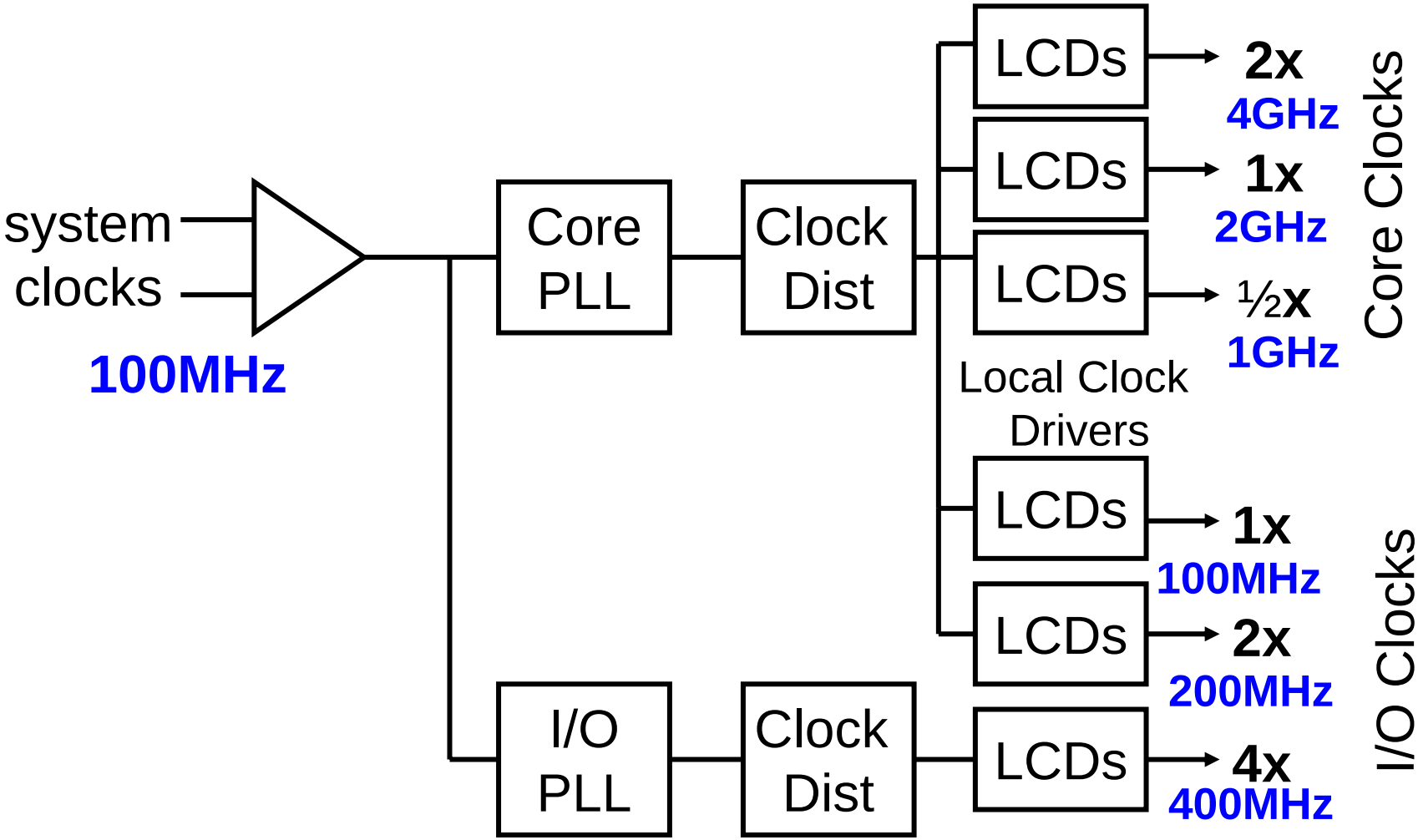
Pentium®4 Clock Challenges

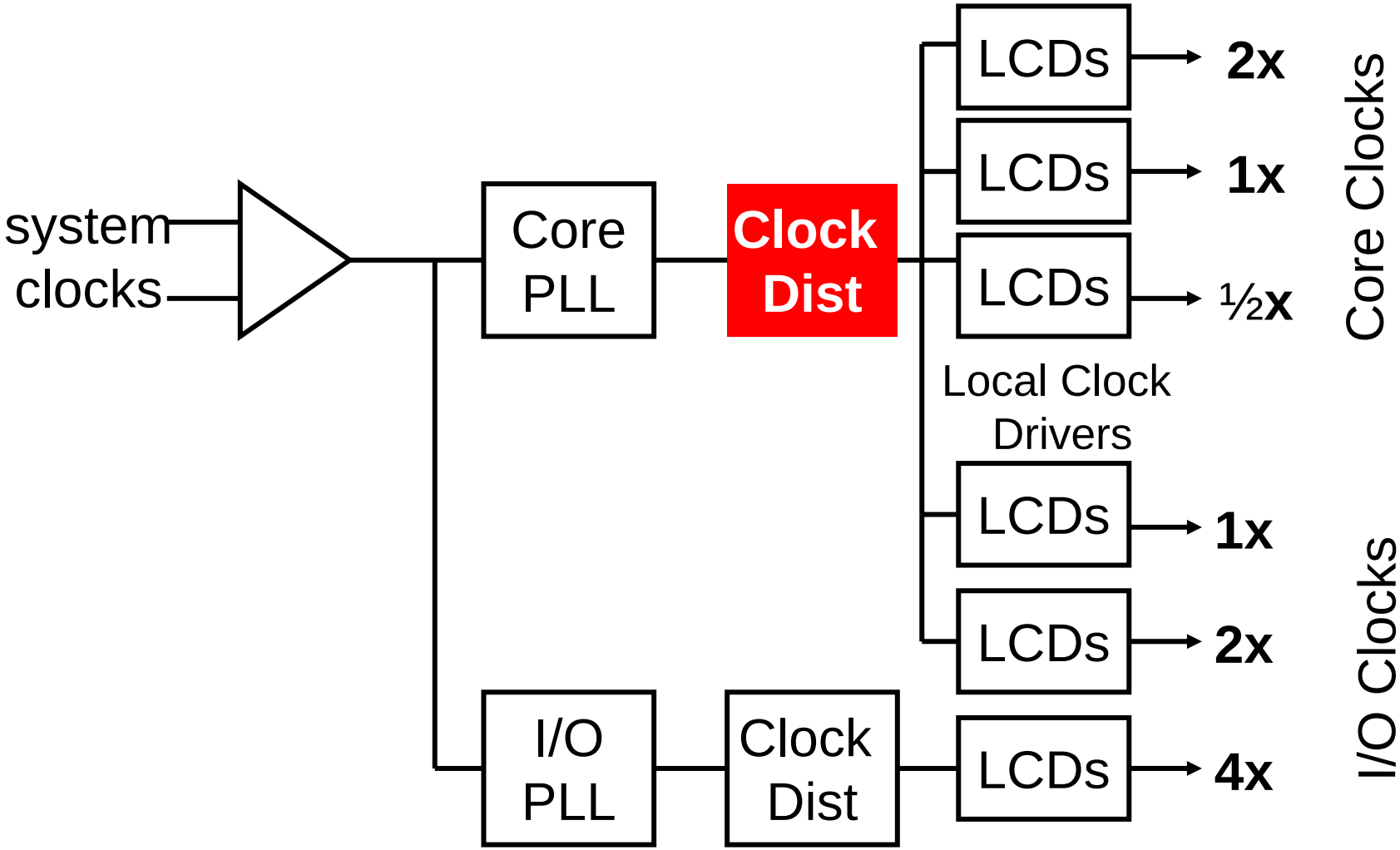
- Enable Netburst™ micro-architecture for 0.18um technology
  - ≥ 2GHz clock for Hyper Pipelined Technology core
  - ≥ 4GHz clock for Rapid Execution Engine
  - ≥ 400MHz I/O clock for fast data transfer
  - < 10% clock inaccuracy
- Enable clock gating for low power
- Clock observability and controllability for fast debug

Reference: Kurd, Barkatullah, Dizon, Fletcher, Madland JSSC Nov 2001

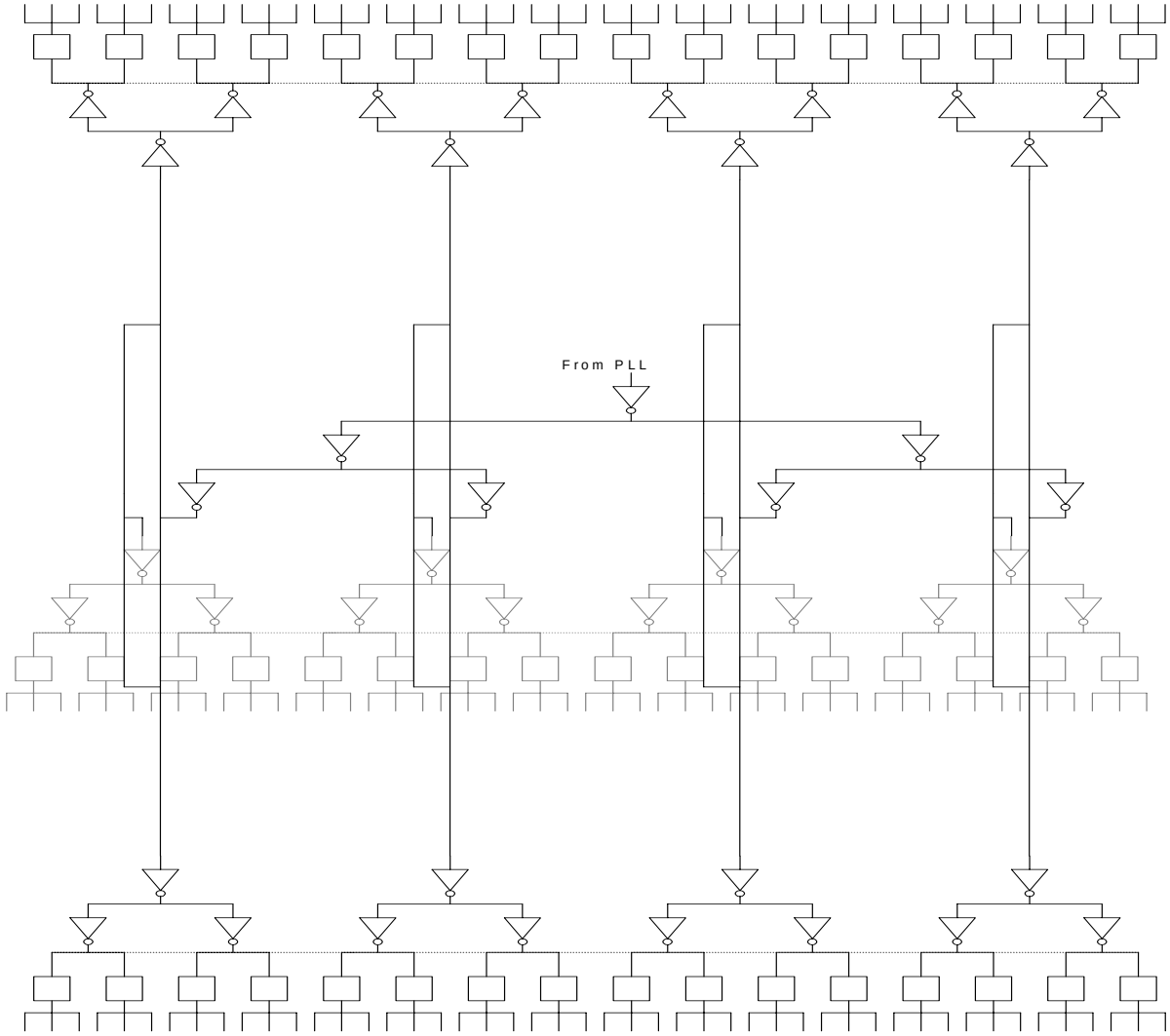
Clock Generation & Distribution



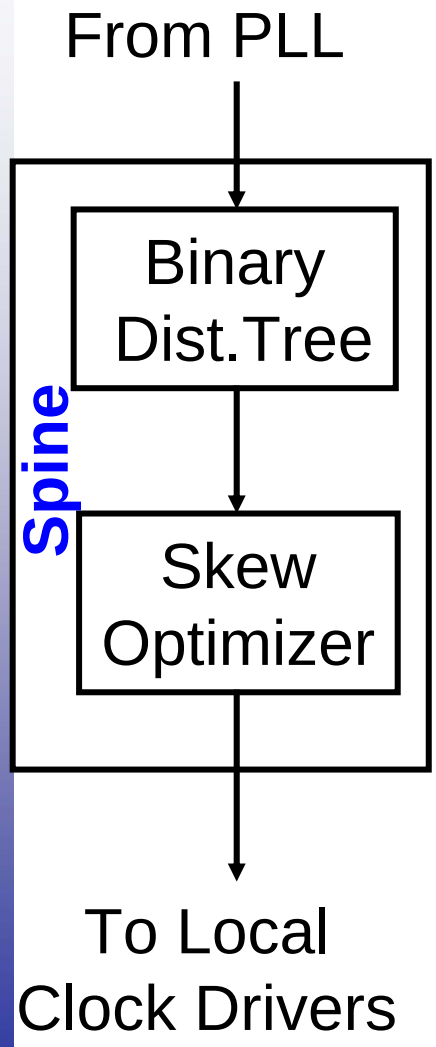
Clock Distribution

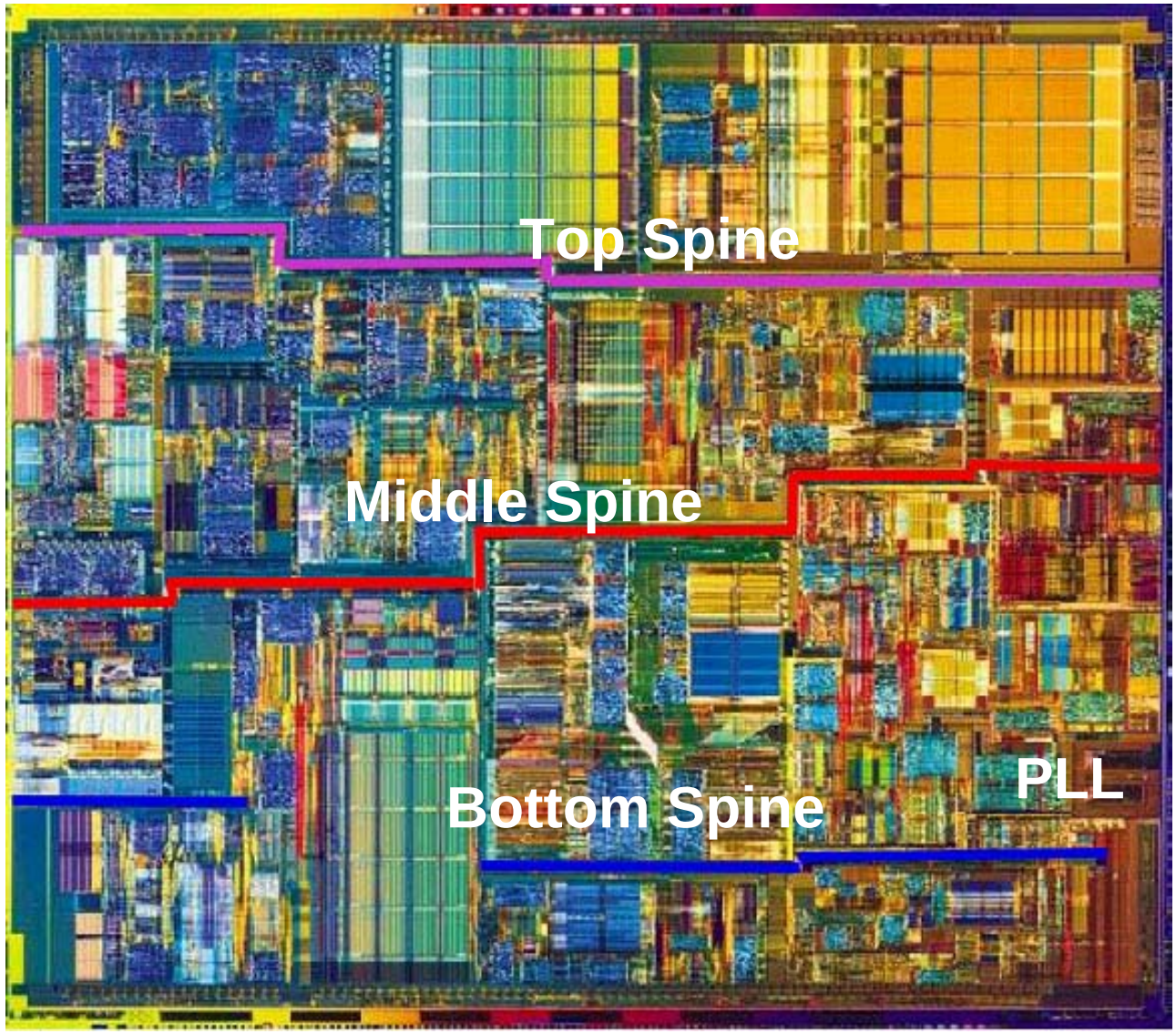


Binary distribution tree in three spines

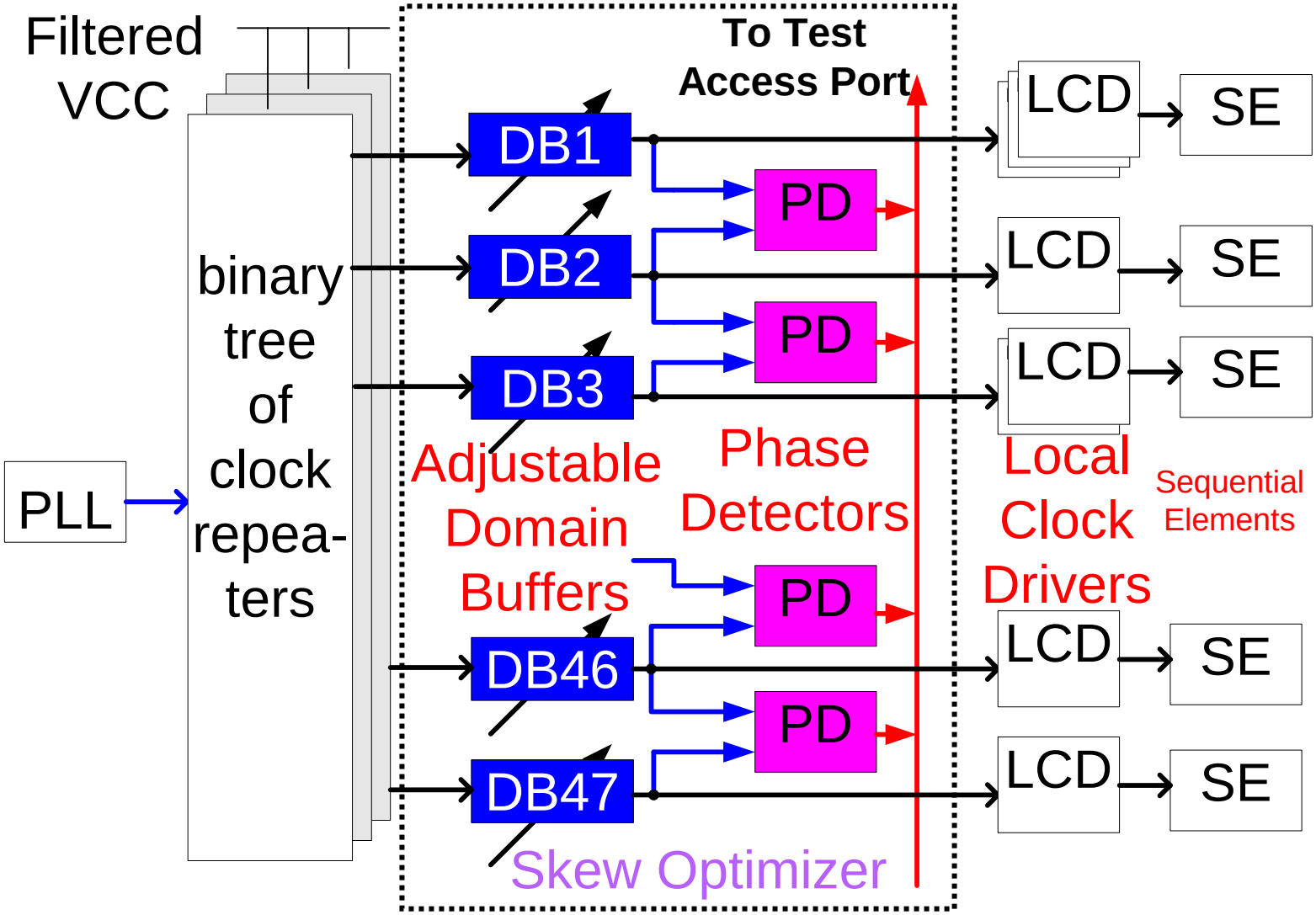


Triple Clock Spines

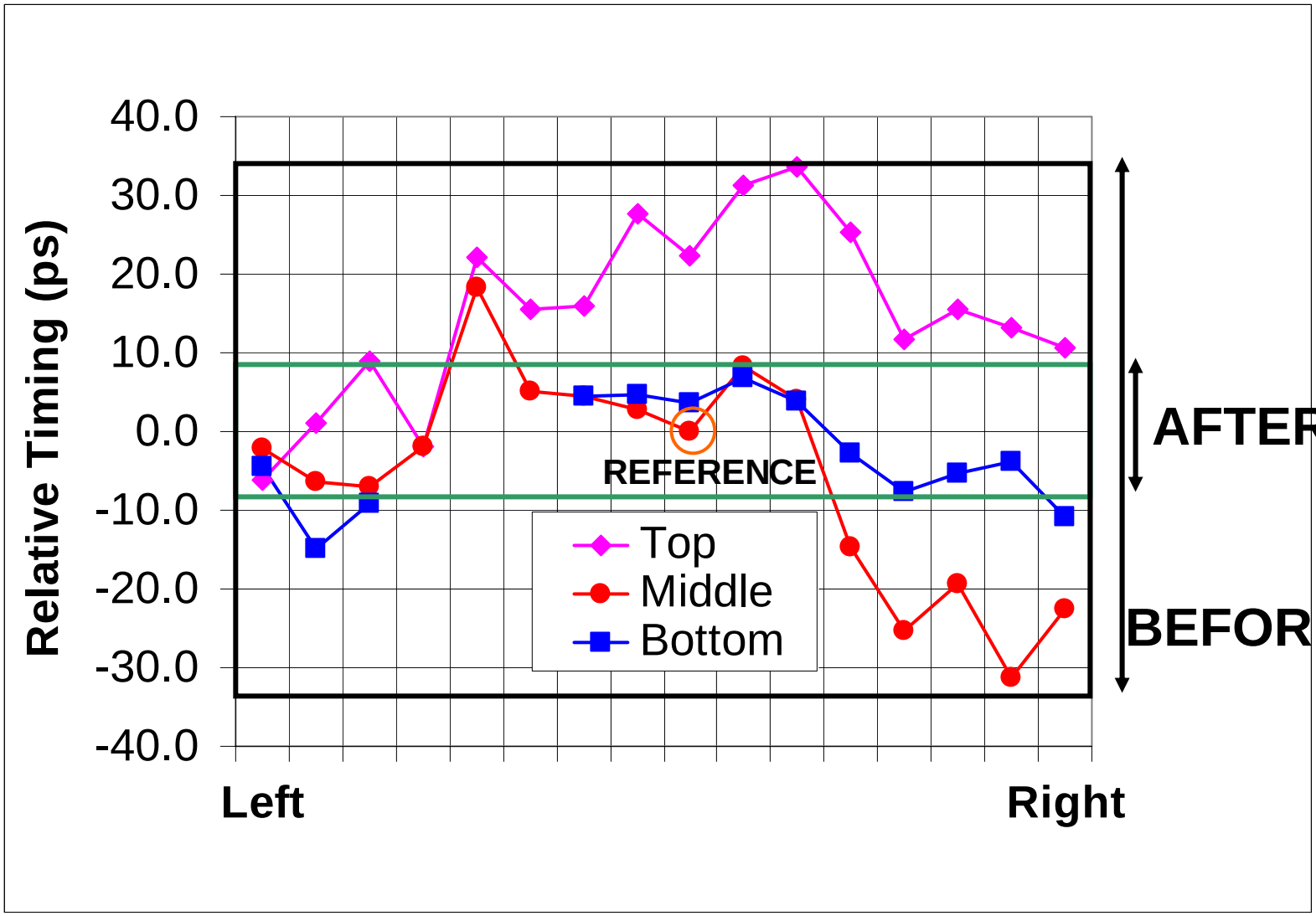




Skew Optimization Scheme



Skew Profile Graph



Skew Control Scheme

- For the particular die example shown
  - Pre-compensation max skew ~ ±32ps
  - Post-compensation max skew ±8ps

- Side benefits
  - Provides a within-die skew profile
  - Deliberately skew clocks for performance
    - 200MHz frequency increase obtained

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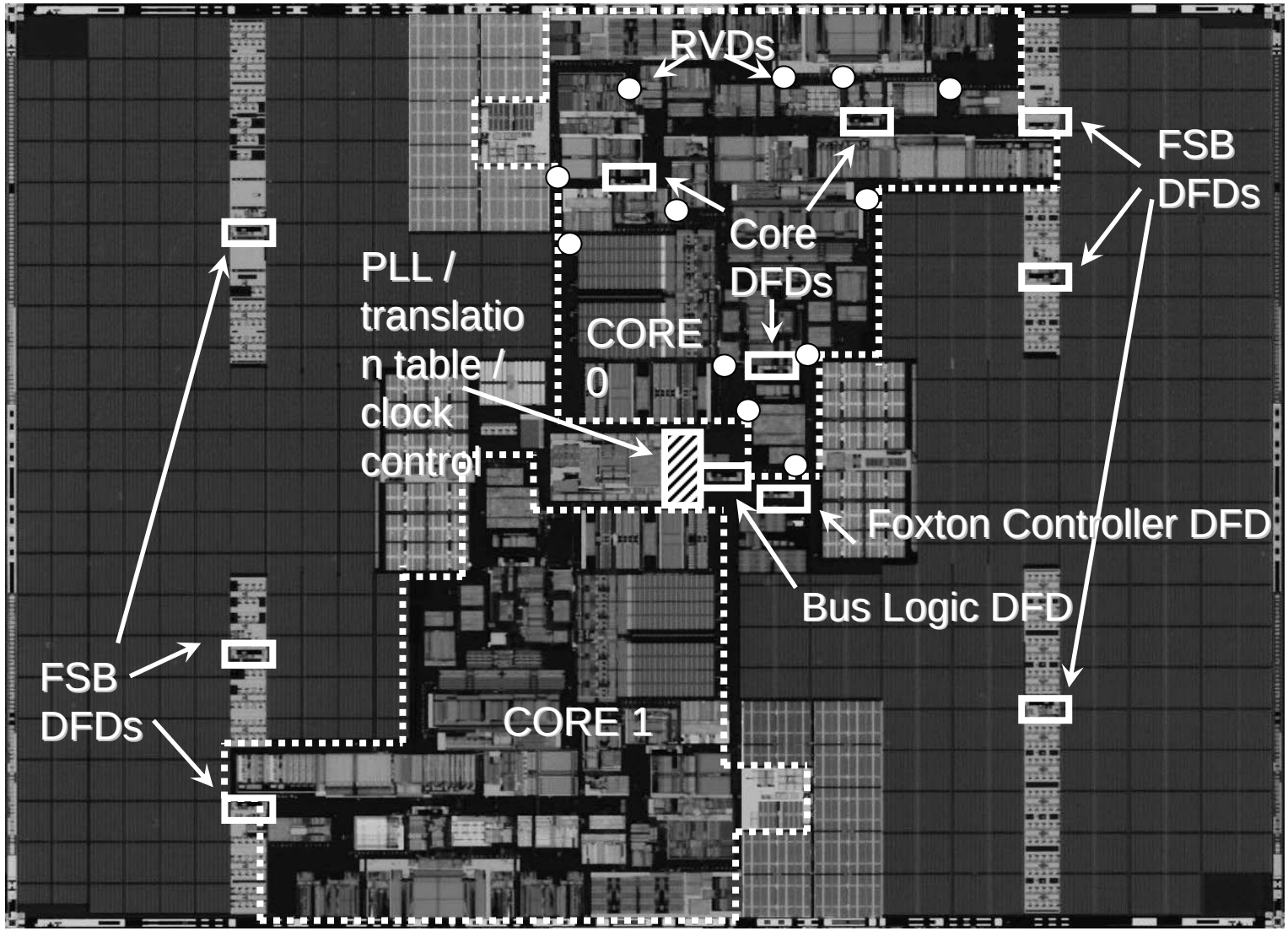
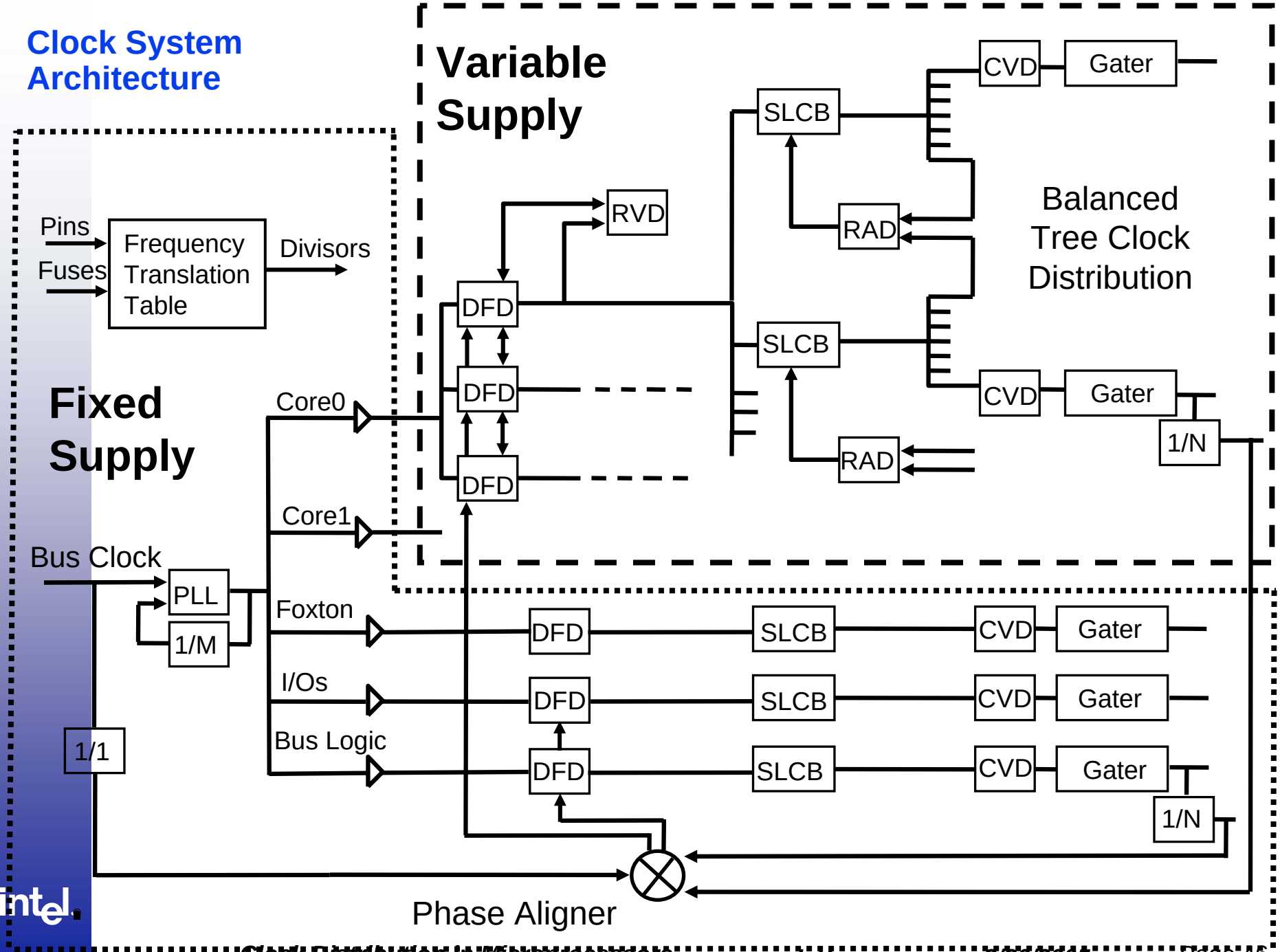
Montecito Clock System Floorplan



References: ISSCC 2005 Paper 16.1, T. Fischer et al,
ISSCC 2005 Paper 16.2, P. Mahoney et al

Clock System Architecture



Montecito Clock Distribution Summary (1)

- Core Clock Frequency controlled real-time based upon DC and transient power supply voltage
  - Montecito/Foxton Power delivery sets DC supply voltage based upon power dissipation (temp. sensors around the chip) of 100W. No worst case power.
  - Ldi/dt supply noise transients slow critical paths and reduce the operating frequency for a few cycles. Constantly varying frequency responds to the core supply voltage transient behavior.
- Regional Active Deskewing system reduces the process voltage and temperature sources of skew across the 21.5mm x 27.7 mm die.
- Clock Venier Devices (CVD) inserted at each local clock buffer allow 70ps of adjustment via Scan control.
- The clock distribution system consumes less than 25W for the 30mm route from PLL through the clock tree to all the Latches.

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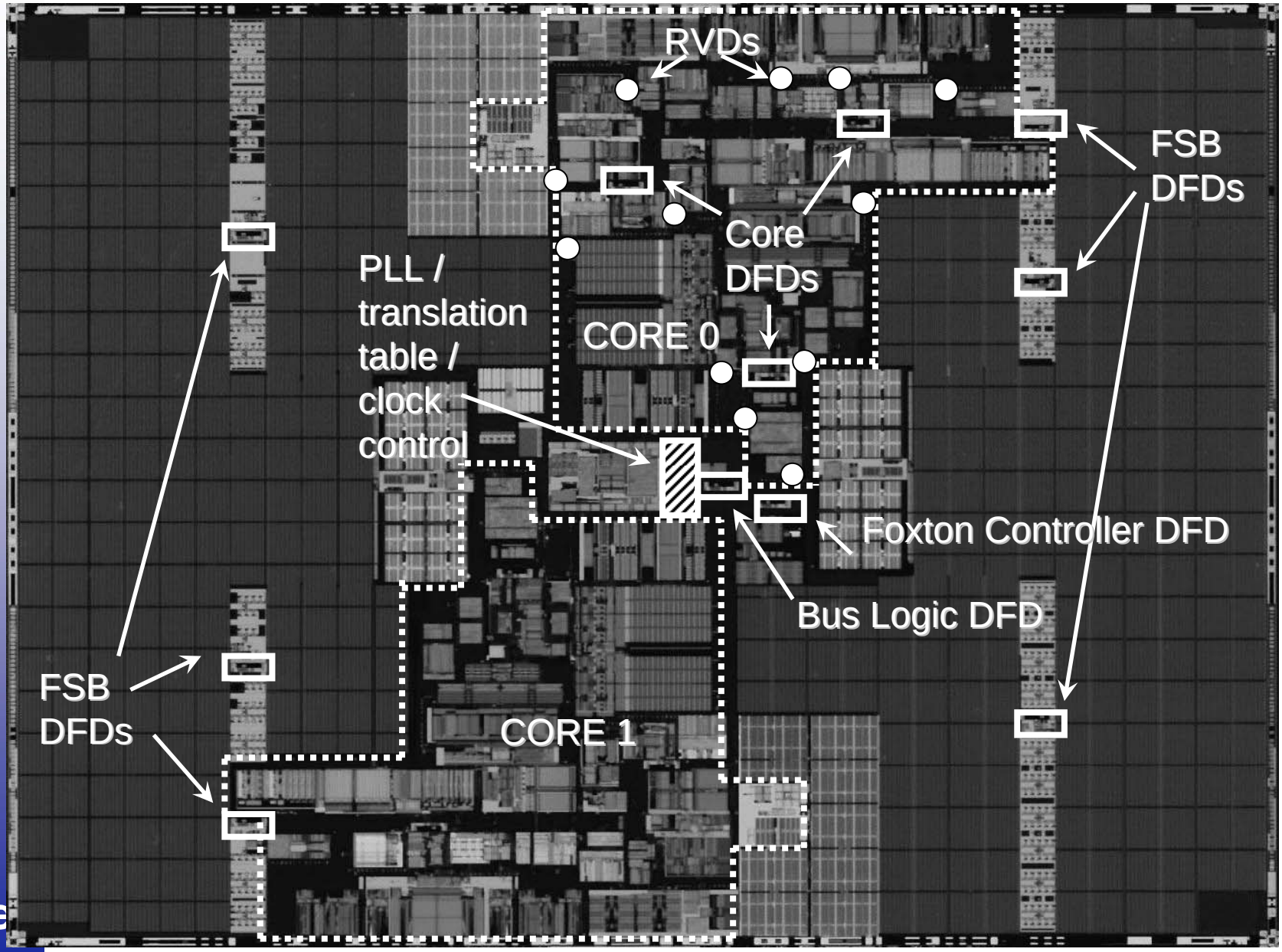
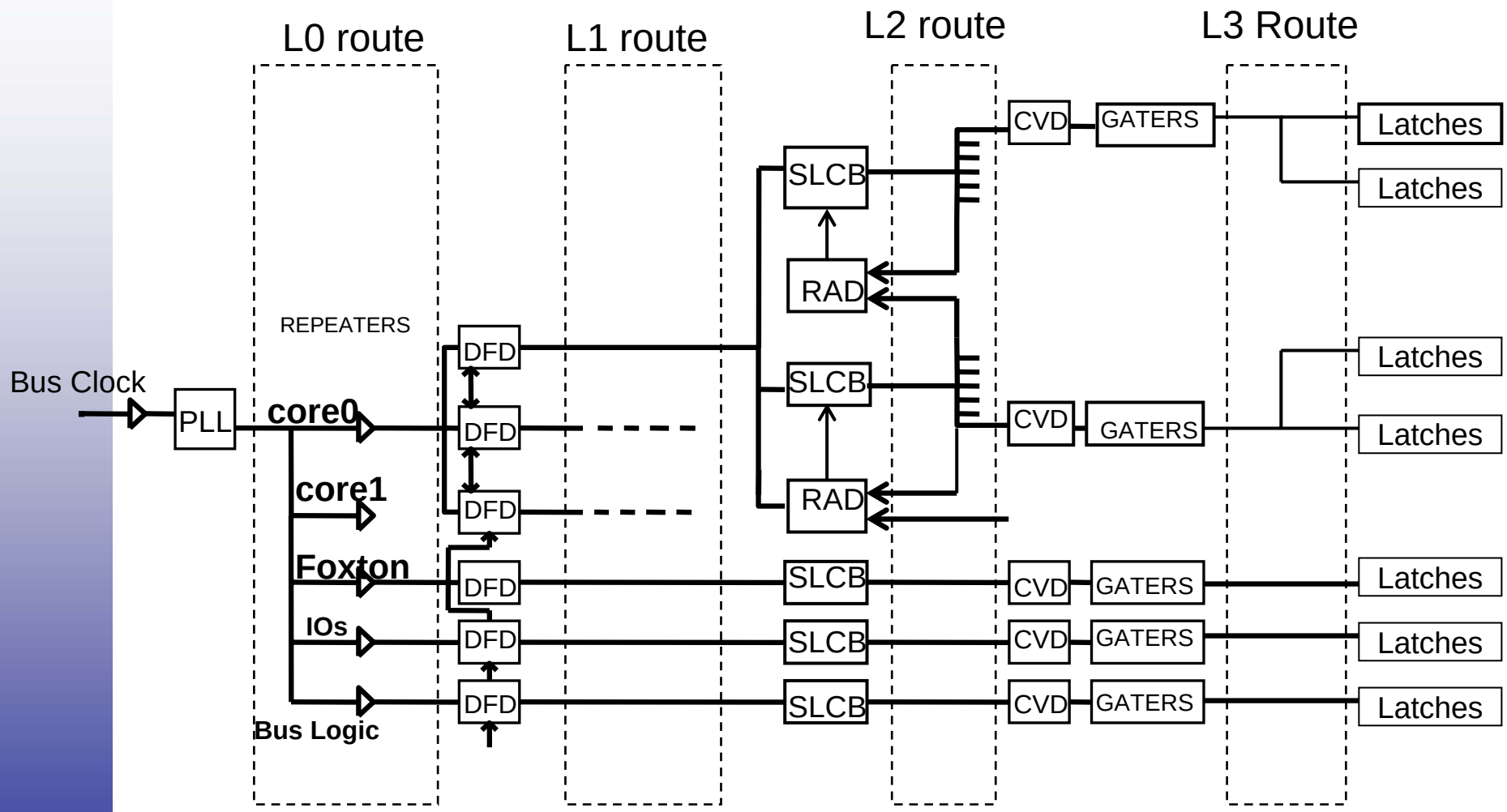


Overview with block diagram



Fixed frequency
Low Voltage Swings

Variable Frequency Full Rail Transitions

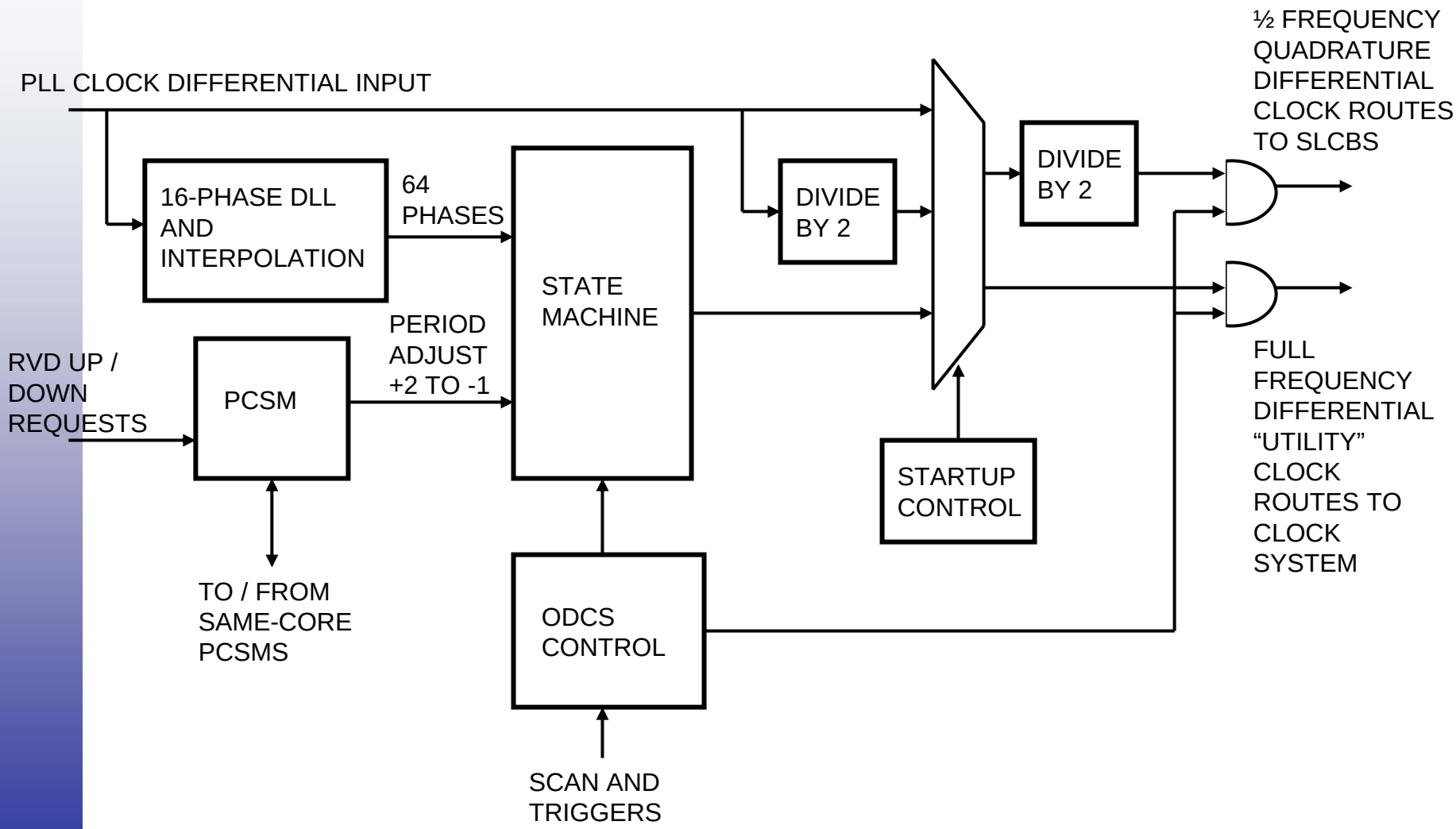
Differential

Single Ended

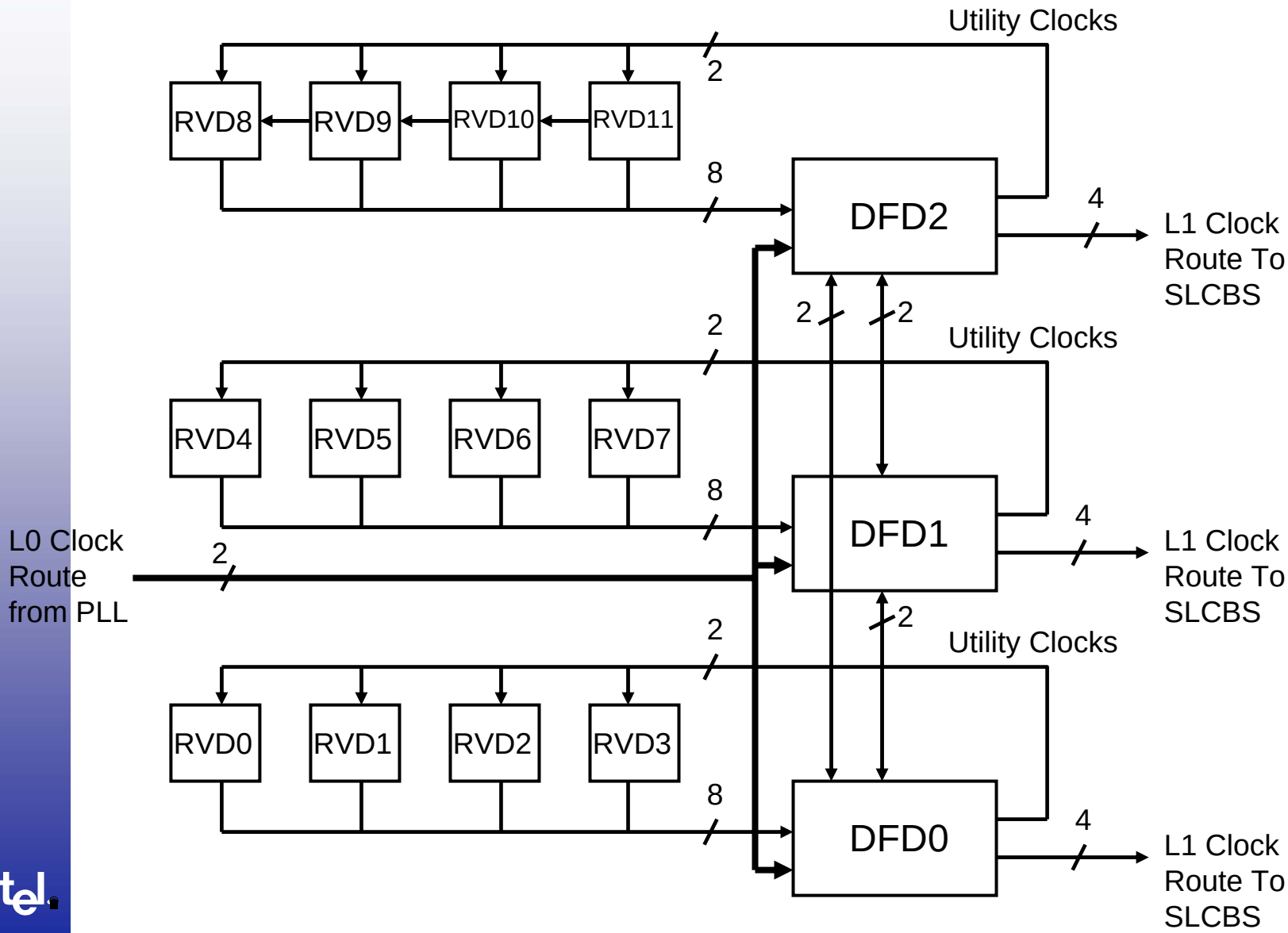
Montecito Clock Distribution Summary (2)

- The LO clock route is differential with 400mV swig and resistive load at the end of each line (length = 20mm)
  - Line width tapering is used
  - A self-biased differential amplifier is the repeater
- L1 route (length = 2mm) from the Digital Frequency Divider (DFD) to the Second Level Clock Buffer (SLCB) is distributed as a half frequency 0° / 90° clocks that are XOR'd in the SLCB and not duty cycle sensitive
- L2 route (length=3mm) from SLCBs to the Clock Venier Device has < 6ps skew using optimization with a CAD timing tool.
- L3 route (length = 2mm), from the CVDs through the clock gaters to the Latches, provides an overall clock skew adjustment to < 10ps to the Latches controlled by test scan

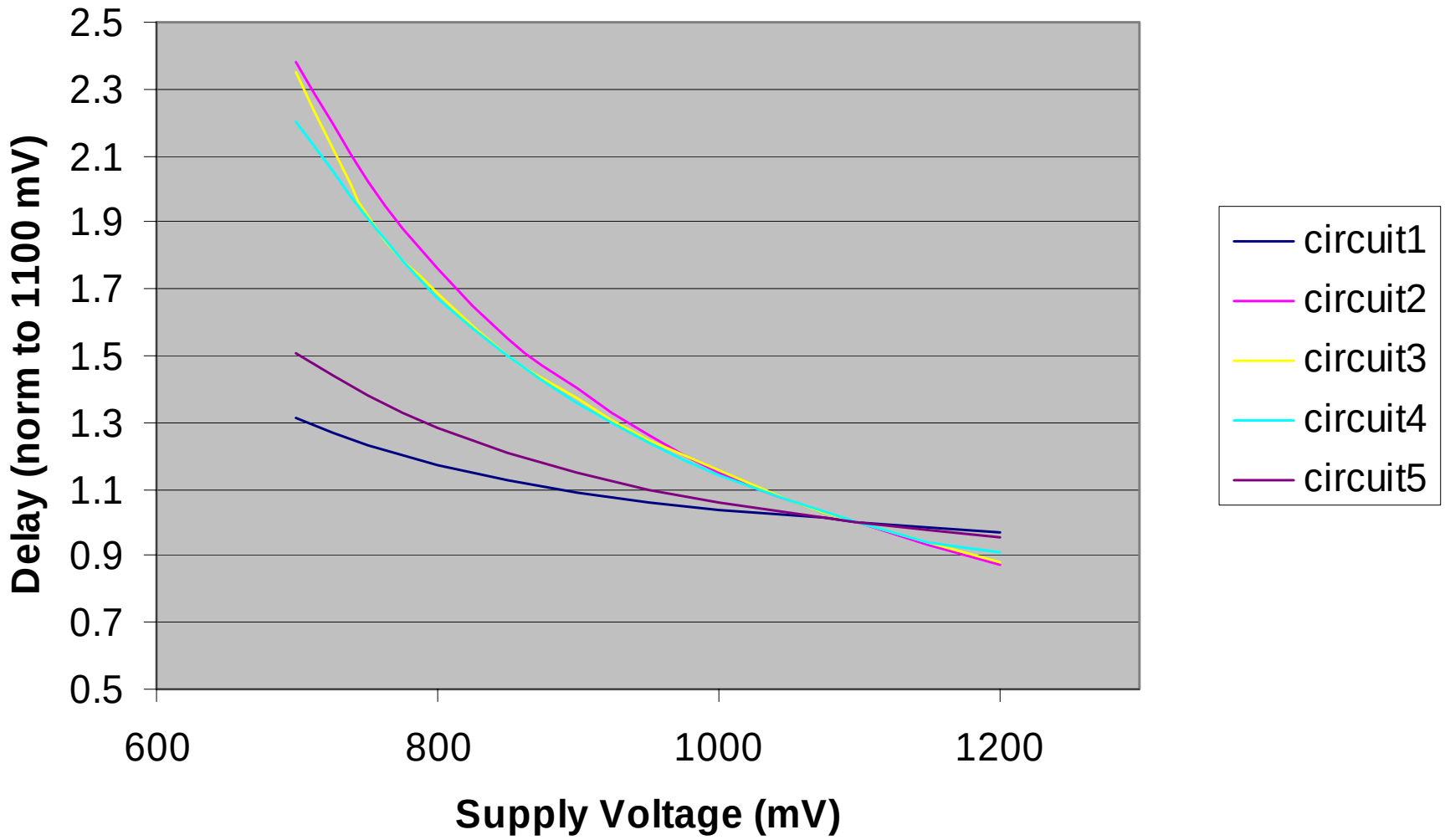
Digital Frequency Divider (DFD) Block Diagram



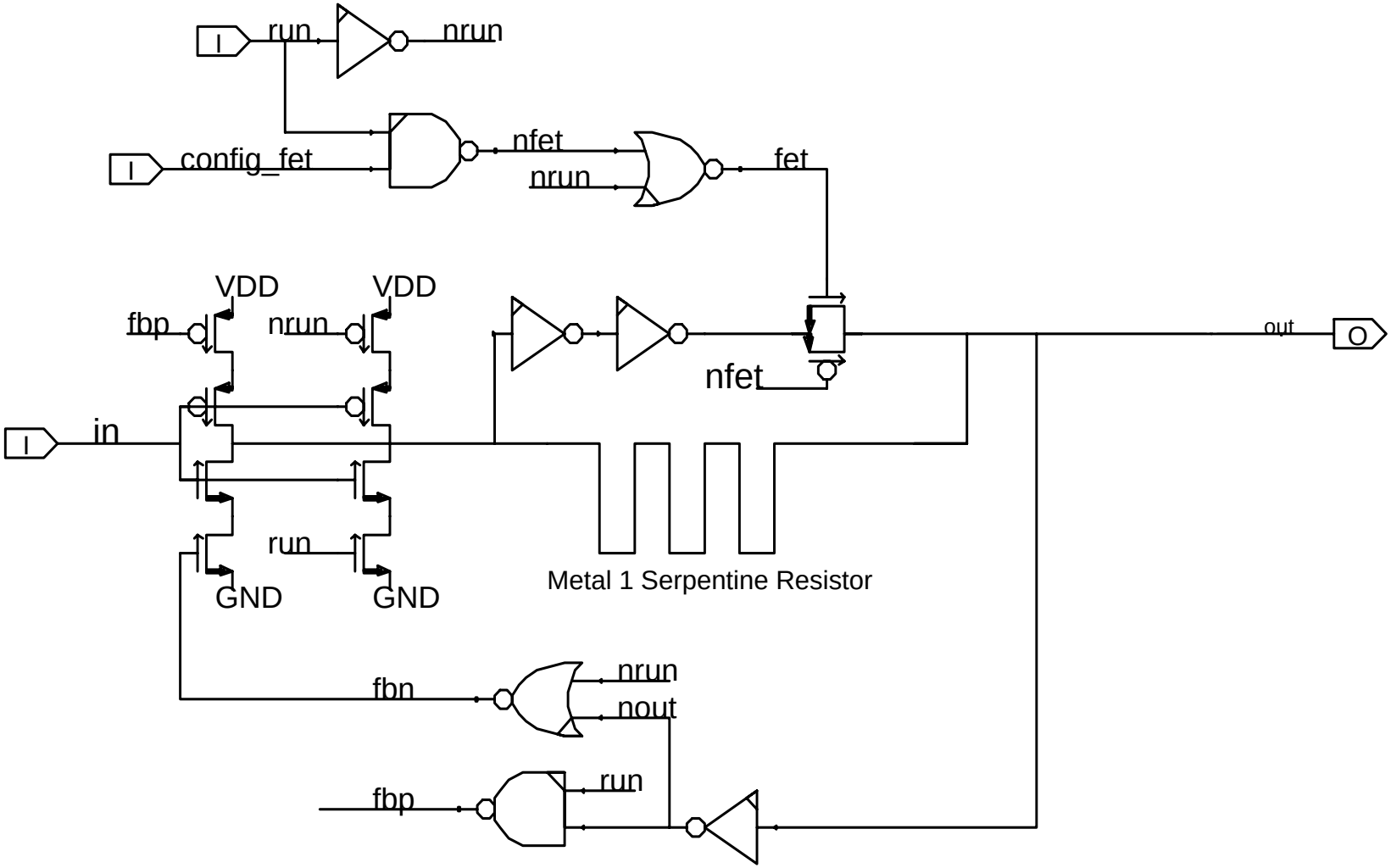
Voltage-to-Frequency Conversion (VFC) Per Core



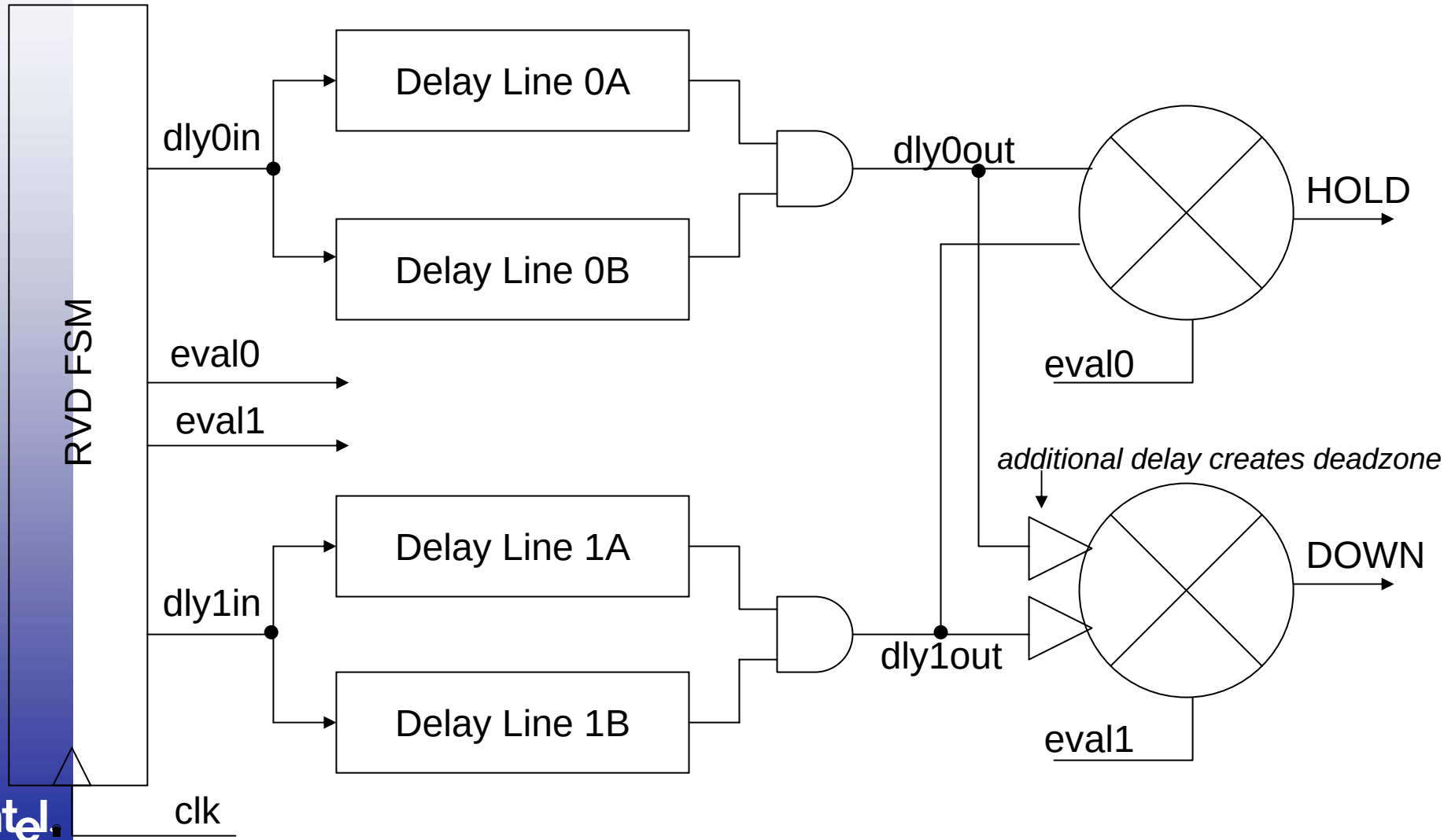
Variable Frequency Mode: CMOS Critical Path Scaling



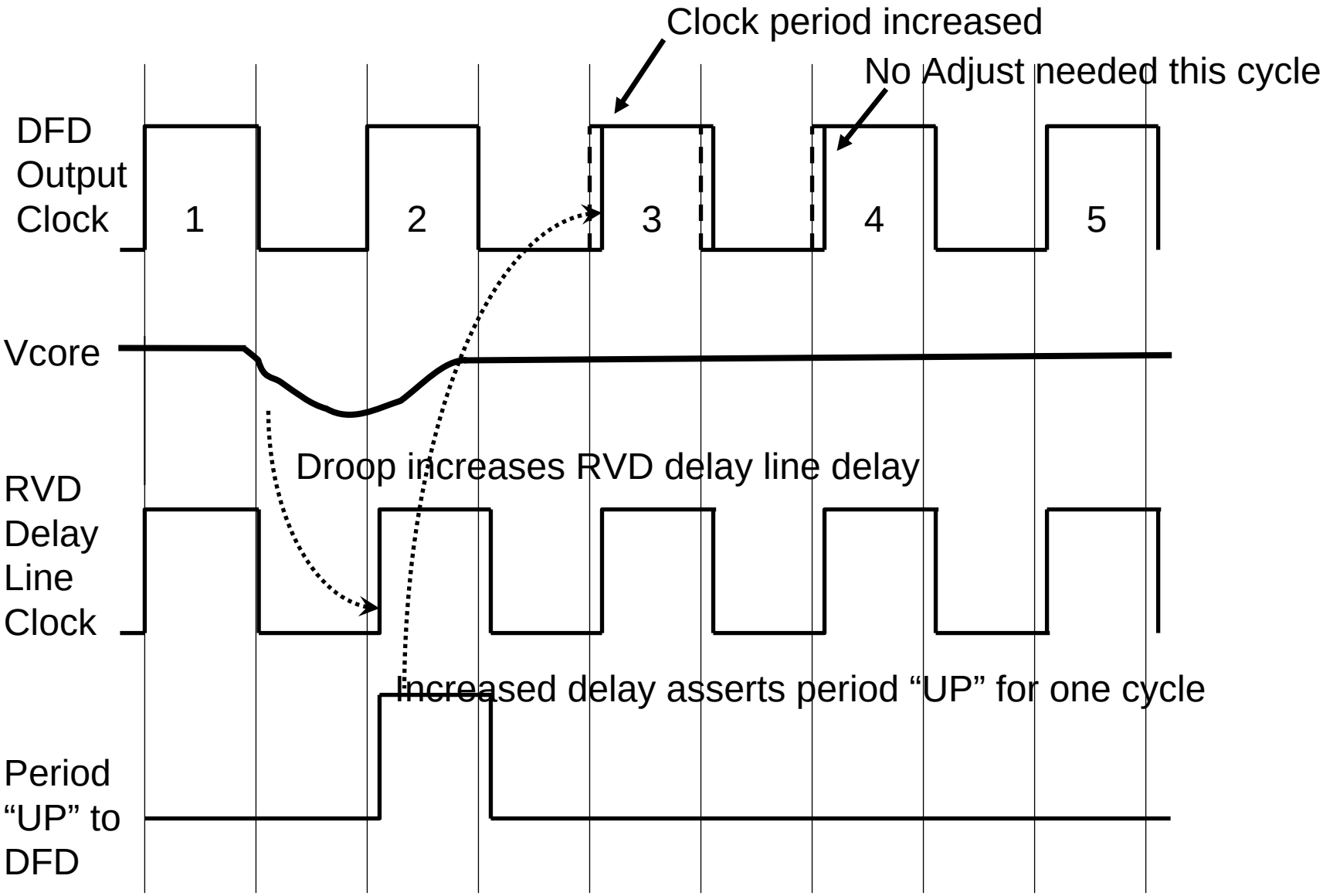
RVD Coarse Delay Element



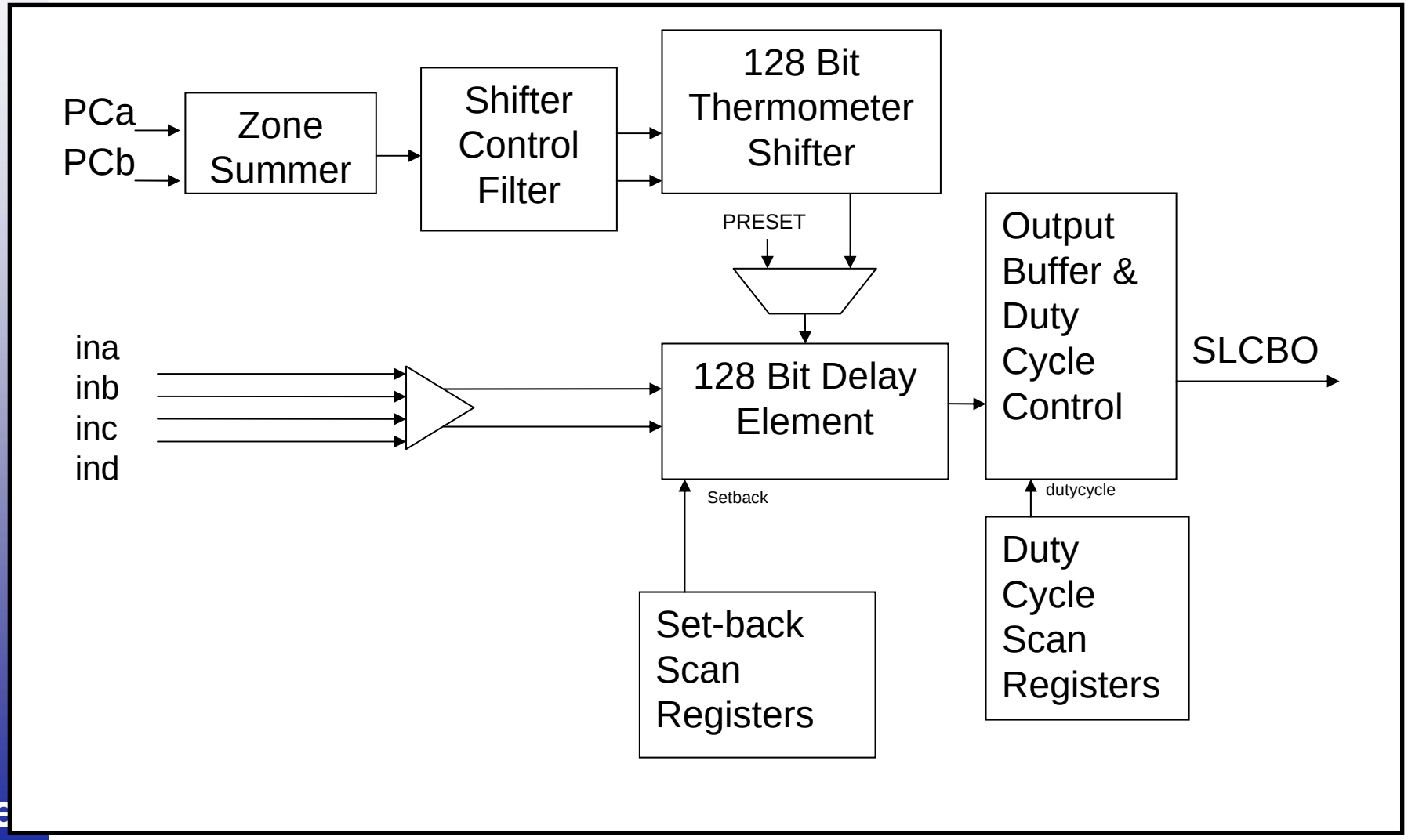
RVD Block Diagram



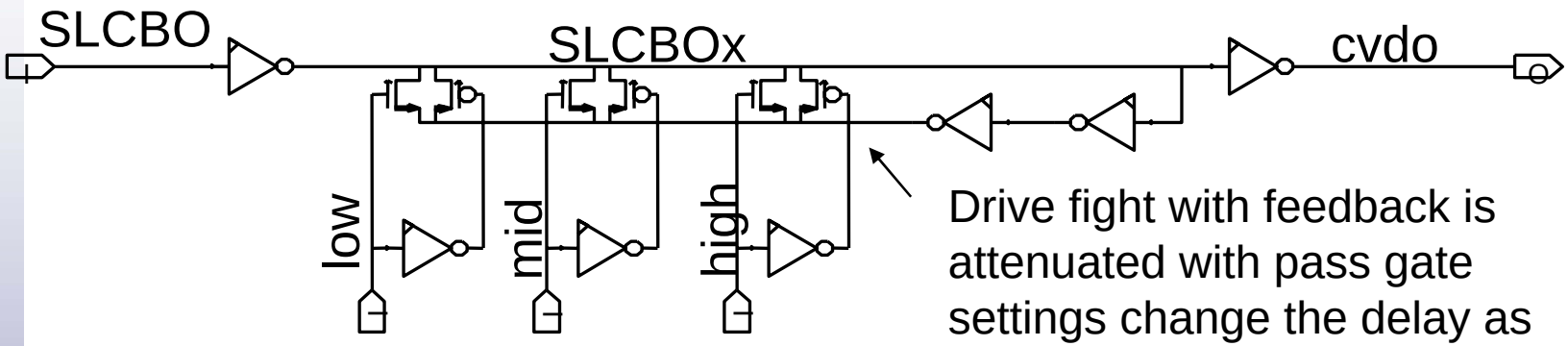
Example VFC Supply Droop Response



SLCB Block Diagram

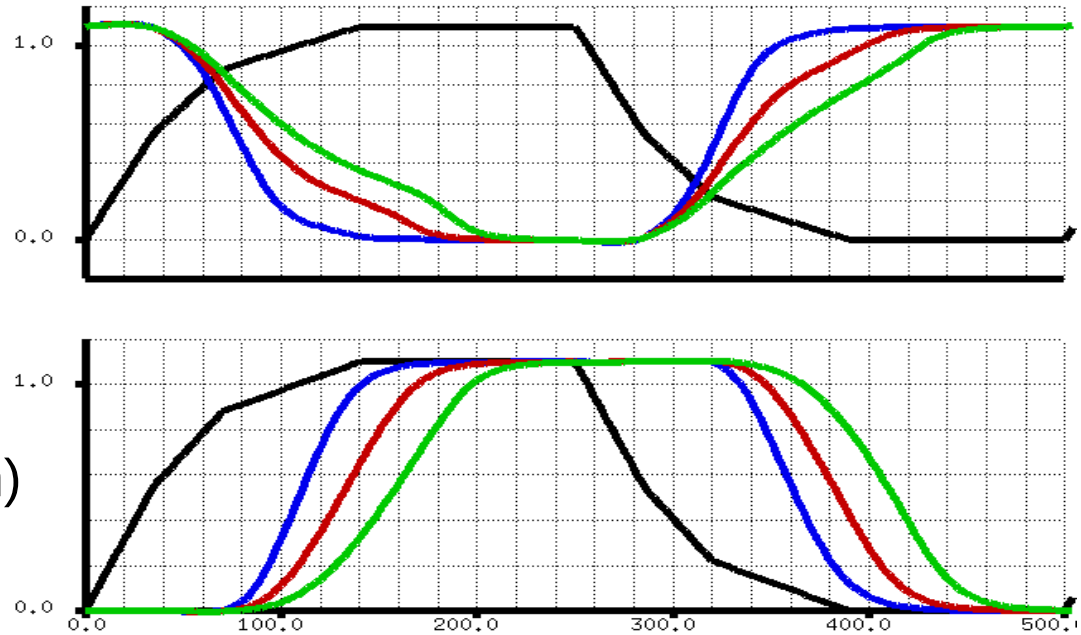


CVD Circuit and Operation



Drive fight with feedback is attenuated with pass gate settings change the delay as desired

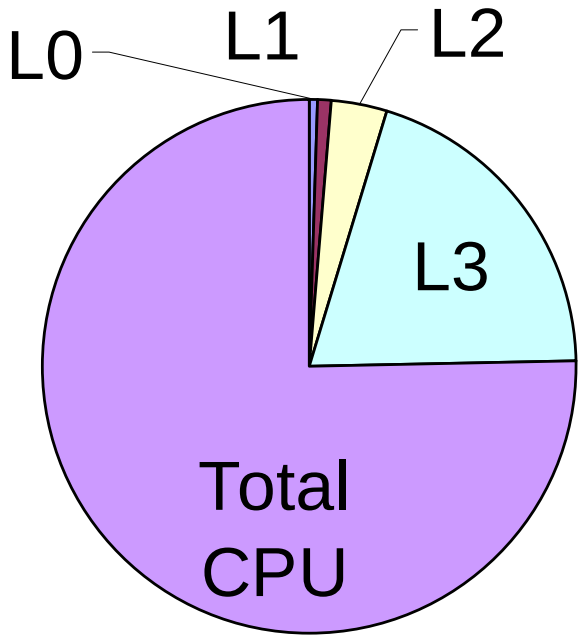
SPICE simulations showing low, mid and high delay settings for SLCBOx (top graph) and CVDO (bottom graph)



Route Statistics and Power

Route	Terminals	Distance	Delay
L0	14	20mm	640ps
L1	71	5mm	215ps
L2	14500	2-3.3mm	60ps
L3	~5 million	0-1.5mm	12ps

Route statistics



Power dissipation contribution by route

- Highest load and most power dissipated in the L3 route.
- Future research into low-power clock distribution should focus on last section of route.

Evolution in Clock Distribution

1991
- 486: PLL on-chip to remove the large clock distribution delay (zero delay buffer). Clock RC skew minimized across chip with metal.

1993
- Pentium: Clock tree with length “tuning” for skew balancing.

1995
- Pentium II: Clock Binary Tree in center Spine with branch length “tuning” to local clock buffer for skew balancing.

1998
- Itanium I: Lightly loaded “balanced” reference clock routed with the highly loaded “unbalanced” clock tree - actively adjust clock buffer delay for low skew (at product test).

2000
- Pentium IV: Three binary tree Spines with “tunable delays” and Phase Detectors distributed across the die. Blow fuses (based upon compare algorithm at test).

2004
- Itanium (Next Gen):
  - Differential global clock distribution (20mm).
  - Digital Frequency Divider (synthesizer) adjusts frequency in 1.6% steps within 2 cycles based upon measured local supply.
  - Regional Active Deskew adjusts Second Level Clock Buffer delay for low skew (done during test)
  - Local clock buffer variable delay adjust to load (flip-flops) by design (time borrowing)

Complexity

Summary / Future Directions

- Clocking systems have evolved with even more complex electrical methods
  - Trimming and active feedback de-skewing circuits developed
  - Transient Frequency adjust based upon local supply voltage
- Design the micro-architecture with interconnect delay in mind
- Exploit locality for frequency scaling
  - Logic / clock domains
- Clock Distribution Power will take a larger % of the total chip power

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