A Tutorial on Delay Fault Testing

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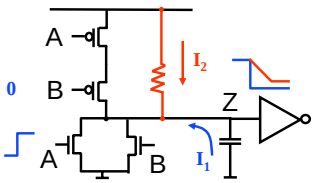
Outline

- **Defects**
  - Manufacturing Defects
  - Design Errors
  - Process Variations
- **Delay Fault Models**
- **Transition Faults**
- **Path Delay Faults**
  - Robust Path Test
  - Non-robust Path Test
- **Segment Delay Faults**

Manufacturing Defects

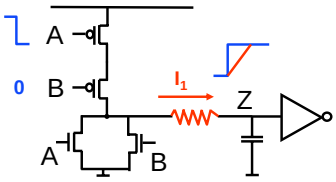
- **Certain manufacturing defects do not change the logic function of the chip, but can cause timing violations**

♦ Resistive Bridges



0-to-1 Transition on A is delayed, but 1-to-0 Transition on A is speeded up!

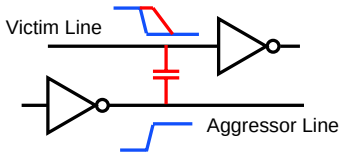
♦ Resistive Opens



Both 0-to-1 and 1-to-0 Transitions On A are delayed.

Design/Manufacturing Defects

- **Aggressive Place and Route**
  - Aggressive Design Rules with reduced guard bands
  - "Under-designed" Power grid (IR-drop slows circuits)
  - Interconnection spacing "too close" (Coupling slows circuits)
- **Abnormal Statistical Variations in Geometry**
  - Affect Line spacing and Line Thickness
- **Process Variations**
  - Gate Threshold variations



Defects and Delay Faults

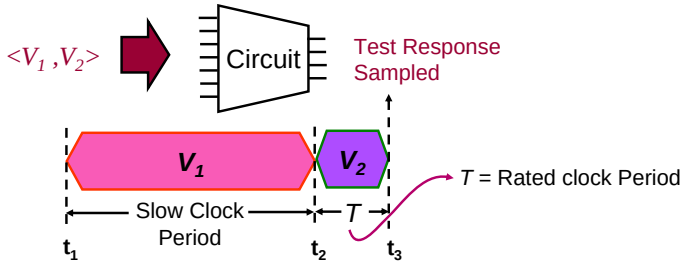
- **Hard Shorts and Opens**
  - Testable by stuck-at test with high confidence
- **Resistive Shorts**
  - May be testable by Stuck-at test but more likely to be detected by a Delay Test
- **Resistive Opens and Coupling faults**
  - Can only be Detected by a Delay Test
- **Resistive Power Supply lines**
  - Excessive IR-drop can be detected by Delay Test
- **Process Variations**
  - Can only be detected by a Delay Test

Delay Fault Testing

- **Propagation delays of all paths in a circuit must be less than the clock period for correct operation.**
- **Functional tests applied at the operational speed of the circuit are often used to test for delay faults.**
- **Scan based stuck-at tests are often applied at speed**
- **However, functional and stuck-at testing, even if done at-speed, do not specifically target delay faults.**
- **Tester limitations will prevent at-speed functional testing in the future.**

Two Vectors Delay Test

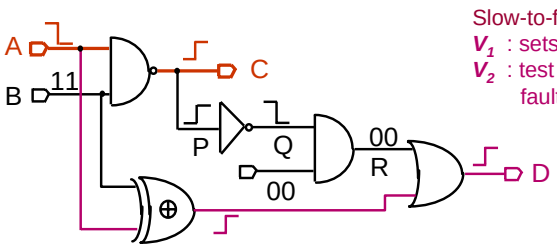
- **Delay Fault Test Methodology**
  - Two Vector Sequence <V_1, V_2>, Initializing Vector followed by Transition Launching and Propagating Vector.



Delay Fault Models

- **All Delay fault models in use today are logic models *Independent of Circuit Delays***
  - **Transition Faults** : Assumes *large delay defect* concentrated at one logical node, such that *any* signal transition passing through this node will be delayed past the clock period.
  - **Path Faults** : Assumes a distributed delay along a combinational path from latch to latch.
- **A new delay fault model***(Heragu and Patel 1996)*
  - Segment Delay Fault Model : Assumes distributed delay along a small segment of a long path.

Transition Delay Fault Model



- **Transition propagation along short path** A-C → **Small delay defects may not be detected**

Test for Transition Faults

- **Slow-to-rise (0 to 1) transition on line k**
- **A two-pattern sequence <V1, V2> is a test for slow-to-rise fault on line k if**
  - V1 sets line k to 0
  - V2 tests line k stuck-at-0
- **Slow-to-fall (1 to 0) transition**
- **A two-pattern sequence <V1, V2> is a test for slow-to-fall fault on line k if**
  - V1 sets line k to 1
  - V2 tests line k stuck-at-1

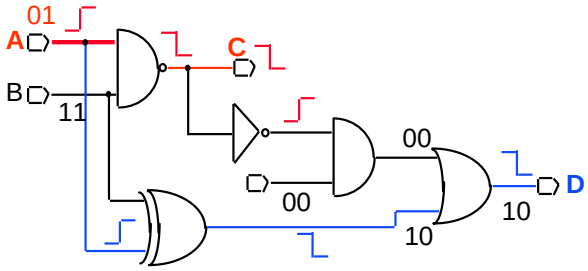
Transition Delay Fault Model

- **Advantages:**
  - May detect delay defects like shorts, coupling defects, opens etc. missed by stuck-at-tests
  - Practically Very Useful
    - Stuck-at-fault CAD tools with minor modifications
    - Fault lists, Coverage Metrics similar to stuck-faults
- **Disadvantages:**
  - May miss distributed and small delay defects
  - Smaller cycle times imply more sensitivity to small delay defects
  - Intel: more high resistance bridges in 0.18u as compared to 0.25u [ITC '99]
  - IBM: more small delay defects than large [ITC '00]

Path Delay Fault Model

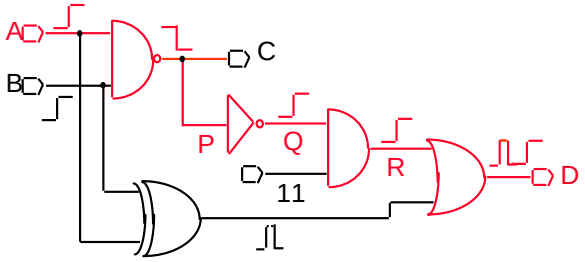
- **A path is a sequence of connected gates from a circuit primary input to a primary output**
- **A path delay fault is said to have occurred if the delay of a path is more than the specified clock period of the circuit**
- **Features:**
  - Models distributed delay defects
  - Path delay fault tests are more likely to detect small delay defects
  - Much more complex than transition delay model
  - Low fault coverage

Transition Fault Test



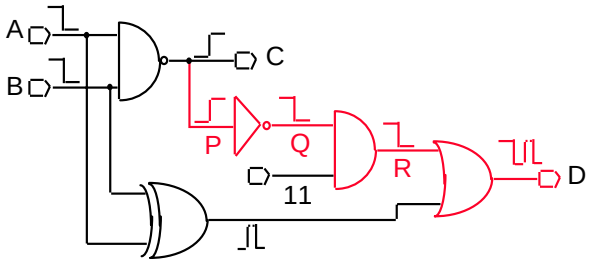
- A large delay defect on line A will be detected at pin C if delay on path A-C exceeds specifications
- A small delay defect on line A may not make delay of path A-C large enough to be detected. It should be tested through long path A-D to be detected.

Path Delay Test



- Path A-P-Q-R-D is tested for rising transition at pin A. Small delay defects distributed along the path will be tested if the cumulative delay exceeds specification.

Segment Delay Test

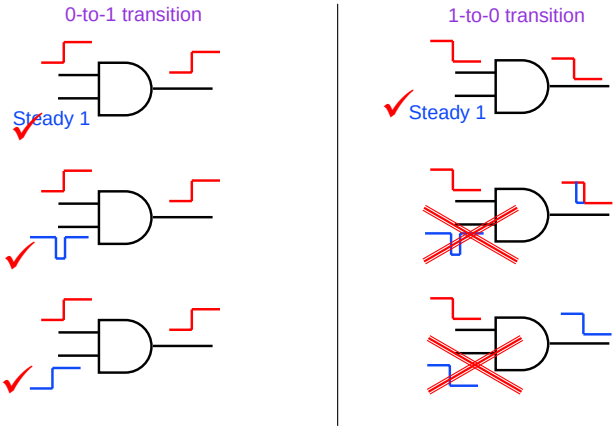


- Path A-P-Q-R-D is Untestable for falling transition launched at A, but part of its segment, namely segment P-Q-R-D is testable.

Path Tests

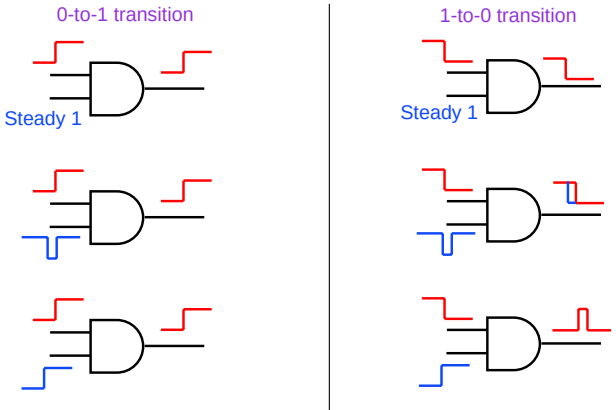
- **Robust Path Test**
  - Guarantees to Detect the Delay Fault on the Targeted Path Independent of all other delays in the circuit.
- **Non-robust Path Test**
  - Guarantees to Detect the Delay Fault on the targeted Path only if no other path delay is increased
  - Present Logic models based on the above definition are “weak”
    - Many situations exist where a Non-robust test is invalidated, meaning it fails to detect the targeted path delay fault.

Robust Test Conditions



*In each case **On-Path** is upper input, other input is called **Off-Path** or **Side** Input*

Nonrobust Test Conditions



Only requirement on the side-input is that the Second Vector value be 1

Robust Test Conditions

- **AND Gate**
  - To propagate a 0-to-1 Transition from the input of an AND gate, all other side inputs of the AND gate must have value 1 on the second vector.
  - To propagate a 1-to-0 Transition, all other side inputs of the AND gate must have a *steady glitch-free logic value 1 on both vectors.*
- **OR Gate**
  - To propagate a 0-to-1 Transition from the input of an OR gate, all other side inputs must have a *steady glitch-free logic value 0 on both vectors*.
  - To propagate a 1-to-0 Transition, all other side inputs must have 0 on the second vector.

Functionally Sensitizable Paths

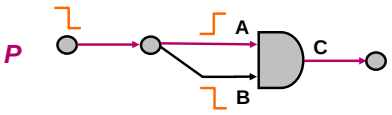
- **AND Gate**
  - For On-path input 0-to-1 Transition, the side input must be a 1 for the second vector
  - For On-path input 1-to-0 Transition, the side input must not be a steady-0 during both test vectors
- **OR Gate**
  - For On-path input 1-to-0 Transition, the side input must not be a steady-1 for both test vectors
  - For On-path input 0-to-1 Transition, the side input must be a 0 for the second vector
- **Functionally Un-Sensitizable Paths**
  - If any of the above conditions is not met, it is Un-Sensitizable
  - Also called Functionally Redundant Paths. Such paths have no effect on the timing of the circuit

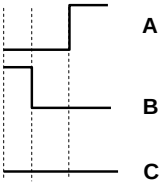
Path Delay Fault Tests

Set of all paths in the circuit

Functionally Redundant	Functionally Irredundant Or Functionally Sensitizable

- Do all paths affect circuit timing? **NO!**





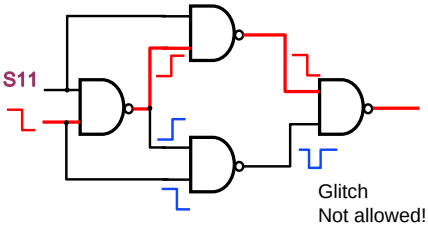
- Delay defect on path ***PAC*** can never cause a timing violation

Path Delay Fault Tests

Set of all paths in the circuit

Functionally Redundant	Functionally Irredundant / Sensitizable Robust

Many Functionally Sensitizable paths are not robustly testable!

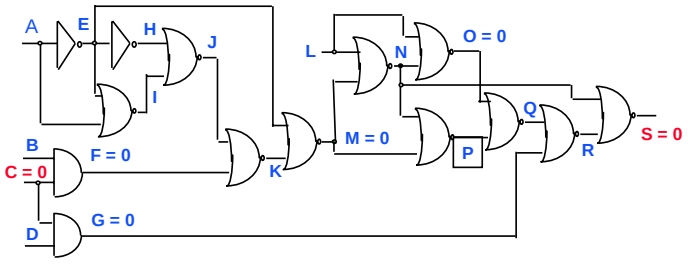


Fast Identification of Untestable Path Delay Faults

- **Input: some set of Logic Implications of both value assignments (0 and 1) for lines**
- **Output: pairs of lines such that every path passing through each pair is untestable for some combination of signal values.**
- **Identifies a large percent of untestable faults very quickly without a test generation**
- **Identifies robustly untestable, non-robustly untestable, and functionally unsensitizable faults**

Reference: *K. Heragu, J. H. Patel and V. D. Agrawal, "Fast identification of untestable delay faults using implications," Proc.IEEE/ACM Int. conf. On Computer Aided Design (ICCAD-97), pp. 642-647, Nov. 1997*

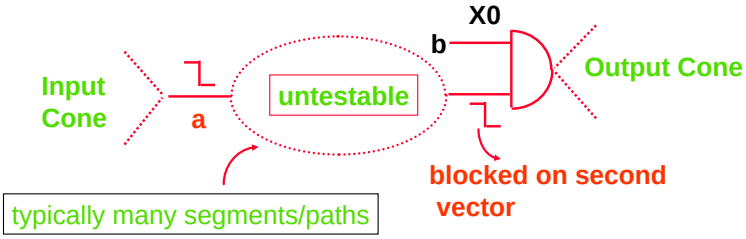
Example: portion of c6288



- **(C=0) => (S=0)**
- **Odd-parity paths between c and s that require 0 on c are unsensitizable (not explicitly enumerated)**

V_2 sensitization

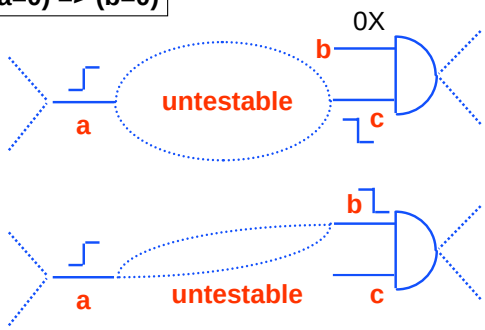
Given: (a=0) => (b=0)



➔ **works for robust and non-robust criteria**

V_1 sensitization

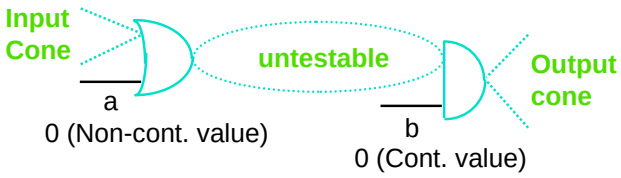
Given: (a=0) => (b=0)



➔ **works for robust criteria. Specific combination of transitions**

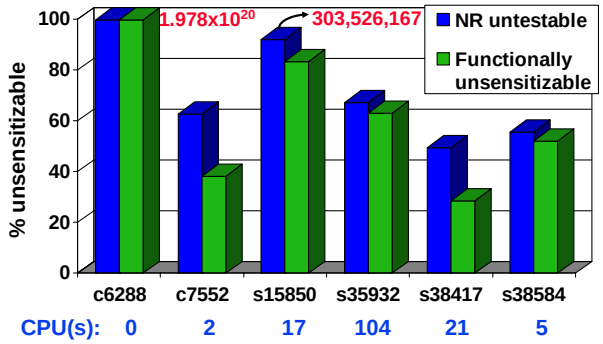
Necessary propagation values

Given: (a=0) => (b=0)



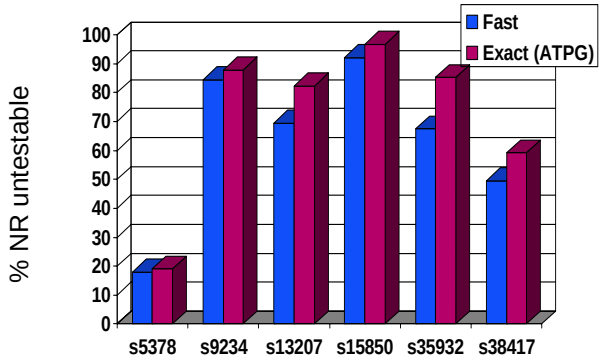
➔ **works for robust and non-robust criteria**

Unsensitizable paths



➔ **Cycle time can be computed independent of Functionally Unsensitizable paths**

Comparison with exact results

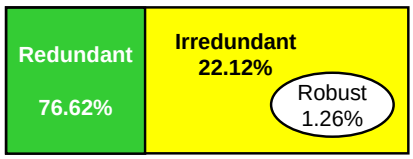


➔ **Implication based fast identification gives only a lower bound on the number of untestable faults.**

Limitations of the Path Model

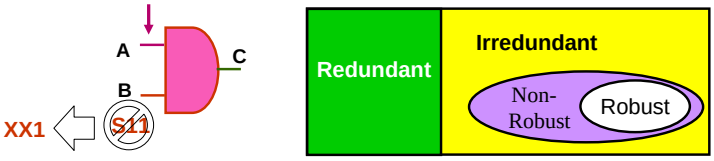
- **The number of paths in a circuit can grow exponentially with circuit size**
  - Fault Simulation, Test Generation etc. computationally expensive
  - Large Test Set Sizes: longer test application time
  - s38584: 3.6×10^4 stuck-at-faults; 2.2×10^6 path delay faults
- **The number of robustly testable paths in typical circuits is much less than the number of irredundant paths**
  - S1269

Longest Paths
Untestable: 105.3ns
Testable: 43.5ns



Getting More Path Coverage

- Non-robust tests: More paths can be tested if the steady non-controlling value condition on the side input is relaxed.
  - Such tests can be invalidated by specific delays

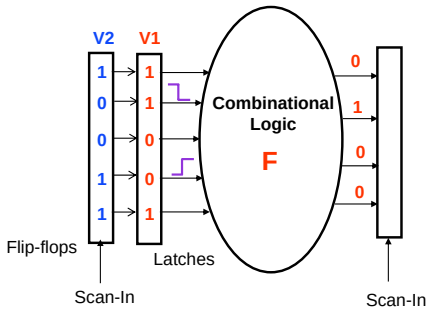


- Multiple Path Delay Faults: Paths that are not non-robustly testable but irredundant, can be covered by generating tests for multiple path faults
  - Much more complex model

Scan Based Delay Fault Testing

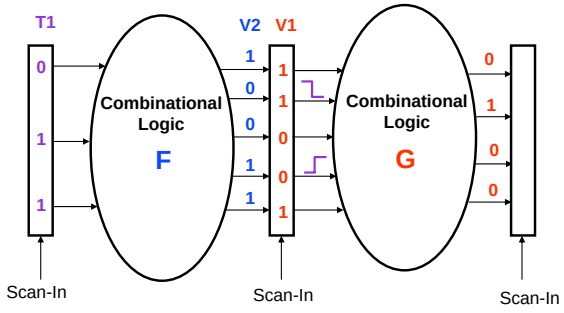
- **For full-scan circuits, three alternative approaches can be used to apply two-pattern tests**
  - A special 3-latch scan cell (or one scan flip-flop plus one latch, "enhanced scan") is used that holds two values, one for the initialization vector and one for the transition vector.
  - Functional Transition Method: First vector is scanned in, the second vector is the functionally generated (also called Broadside test)
  - Skewed-Load Transition Method: First vector is scanned in, the second vector is one-bit shift of the first vector.

Enhanced Scan



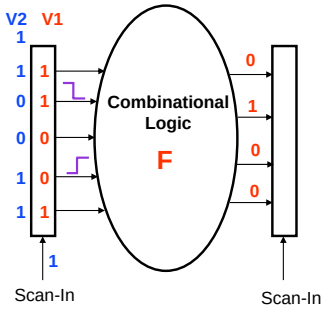
1. Scan in the first vector V1
2. Latch the scan ffs outputs into the latches
3. Scan in the second vector V2
4. Make latches transparent (launches transitions)
5. Capture response

Functional Transition Method



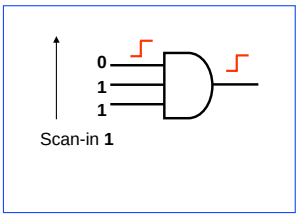
1. Scan in the first vector (T1 and V1)
2. Apply system clock once (Launches Transition from **V1** to **V2 = F(T1)**)
3. Apply system clock second time (Captures response **G(V2)**)
4. Scan out the response

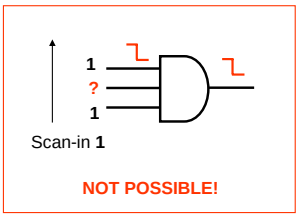
Skewed-Load Transition Method



1. Scan in the first vector V1
2. Shift scan register once (Launches Transition from **V1** to **V2 = shift(V1)**)
3. Apply system clock (Captures response **F(V2)**)
4. Scan out the response

Skewed-Load Transition Method





In practice, loss of transition fault coverage due to skewed-load restriction is small in large circuits. The loss in coverage can be further reduced by Rearranging scan flip-flops and/or inserting dummy flip-flops.

Transition Faults: Summary

- **An idealized, abstract fault model, but practically very useful fault model**
  - Set line K to value 0, then test for K-stuck-at-0
  - Set line K to value 1, then test for K-stuck-at-1
- **Only minor modifications required to existing CAD tools for stuck-at faults**
  - Fault lists and Coverage Metrics are well-defined
- **May detect many Shorts and Opens missed by stuck-at tests**
- **May detect some Capacitive Coupling faults**
- **Distributed and small delay defects may not get covered**
- **Critical paths are not explicitly targeted**

Path Delay Faults: Summary

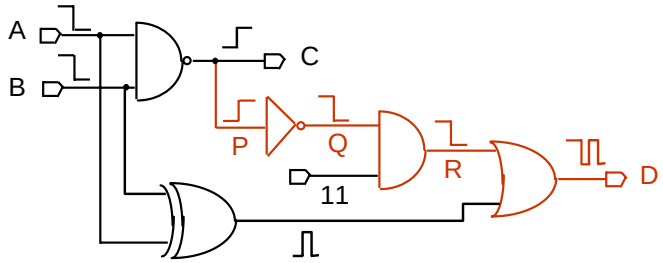
A path whose propagation delay exceeds the specified worst case delay is said to have Path Delay Fault

- **Advantages**
  - Can take care of distributed delays
  - Covers most Transition Faults
  - Much more rigorous test compared to transition test
  - May detect more defects than transition test
  - Can target Critical Paths
- **Disadvantages**
  - The number of paths in a circuit may be very large
  - Fault Coverage is usually very low, giving no help in deciding how much is enough!
  - CAD tools are less mature

Delay Test Recommendations

- **As a minimum perform Transition Tests for all nodes corresponding to the stuck-at list**
- **Use a timing analyzer to identify "critical" paths**
  - Use a reasonable delay threshold, e.g. paths with delays >95% of the clock period.
  - If the number of critical paths is too many, select a random sample
  - Use a path-delay test generator to identify redundant and untestable paths
  - If most paths are untestable than increase the sample size or reduce the critical path delay threshold – OR – use Segment Test!

Uncovered Segments



- **Paths A-P-Q-R-D and B-P-Q-R-D are Untestable for falling transition, but part of their segment, namely segment P-Q-R-D is testable.**

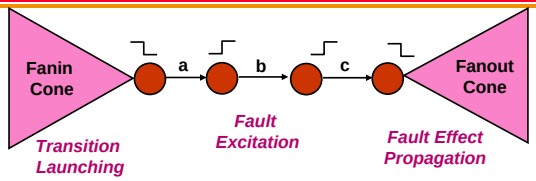
Note: Paths APQRD and BPQRD can be tested as a multiple-path fault, however, identifying such multiple-path faults is very hard.

Segment Delay Fault Model

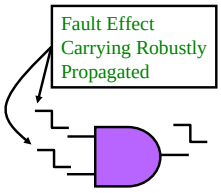
- **A physical segment is a sequence of connected gates, i.e., a section of a full path**
- **Segment Delay Fault Model considers 0-to-1 and 1-to-0 transitions on all segments of length L**
- **The parameter L can be chosen based on defect statistics**
- **A segment delay fault causes a large enough increase in delay to result in a path delay fault on all paths passing through the segment**
- **Explosion in the number of faults can be prevented by keeping L small**

Reference: *K, Heragu, J. H. Patel and V. D. Agrawal, "Segment Delay Faults: A new fault model," 14th IEEE VLSI Test Symp. (VTS), pp. 32-39, April 1996.*

Robust Tests for Segment Delay



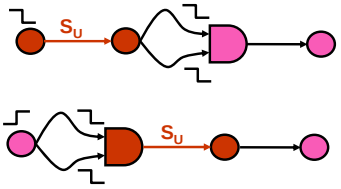
- **A vector pair is a robust segment delay fault test if:**
  - **(1) Launches the desired transition (with possible hazards) at the origin of the segment**
  - **(2) Propagates the transition robustly along the segment**
  - **(3) Propagates the fault effect robustly in the fanout cone to a primary output**



- **Test conditions slightly different from those for a robust path test in the Fan-in and Fan-out cones**

Testing Uncovered Segments

- ***Uncovered Segments*** **Some robustly testable segments may not be part of any testable paths**

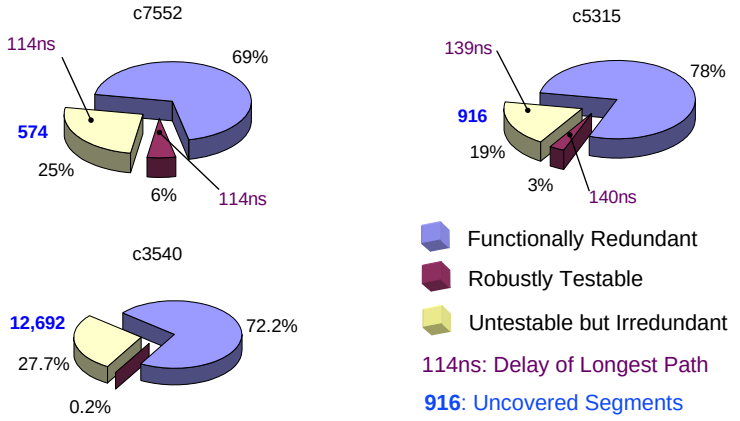


Multiple Fault Effect Propagation Conditions

No Condition on Transition Launching

- **Uncovered Segments are likely to be covered by complete Multiple Path delay fault test sets**
- **However techniques for identifying Multiple Path delay faults do not scale to large circuits**

Uncovered Segment Results

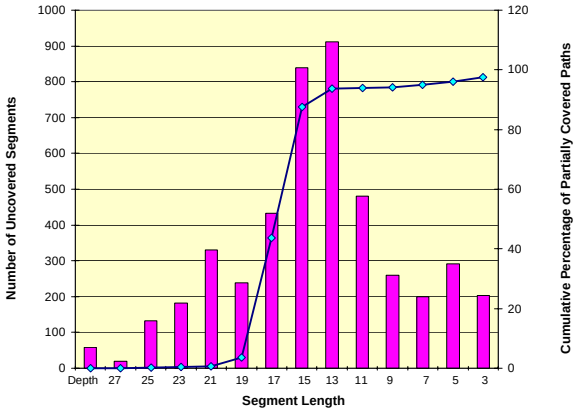


Critical Path Testing

- **A practical approach to improve the coverage of critical paths**
  - Step 1. Identify a set of critical paths using a timing analyzer
  - Step 2. Generate test for all testable paths
  - Step 3. Determine the set of untestable paths that are functionally sensitizable (irredundant)
  - Step 4. Determine the set of uncovered segments
  - Step 4. For each untested path find the largest *uncovered segment* of that path that can be tested
    - Find all paths that cover this tested segment and declare them as *partially-covered*

Critical Path Testing: Results

- **Experimental results for benchmark circuit c7552**



Critical Path Testing: Summary

- **Robust tests for path delay faults do not achieve high delay defect coverage**
  - May miss the longest paths!
- **Delay defect coverage of critical paths can be enhanced by testing uncovered segments**
- **Experimentally shown the presence of such segments in a benchmark circuit**

References:

M. Sharma and J. H. Patel, "Testing of Critical Paths for Delay Faults," Proc. Int. Test Conf. (ITC), pp. 634-641, Oct. 2001

M. Sharma and J. H. Patel, "Enhancing Delay Defect Coverage with Path-Segments," Proc. Int. Test Conf. (ITC), pp. 385-392, Oct. 2000