Artisan Components

Free IP Business Model

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1 Executive Summary

This paper evaluates the feasibility of the Free IP Business Model proposed by Artisan Component in the semiconductor chip library market. After rigorous analysis of the Free IP model using various qualitative and quantitative tools learned in EESOR 483 Strategy Models class, our findings are:

1. Overall, we believe Artisan s Free IP Model provides a superior alternative to the traditional one-time-fee licensing model currently in use. While there is some question as to exactly when the financial performance of this model exceeds the licensing approach, there are substantial benefits to be gained through shifts in the industry structure.
2. The timeframe for revenues in the Free IP model to exceed that from licensing is highly dependent upon the effective royalty rate (i.e., royalty as a percentage of the total wafer cost). This rate should be at least 1.5% to achieve acceptable times for the Free IP annual revenue to exceed that of the licensing model (roughly 4 years).
3. Our research showed that Artisan has the greatest chance for financial success in the next generation of process technology, i.e., in the 0.15-micron and succeeding generation of process technologies. The expected growth in cell-library generated designs in this next generation process technology and beyond should significantly accelerate the revenue stream under the Free IP model.
4. Artisan needs to continue to partner with all of the major foundries. Under the licensing model, creating a set of libraries for a second-tier customer was equal to creating libraries for a leading foundry. With Free IP, however, it is essential to work most closely with top-tier foundries as they represent the highest return to Artisan. This change does indicate a danger in a shift in power to the large foundries, who might seek more favorable contracts.
5. Artisan should craft and articulate a compelling marketing campaign directed towards its chip designing customers to increase corporate brand awareness and brand loyalty. This type of marketing approach is only feasible with the Free IP business model, as Artisan has limited exposure to the designer under a strictly licensing model.
6. Artisan can capture more of the chip area, and hence more revenue under the Free IP model, by working aggressively with Hard IP vendors. These companies are the developers of the system-level macros (SLMs) which will account for an ever greater part of new designs. By working with the SLM vendors, Artisan can get locked into an ever increasing proportion of the chip. It should be noted that SLM vendors are unlikely to work with more than one library vendor, so it is important for Artisan to begin these efforts now.

2 Free IP Business Model: Overview

2.1 History

Semiconductor foundries, named after the steel foundries of a generation ago, manufacture chips for designers and electronic systems companies on a contract, or for hire basis. As the cost of building a semiconductor factory, or fab has continued to increase, the manufacturing infrastructure to build state-of-the-art chips has concentrated into a smaller number of companies able to afford a billion dollars or more for today s factories. Foundries, able to reach a broad range of customers and a large, aggregated customer base, are among those who have continued to invest and are showing an ever-larger share of the semiconductor manufacturing market. Revenue for the dedicated foundry market reached $2.3B in 1997 (Dataquest, September 1998) and is expected to grow strongly in the future.

The design interface for the majority of foundry business has been, and continues to be, at the physical level. That is, the foundry s customer provides either masks or GDS-2 tapes (or equivalent), and the foundry builds chips per those instructions. Recently, however, there has been an increase in business at the logical level; these are chips designed with some type of logic cell library, I/O library and/or memory generator. While this accounted for only 4% of the foundry revenue in 1997, this number is increasing.

There are a number of vendors who, working with the foundries, develop and deliver these libraries. In the past, the business model has had the library vendors working essentially on a contract-engineering basis, where the libraries are paid for with a one-time licensing fee. Typical fees range from roughly $250k to $1M per library, depending on complexity. A given foundry may want as many as 10-15 libraries per technology node (such as 0.18-micron) and have 2 or 3 vendors per library. The total cost to a foundry is therefore typically $5-10M per process generation, with a new process introduced roughly every eighteen months.

2.2 Artisan Introduces the Free IP Model

In 1998 one of the leading suppliers of these libraries, Artisan Components (NASDAQ: ARTI), introduced a new and fundamentally different business model to the industry. In a radical move, Artisan moved away from the upfront-fee approach to a royalty driven system known as Free IP . As before, Artisan develops libraries oriented towards a specific foundry technology but now collects no immediate payment from the foundry. Artisan, rather than the foundry, distributes these libraries directly to the chip designers at no charge, hence the free in Free IP. Compensation comes from the foundries at a later time, as a royalty on the percentage of revenue attributable to the use of Artisan developed libraries (royalty calculations are based upon the relative percentage of the chip area that was created with Artisan libraries).

Another feature of Free IP is that technical support for the libraries is now handled directly by Artisan, rather than by the foundry. In the one departure from the free theme, these support costs are in general borne by the user and not the foundry.

2.3 Analysis of the Free IP Model

The key question raised by this new business model is is this the optimal approach for the long term? , especially for Artisan Components in particular. To address this question in a rigorous fashion, the QuasiOmniscients team evaluated this model from a number of different perspectives. First, there are substantial qualitative effects on the industry infrastructure surrounding the development and use of foundry libraries. These changes can alter the balance of power between the foundries and library developers, and provide some interesting strategic opportunities.

Second, the team looked at the economics of Free IP. Expected revenue streams were derived from both a single foundry/single technology as well as industry-wide orientation. Both the qualitative and quantitative methods and results are discussed in the subsequent sections of this report.

3 Qualitative Analysis

3.1 Foundry Relationship

By moving to the Free IP model, Artisan is creating a more complex relationship with their foundry partners. Under the previous model, the foundries were purely customers of Artisan, and the industry structure favored neither side disproportionately. There were (and are) a number of library vendors, some generalized such as Artisan and some more specialized such as Virage (a memory generator vendor), selling to an increasing number of foundries. In essence, the library developers were providing a contract engineering service.

Now, however, the introduction of the Free IP model has the potential to shift the balance of power. On the surface, the foundries and library providers now work more as partners (although the foundries still ultimately pay the bills) to deliver the end product to a common customer: chip designers. Both the foundries and the library providers share in the success or failure of the end product. However, the bargaining strength of the foundries has shifted considerably. Whereas before all foundries were equal customers to vendors such as Artisan, sharing some of the production rewards makes the larger foundries the most desired partners. This gives a TSMC, with more than $1B in production, much greater bargaining power with an Artisan than has a Winbond with under $100M in revenues. It is highly likely that a TSMC will take notice and advantage of this fact under a Free IP partnership to secure favorable royalty rates, royalty caps, etc. In fact, it has been speculated that at some point in the future, the large foundries could choose to renege on their agreements. We regard this as highly unlikely, but the possibility certain exists for a large foundry to insist on renegotiating current contracts if a vendor wants any future business. The converse holds for the smaller foundries, who may have to make concessions to work with leading library developers.

Another change in the library developer-foundry relationship engendered by the Free IP model concerns the number of libraries supported by the foundry. Essentially, the lack of up-front fees under this new model makes libraries a no-cost option for the foundries, who are likely to encourage all of the qualified vendors in the market to partner with them. As we show later, the total royalty paid in the Free IP model is independent of the number of library suppliers. This also shifts the relative power in favor of the foundries.

Lastly, the new model shifts some of the production risks, a comparatively small amount to the foundry but large to the library supplier. In return, the library developer should be able to expect a typically higher rate of return. This is analyzed in section 4 of this report.

3.2 Competitive Effects

While most of the changes in the industry effects with the foundries are deleterious to a company such as Artisan, there are some compensatory swings in the competitive landscape. The key issue concerns timing of the revenue stream. As opposed to a straight licensing approach, the Free IP model postpones the revenue until (and if) the chips begin production. In the semi-custom chip market, this can be a substantial delay. It is not uncommon for a design to take over a year to even begin the production ramp, even when everything works correctly the first time. The chips must be designed, built and then tested in prototype systems. Then, the end system must go through its own launch phase, gradually ramping up to full production volumes. A company such as Artisan, with an already existing revenue stream and

financing options including the issuance of new stock, can afford to wait out this period in anticipation of ultimately higher returns. A small startup, however, usually cannot wait — especially the small garage shops with little or no financial backing. Thus, a shift to the Free IP model raises the bar to new entrants, probably high enough to shut out most new competitors from the market.

Compounding this is the issue of library support. The Free IP model includes a shift in the support from the foundries to the library developers. This was not a major hurdle in the licensing scheme, as the number of customers (the foundries) was low and small entrants could provide adequate support. With the new model, however, the number of direct customers (the chip designers) is orders of magnitude larger and commensurately more difficult to support. This, and the potential for going out of business without immediate revenue, is likely to make foundries hesitant to work with new and/or small market entrants.

It must be noted that developing cell libraries, I/Os and memory generators is not rocket science although certainly some vendors do a better job than others do. The barriers to small startups mentioned above does not preclude highly resourced competition. The foundries themselves could, in fact, begin to develop their own libraries if the Free IP model proves too successful.

In terms of competition, the other major factor concerns existing competition from vendors such as Avant! who are holding fast to the existing licensing model. The belief by these companies is that the current model is superior, and as we show later they may be correct, at least in the short term. But it will be difficult to continue charging for a library when there are other vendors who are willing to get paid at a later time and then only if the customer is successful.

3.3 The New Customers: Chip Designers

At the very heart of the Free IP model is a shift in the customer base from the foundry to the chip designer. In a very real sense, of course, the foundry pays the bills and must be considered the customer but there are still some new and powerful opportunities afforded by this new model. Regardless of the model, the foundries have no particular interest in which vendors library is used to design a particular chip as long as the library delivers as promised and the chip is functional. From a purely marketing approach, it may be possible to sell chip designers on the particular merits of a given vendor s library. For example, Artisan states that there has never been a design failure as the consequence of flaws in an Artisan library. This could easily be used in a marketing campaign to gain market share, a necessity under the Free IP model as the total royalties is a fixed amount to be divided among the library developers.

The growing trend towards reusable semiconductor IP (and in this case we re referring to virtual components, such as embedded microprocessors or other high-level functions) opens up some very attractive business opportunities. In the future, a high percentage of the die area will be taken up by predesigned functions, often provided by third party vendors such as ARM, Ltd. Whoever provides the libraries to these companies will have found the most effective way to escalate the revenue stream from a given library.

Another semiconductor industry trend that can be leveraged through the Free IP model is the increasing proliferation of design houses. These firms provide chip design expertise to systems companies that do not have IC design competency in-house. By working closely with the largest and most successful design houses, a company such as Artisan could become a preferred vendor and capture a disproportionate share of the market.

4 Quantitative Analysis

4.1 Financial and Economic Analysis

One method to evaluate the desirability and impact of the free IP model is to take a look at industry forecasts for the markets in that Artisan does or could compete in. From these forecasts, we can undertake a quantitative comparison of royalty vs. licensing schemes. Our quantitative analysis will focus on single point analysis, aggregate industry analysis and break even point analysis of proposed models.

4.1.1 Single Point Analysis

Perhaps the first question that should be asked is whether or not the Free IP model is, from a purely economic perspective, an optimal solution for today s process technologies. There are trends within the foundry industry that may change the answer to that question over time, which will be discussed later.

4.1.1.1 Analysis Methodology

Unlike the fairly deterministic income from the traditional licensing model, the revenue stream under the Free IP model depends on a number of highly uncertain factors in the future. The team decided to use Monte Carlo techniques to incorporate these uncertainty rather than use point forecasts for unknowns such as foundry revenue. The base model was built into a standard Excel spreadsheet (see Appendix 8.1), which was then modified using macros developed by Prof. Sam Savage at Stanford University. These macros allow cells within the spreadsheet to be specified as any number of types of random variables.

4.1.1.2 The Free IP Model

This model analyzes the library revenue stream by taking a look at a single foundry s wafer production (measured in dollars) for a single process technology. In this case, the group used the 0.18-micron drawn gate length processes just beginning to enter the prototype and early production phases. We then applied a weighting factor to represent the proportion of this revenue addressed using libraries such as developed by Artisan. In 1997, Dataquest reported this proportion to be 4% of dedicated foundry revenue; it should be noted that in that timeframe a sizable percentage of foundry revenue came from older (0.6-micron geometries and larger) products, and we believe that the percentage of revenue coming from library-based designs is increasing.

Applying a royalty rate to this foundry revenue then gives the total available market (TAM) for library companies. This royalty stream, discounted to a net present value, can then be compared to the TAM under the current licensing scheme.

Mathematically, the calculation is as follows:

Royalty NPV = Summation_n (WR * CLD * RR) * $(1 /(1+r))^n$

where

WR = annual total wafer revenue for a given process at a single foundry

CLD = the percentage of the total wafer revenue attributable to cell-library based designs

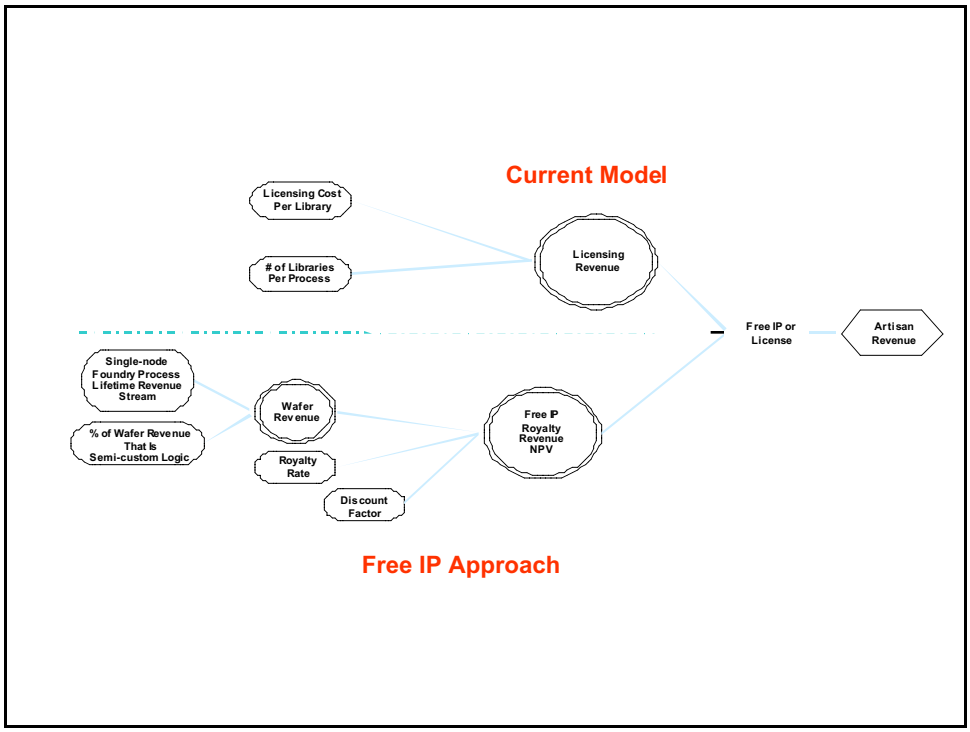
RR = the effective royalty rate paid as a percentage of total wafer cost

r = the cost of capital

n = the nth year of product for the process

Figure 1 graphically shows the decision between the licensing and Free IP models.

Figure 1
Single Technology Node Decision Analysis



4.1.1.3 Assumptions and Random Variable Assignments

To determine the wafer revenue, we assumed a 6-year lifecycle for a given process. While processes do in fact remain in production for longer than 6 years, the great majority of revenue falls within this lifetime. We set the single-year peak revenue as a normally distributed random variable with a mean of $1200B and a standard deviation of $200M. We then assumed a production lifecycle as follows:

Year	1	2	3	4	5	6
% of Peak Revenue	10%	50%	100%	100%	60%	20%

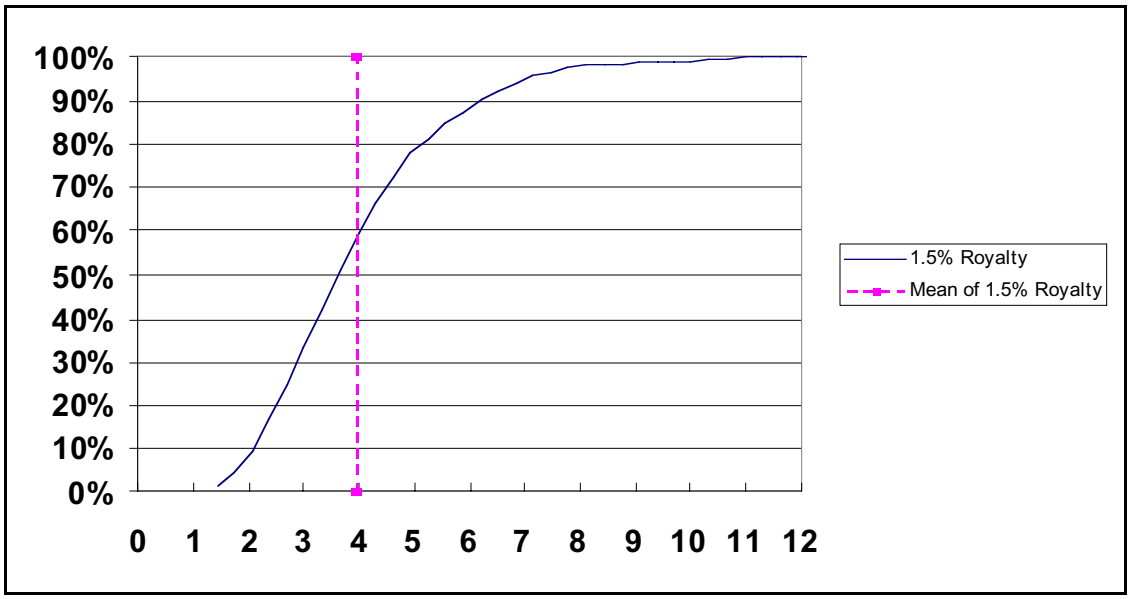
In the first year of production, the percentage of revenue attributable to cell-library based designs was set as a triangularly distributed random variable with a lower bound of 3%, a mean of 4%, and an upper bound of 8%. To reflect our belief that this proportion will increase over time, we set the second year s mean to equal the actual value of year 1, with a lower bound of 75% of the new mean and an upper bound of 200% of the mean. This also takes into consideration the fact that the proportion in one year will depend somewhat on the previous year s value (as the production lifetime for any given chip typically exceeds one year). For the fixed numbers, we used 10% for the cost of capital and tested royalty rates ranging from 1.1% to 1.9%. Sources within the foundry industry have stated that the effective royalty rate is typically 1.5%.

After running 2000 trials in the Monte Carlo analysis, we obtained the results found in Appendix B. For a 1.5% royalty rate, the results are shown below in Figure 2. The expected total royalty payments by the foundry have a net present value of just under $4M, with a standard deviation of $1.7M. This is in stark contrast to the current licensing scheme, which yields payments for libraries in the range of $5-10M (as these are upfront payments, there is no need to discount these figures). It must be remembered that these results reflect the *total* payments made by the foundry to its library suppliers, regardless of how many suppliers there may be. Each individual supplier is competing for a share of this amount.

Given these results, it seems highly likely that from a purely financial basis the current 0.18-micron generation was too early to go to the Free IP approach. Even if Artisan was the only library vendor in the market, it is still quite possible that their revenues would decrease. In fact, the simulation gives a probability of roughly 1/3 that the Free IP model will provide revenues of under $3M. From this analysis, it seems likely that the Free IP model will not have a financial edge over straight licensing until the 0.13-micron product generation (which should begin production in roughly 2002) or even beyond.

However, this model provides only a first-order look at the market, and several of the assumptions merit further review, particularly the percentage of revenue coming from cell-library based designs. As the market for these types of chips grows — particularly application-specific standard product (ASSP) designs from the new and growing breed of fabless semiconductor vendors such as C-Cube and Chameleon.

Figure 2
0.18-micron Technology Royalty Analysis



Further, while this analysis provides insight into the 0.18-micron product generation, it is likely that future silicon processes will show both a higher revenue curve and have a higher proportion of designs based upon libraries such as Artisan s. Both of these effects will increase royalty revenue, and make the Free IP model increasingly attractive.

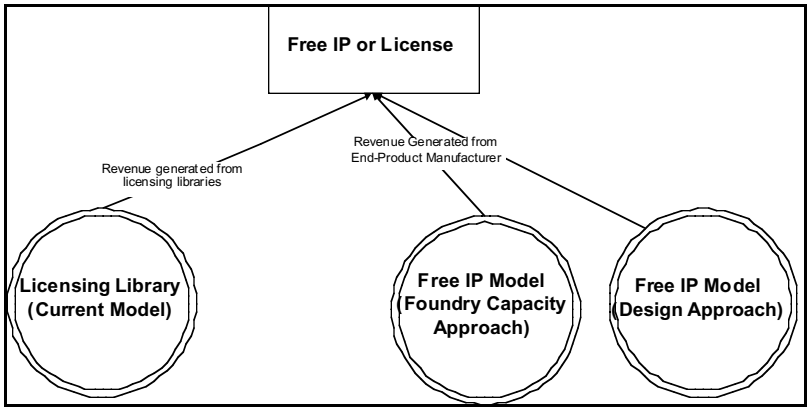
4.1.2 Total Industry Analysis: Free IP Model vs. Licensing

4.1.2.1 Decision Tree

We setup the decision between the two competing business models. To gain a higher level of accuracy on the Free IP revenue, we evaluated the market in two different ways.

- **Licensing Libraries Model (Current Model)**
- **Free IP Model (Foundry Capacity Approach)**
- **Free IP Model (Design Approach)**

Figure 3
Decision Analysis Models



Model 1: Licensing Libraries (Current Model)

In the licensing model, licensing revenue is determined by the rate of new silicon processes generated per year per foundry, the number of foundries in the market, the number of libraries used per process and the licensing cost per libraries.

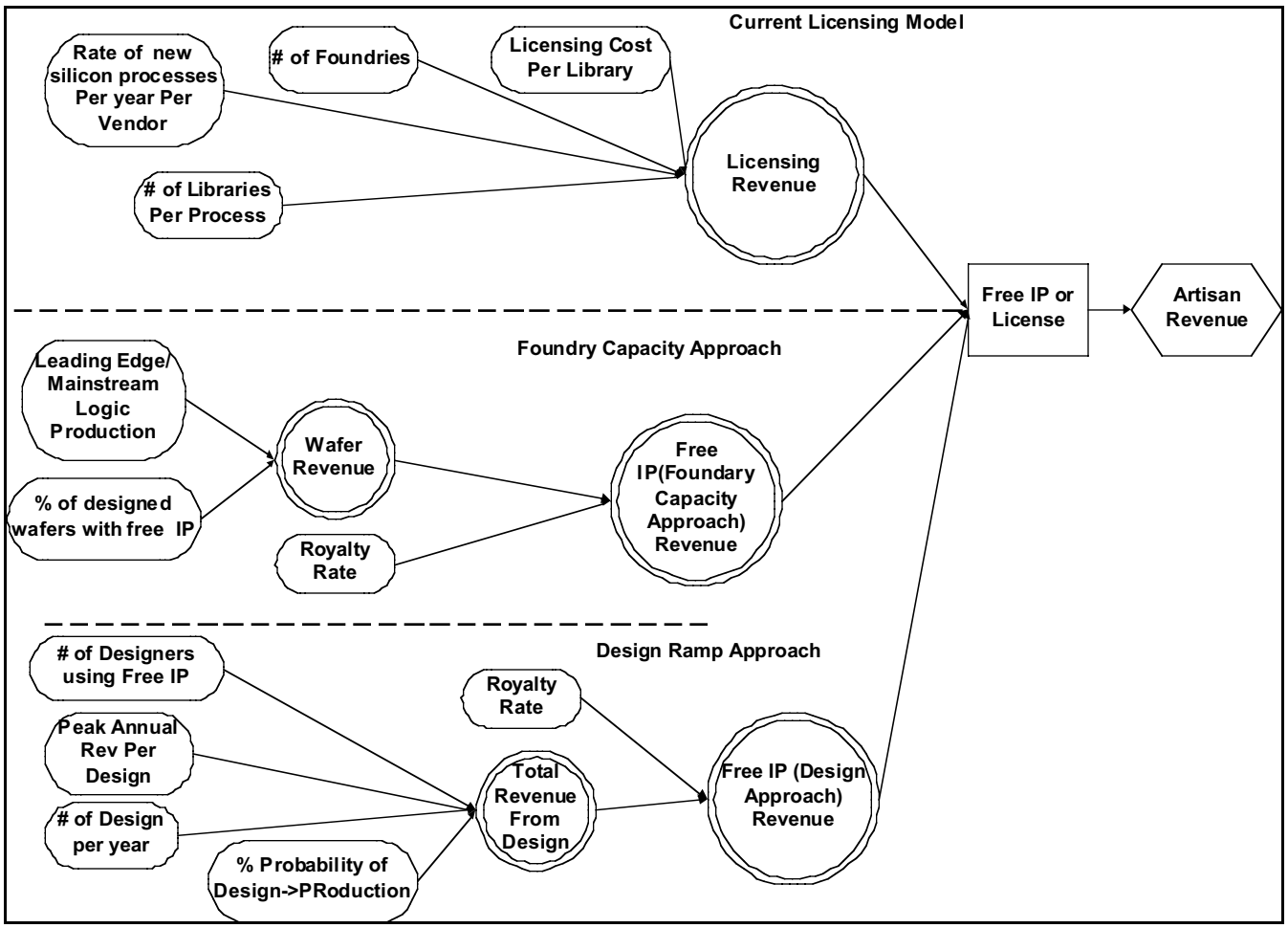
Model 2: Free IP Model (Foundry Capacity Approach)

In the Free IP business model, we can forecast wafer revenue by taking a percentage of end products designed using Free IP libraries, specifically the leading edge/Mainstream logic products in which Artisan products are used. We assume that Artisan charges manufacturers an effective royalty rate of between 1.1% to 1.9%.

Model 3: Free IP Model (Design Ramp Approach)

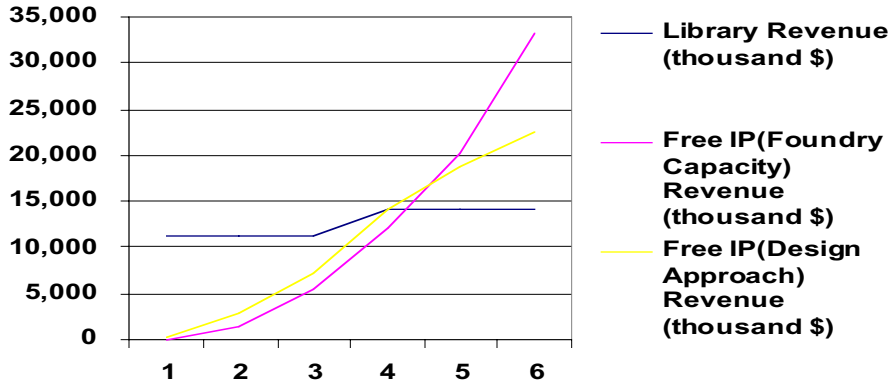
Alternatively, we can generate revenue forecast from a total number of designs designed with Free IP libraries that go into volume production. The total revenue from these designs is determined by number of designers using Free IP, the number designs per year, the success rate of the designs and revenue generation ramp and lifecycle of a design. Similar to model2, the total Free IP Revenue of Artisan is determined by the total revenue and royalty rate.

Figure 4
Industry Wide Revenue Decision Analysis



Next we evaluated Artisan s whole revenue in the market. We calculated Artisan s expected revenue for the next six years based on the decision diagram above (see Figures 3 and 4). The expected revenues are plotted as shown in Figure 5. The curve representing library licensing revenue is almost flat, expected to climb slightly to $15 Million annually after six years. On the other hand, at a nominal effective royalty rate of 1.5%, Free IP revenue starts at zero revenue at the first year and is expected to reach more than $20 Million annually after six years. In the Free IP Model based on the foundry capacity, the forecast is somewhat more optimistic at greater than $30 Million annually after six years. The removal of up-front cost to the foundries encourages greater and continued cooperation, and therefore broader dissemination of Artisan s libraries. Moreover, in five years the production of leading edge/mainstream logic by the foundries is expected to be three times as much as the current amount, and this substantial increase contributes to the high revenues in the future.

Figure 5
Licensing Model vs. Free IP Model (6 year forecast)



However, the crossover point does not occur for 4 years at which time Artisan receives more revenue per year in the Free IP model than in the library licensing model. This timeframe is fairly long because, as stated earlier, Artisan obtains the royalty revenue only after the chips designed using its libraries are sold as end products. Artisan has enough resources to hold out while the royalties start to come. While employing the Free IP Model impacts Artisan s financial position at the present time, in the long run it should prove superior.

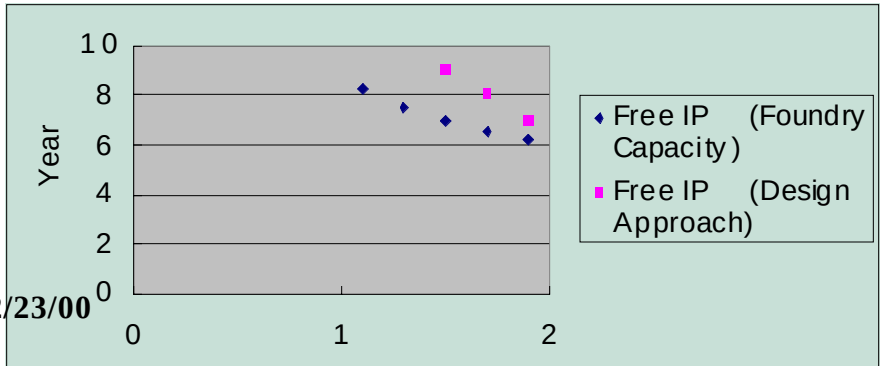
4.1.3 Break Even Point Analysis

We next compared the net present value (NPV) of Free IP model with that of the current model and identify the break even point when the NPV of Free IP model exceeds that of the current model. We assumed the cost of capital is 10% and determined the NPV of the revenue streams for several years. For example, in order to calculate the NPV of the first 5 years, we sum up the discounted revenue of the first 5 years.

Licensing Model: $$NPV_{5\,years} = \sum_{y=1}^{5} \{(Revenue\ in\ yth\ year) \times (0.9)^{y-1}\}$$

Free IP Model: $$NPV_{5\,years} = \sum_{y=1}^{5} \{(Revenue\ in\ yth\ year) \times (0.9)^{y}\}$$

Figure 6
Break Even Point Analysis

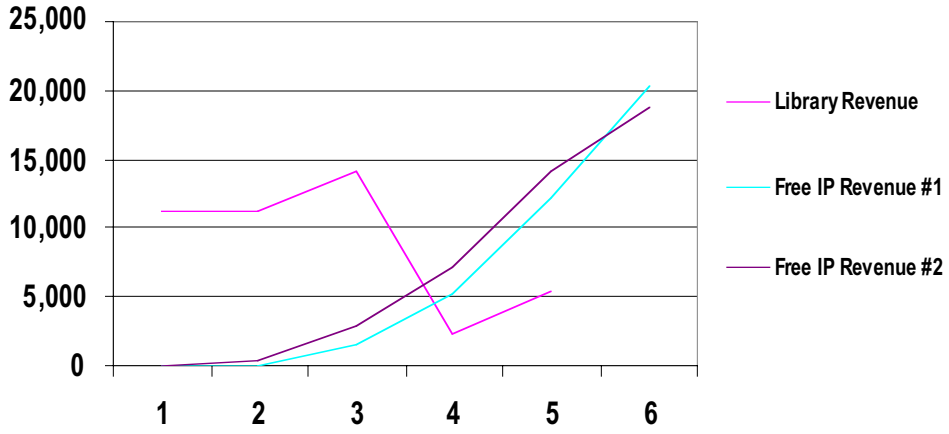


The relation between the royalty rate and the break-even point is plotted in Figure 6. At an effective royalty rate of 1.5%, the annual revenue in Free IP Model will exceed that of the current model in four years, but Artisan will need at least an additional three years for the Free IP NPV to finally exceed than that of the current model. If Artisan sets the royalty less than 1.5%, Artisan is unlikely to attain a higher net present value using Free IP Model than the licensing model in less than 10 years. Therefore, the royalty should be more than 1.5%.

4.2 Economic Scenario Evaluation

Historically, the semiconductor industry advances a technology generation every 18 months, part of what drives what is popularly referred to as Moore s Law . While the industry has stayed on this cycle for many years, there is always the concern that some event or physical barrier, either seen or unforeseen, will slow down the introduction of some advanced process generation. The current concern revolves around the lithography equipment for printing circuits on chips. The current approach, optical lithography, may not work beyond the 0.13-micron process generation (although it should be noted that it was also believed that optical lithography would not work at 0.13-micron, but advances in optical phase correction and other techniques have extended the optical approach). While there are several promising approaches to optical lithography s successor, development of these technologies (such as x-ray lithography, e-beam, etc.) is extremely expensive. The semiconductor manufacturing equipment vendors are likely to wait until consensus has been reached on one particular approach before building production equipment. Therefore, we have to consider the possibility of a substantial discontinuity in new process introduction. Library development would be impacted under this situation — without new processes, there is no need at all for new libraries. If we assume the rate of new silicon processes will drop down from 0.75/year/vendor to 0.10/year/vendor after 3 years because of new lithography approaches, the expected revenues are drawn as in Figure 7. Revenues under the free IP model are much less affected, however, as royalties of older technologies (whose production lifetimes will be extended to fill the gap caused by the lack of new process technologies) will keep providing revenue for Artisan, even though no new technologies come out. This will reduce Artisan s financial risk.

Figure 7
Technology Discontinuity Analysis



5 Conclusions

The Free IP business model is a qualitatively superior alternative for Artisan and its partners - the foundries and system designers. Despite some sacrifices in the relative strength compared to leading foundries, there are a number of favor industry shifts engendered by the Free IP model. However, the Free IP model becomes economically superior for Artisan only under certain market and royalty conditions as outlined in our analysis. In the near term, it is unlikely for the Free IP model to become a financial improvement over the current model in the 0.18-micron process generation. The new model has a higher probability of success in the next generation technology, i.e., at the 0.15-micron process generation or beyond. From our analysis we conclude that Artisan needs to have an effective royalty rate greater than 1.5%, at least at first. In the near future, i.e., in three years or less, we see Artisan s model taking root in the industry with its superior benefits to all players involved. In this time frame, Artisan probably has the high probability of success for its Free IP model under the assumption that the 0.13-micron technology will generate substantial foundry revenues for parts designed using cell libraries.

The conclusions drawn above are supported by the basic industry dynamics, which are a combination of Moore s Law for process technology lifecycles. Even with modest effort, Artisan has a good chance to win mind-share and IP share in the library market for logic cells and memory modules not only at the foundries, but as increasingly important, at the chip designers desktop as well. We recommend that Artisan should continue an aggressive partnering strategy with at least the top three foundries in the industry, who control more than 50% of the market combined for dedicated foundry silicon wafer processing. Artisan can lock these large foundry fabs into its Free IP model and make it economically infeasible for Artisan s licensing-only competitors.

6 Strategic Recommendations

Artisan should embark on an aggressive marketing campaign to increase brand awareness of their libraries. We recommend a campaign of co-branding Artisan s customers products (or at least the loyalties) with something like an Artisan Inside . This approach is not feasible without the Free IP model and as the industry leader Artisan is in an ideal position to capitalize on this opportunity. Another essential tactic is stave off potential start up competition through a cleverly articulated message of FUD (Fear, Uncertainty and Doubt) in both foundries and chip designers.

In the long term, Artisan needs to make a concerted effort to work with Hard-IP developers (the companies providing the high-level system functions such as micropocessors) to capture more chip real estate. Since the royalty payments for the use of Artisan s logic cells and memory modules embedded in the wafer determines the revenue stream, it is in Artisan s interest to maximize this revenue stream by increasing its share of the silicon wafer area. By working with the system function providers, Artisan can dramatically increase their potential revenue stream.

Another strategic project for Artisan to undertake is to establish a long-term strategic alliance with leading independent design houses such as Cadence and Synopsys. The goal of this relationship should have only one purpose — to drive the industry-wide adoption of Artisan s components the de facto standard. With the size and reach of these EDA (Electronic Design Automation) firms, they can significantly influence the market for Artisan, since they determine the library and embedded components which will be used in their custom logic designs for advanced semiconductors

7 Recommendations For Further Study

The issues surrounding the Free IP model are extremely complex, and the scope of this project is insufficient to evaluate all of these areas fully. In particular, the analytical models used in this report should be extended and the assumptions behind the models very, very carefully tested. The sensitivity of the outcomes to an input variable such as the foundry industry forecast is quite high, and can swing the results significantly.

The opportunities for partnership with leading hard IP providers should be quantitatively evaluated, as this area holds a great deal of promise.

Statistical evaluation is a very powerful tool, and could be used to great effect on the industry-wide analysis. It is important to establish the random variables carefully, both in terms of variable type and distribution.

Further inputs from Artisan s direct competition and objective industry analysts would be of value to explore any other possible weaknesses in the Free IP model.

8 Appendix

8.1 Forecast Data for Single Point Analysis

Discount Rate	10%							
Discount Factor	0.909091	0.82644628	0.7513148	0.68301346	0.62092132	0.56447393		
	1	2	3	4	5	6		
	1999	2000	2001	2002	2003	2004		
Wafer Revenue	100	500	1000	1200	700	200		
Logic Percentage								NPV
4%	4	20	40	48	28	8		105
8%	8	40	80	96	56	16		210
12%	12	60	120	144	84	24		315
16%	16	80	160	192	112	32		420
20%	20	100	200	240	140	40		525
		Royalty Rate						
		1.1%	1.3%	1.5%	1.7%	1.9%		
	4%	1.2	1.4	1.6	1.8	2.0		
	8%	2.3	2.7	**3.1**	**3.6**	**4.0**		
	12%	**3.5**	**4.1**	**4.7**	**5.4**	**6.0**		
	16%	**4.6**	**5.5**	**6.3**	**7.1**	**8.0**		
	20%	**5.8**	**6.8**	**7.9**	**8.9**	**10.0**		
Cost/Library	0.25							
Libraries/Node	12							
Library Revenue	**3**							

8.2 Forecast Data for Industry Analysis

Year	1999	2000	2001	2002	2003	2004
< Licensing Model>						
New Silicon Processes Per Year Per Vendor	0.75	0.75	0.75	0.75	0.75	0.75
Number of Foundries	4	4	4	5	5	5
Number of Libraries Per Process	15	15	15	15	15	15
Licensing Cost/Lib.	250,000	250,000	250,000	250,000	250,000	250,000
Library Revenue (Thousand $)	11,250	11,250	11,250	14,063	14,063	14,063
<Free IP Model - Foundry Capacity>						
Leading Edge/ Mainstream Logic Production (Million $)	3,676	4,897	6,976	8,010	9,612	10,988
Ratio of Wafers Designed Using Free IP	0%	2%	5%	10%	14%	20%
Wafer Revenue (Million $)	0	98	349	801	1,346	2,204
Royalty(%)	1.5%	1.5%	1.5%	1.5%	1.5%	1.5%

Free IP Revenue (Thousand $)	0	1,469	5,232	12,015	20,185	33,064
<Free IP Model - Design Approach>						
Number of Designers Using Free IP	400	600	800	1000	1100	1200
Number of Designs per Year	100	150	200	250	275	300
Success Rate of Designs	50%	50%	50%	50%	50%	50%
Peak Annual Revenue Per Design (Million $)	4	4	4	5	5	5
Total Revenue From Designs (Million $)	20.00	190.00	480.00	937.50	1243.75	1487.50
Royalty	1.5%	1.5%	1.5%	1.5%	1.5%	1.5%
Free IP Revenue (Thousand $)	300	2,850	7,200	14,063	18,656	22,313

8.3 Economic Analysis Models

Model 1: Licensing Libraries (Current model)

$$r_{Art} = N_p \leftrightarrow N_l \leftrightarrow N_f \leftrightarrow C$$

where

$r_{Art} = Revenue\ of\ Artisan$

$N_p = Number\ of\ new\ silicon\ processes\ per\ year\ per\ vendor$

$N_l = Number\ of\ libraries\ per\ process = 15$

$N_f = Number\ of\ foundries$

$C = Licensing\ cost/library = \$250,000$

Model 2: Free IP Model (Foundry Capacity Approach)

$$r_{Art} = r_T \leftrightarrow R$$
$$r_T = y \leftrightarrow P_f$$

where

$r_{Art} = Revenue\ of\ Artisan$

$r_T = Total\ revenue\ from\ wafers\ manufactured\ using\ Artisan's\ libraries$

$R = Royalty$

$y = Leading\ edge/mainstream\ logic\ production$

$P_f = Ratio\ of\ wafers\ designed\ using\ free\ IP$

Model 3: Free IP Model (Design Approach)

$$r_{Art} = r_T \leftrightarrow R$$
$$r_T = (\dot{N}_D \leftrightarrow n_D) ? \dot{P}_P \leftrightarrow P_S \leftrightarrow r_D$$

where

$r_{Art} = Revenue\ of\ Artisan$

$r_T = Total\ revenue\ from\ Artisan's\ designs$

$R = Royalty$

$\dot{N}_D = Number\ of\ designers$

$\dot{P}_P = Ratio\ of\ peak\ revenue$

- 10% *in the 1st year after designed*
- 80% *in the 2nd year after designed*
- 100% *in the 3rd year after designed*
- 40% *in the 4th year after designed*
- 10% *in the 5th year after designed*

$n_D = Number\ of\ designs\ per\ designer\ per\ year = 0.25$

$P_S = Success\ rate\ of\ designs = 50\%$

$r_D = Peak\ annual\ revenue\ per\ design$

8.4 References

1. http://www.artisan.com
2. Dataquest Reports .
3. EESOR 483 Strategy and Planning Models Course Reader
4. Interview with Jeff Lewis, VP of Marketing at Artisan Components

8.5 Presentation Slides

(Please see attached presentation).