BioE332 Lecture 5: Neurogrid Tutorial I

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ops per second/\$ doubles every 1.0 years

doubles every 7.5 years doubles every 2.3 years

1880 1900 1920 1940 1960 1980 2000

Jim Gray 2001

Thursday, April 21, 2011
The graph illustrates the trend of operations per second ($ops\ per\ second/$) increasing over time. It shows that the computing power doubles every 1.0 years, every 7.5 years, and every 2.3 years from 1880 to 1980. The graph includes historical computing devices, such as the Brunsviga Model 20 and the 100Mz Compaq, to visualize the evolution of computing technology.
64 Processors

2,048 Processors
2,048 Processors

131,072 Processors
5 watts
1M neurons
6B synapses
10 spikes/s each
Neurogrid = 22 BG Racks

<table>
<thead>
<tr>
<th></th>
<th>Chip</th>
<th>Board</th>
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</thead>
<tbody>
<tr>
<td>Neurons</td>
<td>65K</td>
<td>1.0M</td>
</tr>
<tr>
<td>Syn/s</td>
<td>3.9G</td>
<td>63G</td>
</tr>
<tr>
<td>Watts</td>
<td>150m</td>
<td>5.0</td>
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<tbody>
<tr>
<td>Syn/s</td>
<td>1</td>
<td>63G</td>
</tr>
<tr>
<td>Flops</td>
<td>1K</td>
<td>63T</td>
</tr>
<tr>
<td>Bytes/s</td>
<td>66</td>
<td>4.2T</td>
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<tr>
<td>Watts</td>
<td>10μ</td>
<td>0.63M</td>
</tr>
</tbody>
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* 5W vs 630,000W
256x256 Neuron Array

- 65,536 neurons
- 23M transistors
- 160 mm²
- 0.18 um CMOS
256x256 Neuron Array

65,536 neurons
23M transistors
160 mm$^2$
0.18 um CMOS
50-150 mW
Modeling cortical cell types

- Fast spiking
- Regular spiking
- Intrinsic bursting
- Chattering
Cortex

Chips
Cortex

Chips

On-chip RAM

Off-chip RAM

Leaky cables

Cell parameters

Vertical

Horizontal

Arbor

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256x256 Neuron Array
For this class

* Single-compartment, fast or regular-spiking neuron with quadratic or cubic positive feedback
* Conductance-based synapses with arbitrary $E_{rev}$
* Local arbors with programmable space-constant
* No dendrite; no channels; no NMDA (not calibrated)
* USB Bandwidth: 2.5 to 10 Mspk/sec*
* Daughterboard Fanout x Spike-Rate: 5 Mspk/sec*
* Weights using probabilistic synapses*

*Still debugging and optimizing*