The Hardware

DACs and RAM specify properties & connectivity of STDP chip's 1280 silicon neurons.

Computation is analog; communication is digital. Spikes share a common set of input/output lines. Addresses specify identity of source/target.
A neuron's address is output when it spikes; the corresponding synapse is activated.

Assigning unique addresses to $N$ sources/targets requires $\log_2[N]$ bits.

These bits are transmitted over $\log_2[N]$ shared wires—have to run $N$ times faster.

Source–target pairs are specified by a look-up table (stored in RAM).

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**Address-event link**

<table>
<thead>
<tr>
<th>Address Encoder</th>
<th>Digital Bus</th>
<th>Address Decoder</th>
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<tbody>
<tr>
<td></td>
<td>1</td>
<td>1</td>
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<tr>
<td></td>
<td>2</td>
<td>2</td>
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<tr>
<td></td>
<td>3</td>
<td>Time</td>
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</tbody>
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Encoder outputs source’s address; decoder recreates spike at target location.

The encoder’s \( N \) inputs are tied to the neurons’ spike-outputs; it places \( \log_2[N] \)-bit addresses on the bus.

The decoder’s \( \log_2[N] \) inputs come from the bus; its \( N \) spike-outputs trigger postsynaptic potentials.

Dealing with coincidences

An arbiter ensures that encoder’s inputs are activated one at a time.

If two neurons fire at the same time, the arbiter selects one of them. That neuron’s spike is transmitted first, and then the second neuron’s spike is transmitted. Since it takes only 40ns to transmit a spike, the delay is negligible.
STDP chip

There are row and column decoders, arbiters and encoders. Addresses specify row and column of source/target—encoded by row and column encoders and decoded by row and column decoders.

Targets can be individual STDP synapses as well as neurons, which can be excited or inhibited directly.

STDP chip's microcircuit
The chip’s core is tiled with a regular array of identical microcircuits.

A microcircuit includes 4 pyramidal neurons and 1 interneuron; there are 21 plastic synapses (STDP) for each pyramidal neuron.

With a 16×16 array of microcircuits, the chip has a total of 1024 pyramidal cells, 256 interneurons, and 21,504 plastic synapses, all of which are individually addressable.

Microcircuit schematic

Pyramidal cells and interneurons interreact through fast and slow synapses and diffusors, which model their dendritic arbor’s cable-like decay.

Many inputs are shared:

— Input_slow drives the slow inhibitory synapse as well as the slow excitatory synapse.
— Input_fast provides fast excitation to the pyramidal neurons as well as the interneuron.

However, the strengths of these inputs can be controlled independently.
A look-up table is stored in the RAM.

When a pyramidal neuron spikes it can trigger up to 32 (arbitrary) synapses on the chip.