Chapter 4

Fabrication of Micro-Magnetic Traps for Cold Neutral Atoms

This is an updated and expanded version of Reference [8].

Many proposals for quantum information processing or quantum feedback experiments require precise control over the motion of neutral atoms, as in the manipulation of coherent matter waves or the confinement and localization of individual atoms. Patterns of micron-sized wires, fabricated lithographically on a flat substrate, can conveniently produce large magnetic-field gradients and curvatures to trap cold atoms and to facilitate the production of Bose-Einstein condensates. The intent of this chapter is to provide the researcher who has access to a standard clean-room enough information to design and fabricate such devices.

The clean rooms of Professors Michael Roukes and Axel Scherer were used extensively in this research. Eyal Buks, Darrell Harrington, and Marko Loncar were generous with their time in teaching the author the basics of photolithography and ion milling.

4.1 Fabrication Challenges and Constraints

Fabrication of atom chips poses several challenges in addition to those encountered in standard photolithography [90]. Many applications require the wires to be a couple microns wide by a few microns tall and spaced only a few microns from one another. One micron resolution is near the limit of standard photolithography, and much care
must be taken to accurately produce these micron-sized wires. Wires with widths much less than a micron—though perhaps important for realizing potentials with sub-micron scale features—are of limited usefulness for creating large magnetic field gradients and curvatures since they become limited to the same maximum current density as micron-sized wires [68]. Further fabrication complications arise from the need to trap the atoms near the substrate’s surface, and the need to connect the microwires to macroscopic leads without blocking optical access. A common technique for trapping atoms near the substrate surface, the mirror magneto-optical trap (mMOT), requires that this surface be an optical mirror as well as the support surface for the microwires (see Figure 2.8) [2]. The substrate surface needs to be larger than 5 to 10 cm\(^2\) to accommodate the reflected trapping beams as well as to allow the pads for macroscopic wire contacts to be outside of the mirror area and not blocking the optical access needed for the trapping, imaging, and pumping beams. Consequently, the wire pattern must be flawless over an exceptionally large surface area: during fabrication one must be extremely careful that no dust or surface defects break or short the wires.

The major fabrication challenge lies in increasing the height of the wires to a few microns. Even the smallest wires need to support up to an amp of current, and consequently, the cross-sectional area of the wire must be maximized. This reduces wire resistance and limits the heating that causes wire breakdown. Moreover, attention must be paid to the thermal conductivity of the substrate and mounting system to ensure sufficient power dissipation. Sapphire or polished aluminum nitride (AlN) substrates provide sufficient thermal conductivity, but are slightly trickier to use for fabrication than more standard substrates. The group of Joerg Schmiedmayer in Heidelberg has recently found that Si coated with an insulating oxide layer is the optimal substrate in terms of thermal conductivity [91].

The use of microwires to create an Ioffe trap illustrates these challenges. The wire pattern shown in figures 4.1(a) and (b) creates a 3D harmonic trap when combined with a perpendicular homogenous bias field [3]. Unlike a quadrupole trap, the Ioffe trap has a non-zero field at the trap center and thus does not suffer from Majorana
spin-flip losses. An atom is confined within the Lamb-Dicke regime when its recoil energy is less than the trap’s vibrational level spacing \( \eta = \left( \frac{E_{\text{recoil}}}{E_{\text{vib}}} \right)^{1/2} < 1 \), and for a cesium atom this occurs when the trap curvature exceeds \( 2 \times 10^6 \) G/cm\(^2\). To achieve this extremely large field curvature in all three dimensions, the radius of the wire pattern in figure 4.1(a) must be smaller than \( \sim 30 \) µm. For a trap of inner radius 10 µm, outer radius 15 µm, and wire current \( I = 1 \) A, the curvature and Lamb-Dicke parameter, \( \eta \), at the center of the trap in the axis perpendicular (plane parallel) to the substrate is \( 2 \times 10^8 \) G/cm\(^2\) \( (2 \times 10^{10} \) G/cm\(^2\)) and \( \eta = 0.38 \) \( (\eta = 0.11) \). The closely spaced wires can only be a few microns wide, and even if fabricated to a height of 2 to 4 microns, the wires would need to support the large current density of \( \sim 10^{11} \) A/m\(^2\).

The accommodation of laser beams for atom cooling, loading, and imaging constrains and complicates the atom chip’s design. The trap minimum is only 7 µm from the substrate’s surface, and the mirror patterned on the surface for use with the mMOT must neither short the Ioffe wires nor extend more than \( \sim 5 \) µm from the surface. The following sections describe the necessary fabrication tools and the techniques we use to overcome these challenges.

### 4.2 The Elements of Atom Chip Fabrication

Microfabrication is a labor intensive process, often involving several weeks of trial and error to perfect the fabrication recipe. However, once the process works, five to ten atom chips can be produced over a span of two to three days. The intent of this paper is to provide the researcher who has access to a standard clean-room enough information to design and fabricate an atom chip. We will describe the use of fabrication instruments and techniques only insofar as they are relevant to atom chips. Fabrication is not an exact science, and the techniques described here may not be optimal, but nevertheless have proven successful for the chips we have fabricated.

In photolithography, UV light shone through a photomask casts shadows onto photoresist, a light sensitive polymer, which is coated on the surface of the substrate. Either positive or negative photoresist may be used, with the primary difference be-
Figure 4.1: The planar Libbrecht-style Ioffe trap. a) When combined with an opposing bias field, this wire pattern produces a 3D harmonic potential above the substrate with a non-zero field at the trap center [3]. b) A planar Ioffe trap with an on-chip bias coil fabricated with gold on sapphire using the lift-off method. In the sample shown here, the wire height is $1.5 \mu m$ and the minimum wire width is $10 \mu m$. The gold between the wires forms a mirror for creating a mirror MOT.
increase the wire’s thickness pertain to individual fabrication techniques and will be discussed in the next section.

4.2.1 The photomask

The photomask is typically a 10 cm square piece of glass or transparent plastic on which is printed a positive or negative 1:1 image of the wire pattern. Wire patterns with widths or spacings less than $\sim 30 \, \mu m$ require a professionally made chrome mask: one in which the pattern is written with chromium on a glass plate. We have used the company Photronics, Inc. (telephone 619-992-8467) to make photomasks from AutoCAD drawings. Much care must be taken in producing the AutoCAD files since not all functions are properly converted to the company’s file format. In particular, all shapes should be drawn as closed, unfilled polylines. These masks are quite expensive, costing between $600 and $800, but have sub-micron resolution and are typically shipped within a week. It is possible to purchase a laser writer to produce in-house photomasks with resolution down to 0.8 $\mu m$. This can be a cost-effective alternative to purchasing individual masks from companies.

Many commercial printing shops are capable of printing overhead transparencies with high enough resolution to serve as photomasks for wire patterns with features larger than $\sim 30 \, \mu m$. The line edges are granular on a scale of a few microns, and the UV exposure time must be adjusted to account for the ink not being perfectly opaque. However, the one day turn-around, low cost of $\sim$20, and ease of file preparation—only an .eps file is typically needed—make the transparency photomask quite an attractive alternative for large features.

4.2.2 The substrate

As mentioned earlier, the substrate material for the atom chip should be carefully chosen: it must be electrically insulating, highly polished, not susceptible to fractures upon localized heating, and an excellent thermal conductor. We found that both sapphire and AlN substrates satisfy these requirements. Sapphire substrates 0.5 mm
to 2 mm thick with surface areas of several cm$^2$ may be purchased from companies such as Meller Optics, Inc. (telephone 800-821-0180) for $30 to $50 apiece. A surface quality of 80-50 scratch-dig is sufficient for fabrication. The thermal conductivity of AlN, $170 - 180 \text{ Wm}^{-1}\text{K}^{-1}$ at 20$^\circ$ C, is $\sim 4.5$ times higher than that of sapphire [68]. We measured that the max current density supported by microwires on AlN, $\sim 2 \times 10^{11} \text{ A/m}^2$, is a factor of two greater than for microwires patterned on sapphire. This was measured using electroplated gold wires of varying cross-sections patterned exactly the same way on both AlN and sapphire substrates. Specifically, we used several 3 $\mu$m and 20 $\mu$m wide wires whose heights ranged from one to three microns. The substrates were glued to room temperature copper blocks using Epotek H77 (Epoxy Technology, telephone 978-667-3805), a thermally conductive epoxy. Reference [91] finds that substrates of oxide on silicon have superior thermal properties to sapphire and AlN, and this silicon substrate is in some cases more amenable to standard microfabrication techniques.

Compared to AlN, sapphire substrates are easier to use for fabrication because their transparency allows one to detect and avoid defects and dust during the photolithography process. Moreover, with a transparent substrate, it is easy to align features on the substrate to devices on the surface underneath. Polished AlN substrates may be purchased in bulk for less than $\sim 75$, and unlike sapphire, AlN substrates can be cleaved with a diamond scorer to any shape desired. We were able to dice a $\geq 1$ mm thick sapphire substrate using a diamond saw, but on occasion the substrate cracks in undesirable ways. The polished AlN still has a considerable amount of surface roughness—one micron wide plateaus a few hundred nanometers tall are typical—but we found that it is nevertheless possible to fabricate on this surface perfect three micron wide wires spaced less than three microns from one another. The surface bumps simply map directly onto the upper surface of the wires.
4.2.3 Substrate cleaning

Before the photolithography process may begin, the surface of the substrate must be cleaned to remove all organic material and dust. Although some of the following steps may seem unnecessary and “overkill,” investing the time to thoroughly clean minimizes the chance that after many hours of work, one discovers that a piece of dirt has broken or shorted a wire. The first step is to immerse the substrate in a beaker of “piranha etch,” sulfuric acid and hydrogen peroxide in a 10:1 volume ratio brought to 100° C on a hot plate for ∼5 min. Teflon coated, flat-tipped tweezers are ideal for manipulating substrates. After the etch, the substrate should be placed in a beaker of acetone, heated again to 100° C for a few minutes, and finally inserted into an ultrasound cleaner for few more minutes. In extreme cases of substrate grime, a cotton tipped dowel can be used to manually wipe away the dirt. Acetone leaves a thin film—and sometimes even particulate—when allowed to dry on a substrate’s surface. It is imperative that one spray isopropanol (IPA) onto the substrate as it is removed from the acetone bath. This rinses the surface of acetone and wets it with IPA which does not dry quickly. The substrate must then be rinsed with methanol, which is relatively clean and does not leave a film, and immediately blown dry with an air or nitrogen gun. It is crucial that the air jet is aimed almost parallel to the surface so that the methanol is blown-off rather than dried on the substrate. When done correctly, the only remaining dirt particles will be along the edge of the substrate that is downwind of the air jet, and not in the center fabrication region. If the substrate is reasonably clean after the piranha etch, than the acetone step (which may actually add some dirt particulate) may be skipped, and the substrate should instead be immersed in IPA and placed inside an ultrasound cleaner.

4.2.4 Thermal evaporation

Certain fabrication techniques, to be discussed below, require that a 100 nm metal layer be thermally evaporated before coating the surface with photoresist. We take this opportunity to discuss the thermal evaporation process. We use gold for the
wires because of its high electrical conductivity, resistance to corrosion, and ease of evaporation, electroplating, and wet etching. To successfully deposit gold on a substrate’s surface, one must first evaporate a 50 Å metallic layer that promotes adhesion between the gold and the sapphire or AlN. We typically use chromium, but titanium may also be used. At the level of our current experiments, the magnetic effects from the thin layer of chromium are negligible. In a thermal evaporator, the substrate is mounted in a vacuum chamber facing a tungsten crucible positioned a few tens of centimeters below. The crucible, known as a boat, can hold 10 to 20 pieces of ∼2 mm long and 0.5 mm diameter gold wire. Current flows through the boat, melting the gold and spewing it upwards toward the substrate. A calibrated crystal monitor measures the deposition rate. One to two boats are sufficient to deposit 100 to 200 nm of gold, and this costs $10 to $15 per boat. There are typically only four sets of electrical feedthroughs in the evaporator’s vacuum chamber, and to deposit more gold, one needs to bring the chamber up to atmosphere, reload the boats with gold, and pump back down to base pressure (∼1 × 10⁻⁶ Torr)—a process that takes about an hour. The substrate mounting area allows several substrates to be coated at once. Evaporating less than 1 µm of gold is reasonable, but depositing more than 1 µm becomes too expensive and time consuming, and the quality of the gold surface begins to diminish. Moreover, the vacuum chamber eventually becomes hot which may result in the failure of the crystal monitor or the burning of photoresist. Sputtering the gold is an option that we have not explored, but may be more efficient.

Some groups have reported an intermittent difficulty with getting the adhesion layer to “stick” regardless of whether Cr or Ti is used, and have not found a consistent culprit. This results in the pealing away of the gold layer after evaporation. We have only had one episode of this occurring (in what is known as the “left” evaporator in Roukes’ lab), and we believe it was caused by the combination of a leaky and dirty vacuum chamber. The Cr or Ti became corroded either as it evaporated onto the substrate or once it was attached. The vacuum pressure would rise abnormally upon the melting of the Cr or Ti boats. The problem was solved by simply switching to the “right” evaporator, but this is hardly a long-term fix and an inspection and thorough
cleaning of the “left” evaporator should be done.

4.2.5 Photoresist spinning and baking

Photoresist does not always adhere well to the substrate’s surface. Before coating with photoresist, the substrate should be baked on a hot plate at $\sim 150^\circ$ C for a few minutes to remove surface moisture. However, caution must be taken with custom-cut sapphire substrates. A few of these have cracked after being placed directly on a 120$^\circ$ C hot plate. Slow ramping of the hot plate temperature may be required.

Hexamethyldisilazane (HMDS) should be used with sapphire and quartz substrates to promote adhesion (this is unnecessary for AlN). Only a few monolayers of HMDS are required: after baking, place the sapphire in a dish next to several drops of HMDS and cover for a few minutes. Note that both HMDS and photoresist are carcinogenic and should be handled with care.

Spinning photoresist onto a substrate is a relatively straightforward process. The substrate, with beads of photoresist dripped onto its surface, is spun by a vacuum chuck to a few thousand rpm for several tens of seconds. A faster rotation results in a thinner film of photoresist. Typically, a film thickness of a few microns is possible with standard photoresists, and there exists special resists that are four to twenty microns thick. These thicker resists are often important for making tall wire structures. The thickness of a photoresist may be increased beyond its specification by dripping resist onto its surface during rotation. After spin-coating, the photoresist needs to be baked on a hot plate to prepare the polymer for UV exposure. The exact temperature and bake duration are often crucial to the success of the fabrication. We would like to note that it is possible to layer microwire patterns on top of one another by fabricating each new wire layer on top of a spin-coated insulator such as polyimide [92]. This will be discussed further in Section 4.2.10.
4.2.6 UV exposure

The central step in photolithography is the UV exposure of the photoresist. An instrument known as a mask aligner allows one to accurately position the photomask flush to the substrate’s photoresist-coated surface, and a built-in UV lamp exposes the photoresist for a specified amount of time. Essential for photomask and substrate registration is an optical microscope mounted on the mask aligner. This enables one to simultaneously view the wire patterns on the mask and on the underlying substrate. Dust particles or scratches often remain on the substrate even after a thorough cleaning. If these defects are sparse, than the substrate may be translated so that the wires avoid all defects. Aligning the chip’s wire pads along one or more edges of the substrate further constrains the relative position of the photomask to the substrate. It should be noted that it is difficult to properly develop the pads (or other wire features) less than a millimeter from the edge due to photoresist beading. Certain fabrication recipes require the photoresist to be baked and exposed again before developing. For periodic micron-sized features such as those used for making an atom mirror (see Chapter 8), it may help to remove the beaded photoresist at the edge of the substrate to allow the substrate to lie flush against the photomask.

It is good practice to clean the chrome photomasks after every use. Photoresist can stick to the surface, and if left for days, will produce hard-to-remove specs that can block the UV light, creating unwanted features or breaks in the patterned wires. Immersing in a dish of acetone and rinsing with IPA and methanol is sufficient for routine cleaning. Some chrome masks can withstand ultrasound cleaning as well as being wiped with a soft, lint-free cloth, and this seems to be the only way to remove encrusted grime or particulate.

4.2.7 Developing

To remove the photoresist regions defined by the UV exposure, the substrate must be immersed and slightly agitated in a beaker of developer for a few tens of seconds followed by a water rinse. The exact developing time depends on the previous fab-
fabrication steps, but it is generally possible—especially with the transparent sapphire substrates—to see a characteristic change in opacity of the photoresist as it becomes fully developed. For instance, when using a positive process, one first sees the exposed photoresist turn hazy, revealing the wire pattern. After a few seconds, the hazy region sloughs off exposing the bare substrate and leaving darker, patterned regions of photoresist. If a mistake is made at any point in the photolithography process, the substrate can be reused by removing the photoresist in a beaker of acetone and cleaning the substrate as mentioned above, starting with the ultrasound.

4.2.8 Ozone dry stripping

Certain fabrication processes require the substrate surface to be etched in an ozone dry stripper. This uses UV light, ozone, and heat to remove thin films of unwanted organic material, photoresist, or HMDS that may prevent the deposition of thermally evaporated or electroplated gold. The time and temperature of the process may be adjusted to optimally remove organics without over-baking the photoresist.

4.2.9 Wire contacts

Wire bonding and ultrasonic fluxless soldering are useful methods for attaching macroscopic wires to the substrate’s contact pads. Wire bonding is the standard method for making contacts to micro- or nanofabricated devices. The wire bonder attaches each end of a thin thread of gold wire to a pad using a heated, ultrasonically vibrating tip. The thin wire may be stretched over several millimeters between the pad on the substrate and a pad on the substrate support structure. The pads on the support structure may then be connected to standard wire contact pins. Because the wire threads are prone to break and cannot individually support more than a few hundred mA of current, it is necessary to make several redundant bonds per pad. This process can be quite time consuming. As an alternative, ultrasonic soldering irons are capable of attaching regular wires to sapphire or AlN using fluxless solder. Attaching wires is nearly as simple as standard soldering, and the fluxless solder is vacuum compat-
ible to at least $10^{-9}$ Torr. Unfortunately, the solder material forms mounds on the substrate’s surface that can limit optical access.

4.2.10 The mirror

Finally, we would like to discuss methods for making the atom chip’s surface mirror-like. This is a crucial step for ensuring good mirror MOT performance and for minimizing scattered light. The latter is important for imaging the atoms with the substrate as a background.

The most compact method involves simply patterning gold on the entire chip’s surface except for thin, $\leq 10 \mu$m wide gaps around the actual wires [7]. This technique does not add any additional steps to the fabrication procedure, but it does increase the likelihood that surface defects will short the wires through contacts to the large mirrored areas. The mirror gaps that define the wires imprint defects onto the reflected mirror MOT beams, but we have nevertheless been able to trap more than a million cesium atoms with this less than perfect mirror. It is important that the wires themselves are highly reflective. Thermally evaporated or sputtered wires work well for this, but electroplated wires do not. The gold electrodeposition process grows wires with a granularity large enough to scatter light non-specularly. Although we have been able to form good mirror MOTs with electroplated wires, it is impossible to fluorescence image atoms looking down onto the substrate when the atoms are above these wires. This limits diagnostic capability.

Coating the chip’s surface with an insulator and then applying a mirror coating can produce a more specular mirror, though at the expense of additional material between the atoms and the wires. Since the atoms can no longer be trapped immediately above the wires, this limits the maximum attainable trap gradient which scales inversely with trap height. Nevertheless, we have found the various forms of this technique quite useful.

Epoxying a silver mirror (with Epotek 353) to the surface forms a good mirror, and it eliminates any corrugations on the mirror surface caused by the underlying
wires [50]. Unfortunately, the minimum distance between the atoms and the wires is set by the mirror and epoxy thickness. An improved mirror can be made by epoxying a dielectric mirror onto the surface. The mirror was grown on a sacrificial glass substrate with a detachable layer between the mirror and the glass. The device to be mirrored is glued onto the mirror with a thin layer of Epotek 353, and after curing the device plus mirror easily peel-away from the glass substrate. Anti-reflection coatings can be attached to difficult-to-coat windows in the same manner. Vacuum of $2 \times 10^{-10}$ Torr, in a chamber baked to $150^\circ$ C, have been achieved despite using this glue and dielectric coating.

An alternative technique, which hasn’t been completely successful, is to spin one or more layers of photoresist onto the substrate. Swabbing with acetone removes the photoresist covering the wire pads near the substrate’s edge, and the mirror is created by using a mask to thermally evaporate gold only onto the coated region. This technique is simple and works well as long as there are no vertical protrusions of gold from the wires to short to the gold mirror layer. We find that one micron tall wires are fine, but wires 5 to 15 microns tall can on occasion short to the mirror even when the surface is coated with three layers of photoresist. We have tried to wet etch the protrusions away before reapplying the photoresist without success. Another drawback of this method is the fact that the photoresist shrinks after a hard baking. A mirror placed on the photoresist before baking will wrinkle terribly. However, one placed on the resist after a hard bake will not wrinkle too badly after subsequent hard bakes. Unfortunately, the photoresist does not planarize the wires, and the wire pattern and wire surface roughness is mapped onto the mirror. The photoresist is removable with acetone in an ultrasonic bath, and once baked is compatible with vacuums down to at least $10^{-9}$ Torr and perhaps slightly lower.

A similar, but much better technique—no shorting problems—is to use polyimide (Kapton) coatings in place of the photoresist. Polyimide is extremely viscous, and when spun onto a substrate and hard baked, forms a tough yellowish protective

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1This coating is produced by the German company OIB (Optical Interference Components) http://www.oib-jena.de/firmenpreng.html
coating. With a single spin, coatings up to 10 microns can be obtained, and with hard baking the film is UHV compatible and acts to planarize wires or other protrusions on the substrate. It is this last attribute that makes polyimide widely used in the semiconductor industry. We purchased our polyimide, Pyralin PI2560, from HD MicroSystems. The thickness for a spin of 2000 rpm is 8 µm and increases to 11 µm for a 3000 rpm spin. (The company sells a similar polyimide, PI2562, that coats up to 2 µm.) Application requires an adhesion promoter, VM-652, bought in addition to the polyimide. The coating procedure is as follows. Pipet the VM-652 onto the substrate as it is held in the vacuum chuck of the spinner. Wait for 20 seconds and spin dry for 30 seconds. The spin speed can be the same as used in the polyimide application step. Bake the VM-652 coated substrate on a hot plate for a minute at 120° C. Be careful not to crack a custom-cut sapphire substrate—a temperature ramp might be required. Placing the substrate back on the vacuum chuck, pipet enough polyimide to cover roughly half the surface. The spinning will cause it to cover the rest. The rotation should start at 500 rpm for 5 seconds before rotating at final speed—2000 to 3000 rpm—for 30 seconds. Remove substrate, and with a towel soaked in acetone, quickly wipe-off any polyimide coating the bottom of the substrate. To prevent flowing, immediately place the substrate on a ∼100° C hot plate for an initial cure of roughly 5 minutes. One will notice that the polyimide surface becomes smoother as it bakes on the hot plate. To fully cure the polyimide and prepare it for UHV chambers, it must be hard baked to 350° C for an hour. A slow ramp is required to prevent substrate cracking. The Munich group has noticed bubbles forming in the polyimide, but we have never seen this problem. It might have been due to an expired polyimide sample: they bought a new batch of PI2560 and the problem never arose again. The main vat of Pyralin PI2560 must be kept refrigerated, and a sample in a room temperature bottle will expire in a month or so and should be discarded.

We found that for 12 to 14 µm tall wires, the polyimide spun at 2000 rpm produced a 50% planarization (only a ∼6 µm bump remained). A soft bake followed by another coating resulted in a 40% further planarization, but a third soft bake and application
Figure 4.2: Polyimide-coated waveguide atom chips fabricated with electrodeposited gold on custom-cut sapphire. The polyimide has been removed above the wire pads revealing the shiny gold underneath. The substrates have a maximum width of 5 cm in the horizontal direction, and the wires are 12 to 14 microns tall. a) Waveguide with P-trap loading. Minimum wire width is 50 µm. Three coats of polyimide. b) Directly loaded waveguide from U-trap. Minimum wire width of 100 µm. A single coat of polyimide.

didn’t change the height of the bumps. Rather, the bumps simply became wider. After a hard bake, the bump height returned to ~6 µm: the polyimide shrunk slightly. Hard baking between each polyimide application would work much better. Wires much shorter than 10 microns would be much easier to planarize, and the Munich group has found this to be the case. The polyimide surface forms a suitable surface for additional microwires, allowing the creation of multilayered chips. Cured polyimide is easy to flake-off the surface of the substrate, which is necessary for uncovering the wire pads, but seems impervious to acetone. Coating with polyimide forms a UHV compatible and easily cleanable protective layer for the delicate microwires and should, if possible, be used. Figure 4.2 show two sapphire substrates coated with polyimide.

Our first attempt at making a mirror MOT using a gold-coated polyimide and 12 µm tall wires proved unsuccessful. Although it formed a smooth, specular surface, the wire bumps—several 100 microns in width—misdirected enough laser power to prevent the MOT from forming. Further improvements in planarization will mitigate this problem (for instance by hard baking between each layer application), and enable
the use of polyimide as a desirable technique for making atom chip mirrors.

Recently, we have been making atom chip mirrors by simply gold coating a thin—130 to 170 μm—glass cover slide, and attaching it to the chip either face up or down with a small drop of photoresist. The mirror is only 90% reflective when placed upside down due to the Cr adhesion layer. A mirror MOT was made with such a mirror and the low laser scattering allowed nice fluorescence images of the atoms to be taken. We have noticed that Cs from our oven begins to discolor (through accumulation, presumably) the gold mirror after a few months of exposure. A mirror MOT may still be formed, but the mirror scatters more light into the imaging CCD cameras. Using a Cs dispenser might help to improve this situation.

4.3 Specific fabrication techniques: wet etching, ion milling, lift-off method, and electroplating

The minimum required wire dimensions vary significantly depending on the atom chip’s application, and an optimal fabrication technique should be chosen accordingly. This section gives the recipe and discusses the relative merit of each fabrication method.

4.3.1 Wet etching and ion milling

The simplest chip to fabricate has wire widths no smaller than 30-40 μm and wire heights less than 1 μm. A transparency mask should be used for the photolithography (see Section 4.2.1). The wire height is set by a thermally evaporated or sputtered gold layer and the photoresist masks the gold intended for wires from the wet etch solution (see figure 4.3(a)). To begin the procedure, the cleaned substrate should be placed in the ozone dry stripper for five minutes at 65° C to ensure that no organic material will prevent the adhesion of chromium and gold. The thermal evaporation step follows, with the thickness of the gold layer determined by chip’s current density requirements. Because the photoresist adheres well to gold, only a 5 min bake at 180° C is necessary
Figure 4.3: Fabrication techniques. (a) Patterned positive photoresist masks the gold layer from the gold and chromium wet etch. (b) The argon ions mill away the gold not covered by positive photoresist. (c) Gold is thermally evaporated into the trenches patterned in the negative photoresist. The undercut allows the photoresist and unwanted gold to separate from the substrate without peeling away the gold in the trenches. (d) Wires are defined by gaps in the positive photoresist, and the walls of the photoresist guide the wires as they are electroplated. After electroplating, acetone removes the photoresist and gold and chromium wet etches remove the seed layer.
for adhesion (this temperature might be too high for cut sapphire substrates). Wet etching removes exposed gold, and the photoresist should be patterned so that it covers the areas intended for wires, i.e. the photoresist should be a positive image of the wire pattern. A photomask on which the wires are opaque, used in conjunction with positive photoresist, will produce a positive image of the wire pattern. We use the photoresist AZ5214 (Clariant), which can serve as both a negative and positive photoresist depending on the bake and exposure procedure. The positive process recipe is as follows: spin coat at 5000 rpm for 50 s, bake at 95°C for 2 min, expose for 10 to 20 s, and develop in AZ327 MIF (or some similar developer) for 30 s. All of the above times are approximate and will vary depending on the UV light intensity of the specific mask aligner and on various environmental conditions such as humidity. It may be necessary to try various exposure and bake times to find the optimal recipe. These exposure times are based on the 16 mW/cm² UV intensity of our mask aligner. To remove the gold not covered by photoresist, submerge the substrate in gold etch solution (Gold Etchant TFA, Transene Company, Inc., telephone 978-777-7860) for a few tens of seconds until only the dull gray of the chromium layer remains. Finally, remove the chromium layer with chrome etchant (CR-7S, Cyantek, Co., telephone 510-651-3341). Figures 4.4 (a) and (b) show a substrate patterned in this manner. The wet etch dissolves the gold isotropically, and the decrease in wire width is insignificant for wires and wire gaps larger than 10 to 20 µm. Of course, transparency masks cannot be used for features smaller than a few tens of microns.

Ion milling can be a useful alternative to wet etching. Instead of removing the unwanted gold with an etch solution, argon ions anisotropically bombard the surface, removing the gold not covered by photoresist (see figure 4.3(b)). This method can produce very narrow features, limited only by photoresist resolution, with heights determined by the thermally evaporated gold layer. The photoresist is also milled, but this is of no consequence as long as it is thicker than the gold layer. The substrate may become quite hot during the ion etching, and one needs to be careful that the substrate does not overheat, causing the photoresist to become hard and difficult to remove. We have used ion milling to make atom chips as well as to etch a common
Figure 4.4: Gold wire patterned using the wet etch technique. (a) This atom chip contains a quadrupole trap in the U configuration. The gold wire, patterned on sapphire and surrounded by a gold mirror, is 300 µm wide and 1 µm tall. (b) Close-up of the wire region. The gold appears darker than the uncovered sapphire substrate.

The lift-off method

The quick and easy wet etch technique is unfortunately not suitable for wire widths smaller than 20 µm, and ion milling machines are not readily available. The lift-off method should be used for the case in which the wires need not be taller than 1 µm but less than 20 µm wide. However, if the surface quality of the sub-10 micron wires is important to the application (e.g., for BEC experiments), than the lift-off method will be worthwhile regardless of the height of the wires (see Section 4.4 for more details about these constraints).

In contrast to the wet etch technique, the photoresist in this method is used as a mask for the deposition of thermally evaporated gold. Trenches are created in a negative photoresist using a photomask with opaque wires, and evaporated gold deposits both into the trenches, adhering to the substrate, and onto the surface of the photoresist (see figure 4.3(c)). If done properly, the walls of the trenches have an overhang—which looks like an undercut when viewed from above—that prevents the unwanted gold on the photoresist from connecting to the gold in the trenches. An
acetone bath dissolves the photoresist, allowing the unwanted gold to lift-off leaving the wire pattern formed from the gold in the trenches.

After cleaning the substrate, the AZ5214 is spun on the substrate for 45 s at 5000 rpm. The maximum height of the thermally evaporated wires is set by the thickness of the photoresist since lift-off will not work once the top of the gold connects with the gold on the overhang. We have been able to achieve lift-off with wires 1.5 µm tall by spinning the photoresist on at 2000 rpm and thermally evaporating many boats of gold over a period of three to four hours. The photoresist should then be baked for 45 s at 100°C, UV exposed with the photomask for 10 s, baked again for 45 s at 123°C, UV exposed with no mask for 2.1 min, and developed for 25 to 35 s. Developing is finished when one can see the wire pattern in the photoresist. A successful undercut can be seen in a microscope as a bright outline of the edges of the trenches. Before thermal evaporation, the substrate should be placed in the ozone dry stripper at 65°C for 5 minutes. This removes unwanted material that could prevent gold adhesion, and does not seem to hamper photoresist removal as in the electroplating process described below. To promote lift-off, the acetone bath should be heated on a hot plate, and the substrate, while inside the beaker, should be sprayed with an acetone squirt bottle. It is very important that all of the gold-coated photoresist be peeled away before the substrate is removed from the acetone. Otherwise, once dried, the unwanted gold flakes become extremely difficult to separate from the surface. Difficulty in achieving lift-off may be overcome by briefly exposing the substrate to ultrasound. This is risky, however, since the gold wires might be stripped-off as well. Figure 4.1 (b) shows an atom chip fabricated with the lift-off method.

4.3.3 Electroplating

The above methods rely on thermal evaporation to achieve the required wire thickness. This limits the wire heights to \( \sim 1 \mu m \). Electroplating the wires can increase the wire height considerably: for example, we have made 3 µm wide wires 4 µm tall, and 50 µm wide wires 14 µm tall. Thick photoresist spun and patterned on a thin gold seed
layer provide a template for the growth of the wires. The walls of the photoresist maintain a constant wire width as the wire height increases (see figure 4.3 (d)). An acetone wash followed by a brief wet etch removes the photoresist and gold seed layer. Electroplating is a tricky process that does not always produce reliable results. We provide here a general guideline for the process, and with this process we have typically been able to achieve a wire height accuracy of ±0.5 µm.

Fabrication begins with cleaning and ozone dry-stripping the substrate, followed by the thermal evaporation of a 100 to 150 nm seed layer of gold along with a 50 Å chromium adhesion layer. For proper vertical wall guiding of the wires, the photoresist must always be taller than the electroplated wires, and a photoresist thicker than that one used in the aforementioned techniques is necessary. Clariant’s AZ9200 series photoresists are 4 to 24 microns thick, and can achieve aspect ratios of 5 to 7 with resolutions of < 1 µm to 3.5 µm depending on the resist thickness. After spin coating, it should be baked on a hot plate at 110° C for two minutes, and then the photoresist should be UV exposed for 60 s (or longer depending on the photoresist thickness) using a photomask with transparent wire patterns. The resist is developed in a 1:4 solution of AZ400K and water for 10 seconds to a minute depending on the exact solution concentration: the exposed photoresist will turn hazy before dissolving away. The gold seed layer also acts as the cathode in the electroplating process, and some of the photoresist must be wiped away with acetone—or a blank spot should be designed in the photoresist—to serve as a contact for the cathode lead. An ozone dry etch is then used to remove any layers of HMDS, photoresist, or organics that might mask regions of the gold from the electroplating solution. The time and temperature of this process is crucial: too long an exposure at too high of a temperature will make the photoresist difficult to remove between closely spaced wires, and too short an exposure will not remove enough unwanted masking material. For example, we found that an 18 s room-temperature ozone dry etch was optimal for removing unwanted material while also enabling the removal of photoresist between wires spaced by 3 µm.

Alternatively, if a rectilinear wire cross-section is not desired, than the cathode
may be connected to the wires on the substrate post-acetone removal. The wires may be formed from performing lift-off, wet-etch, or ion milling and should all be shorted together with connections that are subsequently scratched-out. These electroplated wires grow horizontally as well as vertically with roughly semicircular cross sections.

We use an ammonium gold sulfite solution from Metakem GmbH for the electroplating. A sodium gold sulfite solution from Technic, Inc. did not work as well. Specifically, it would turn brownish (from clear) during a deposition, preventing it’s reuse and causing large towers of gold to form on the wire. The Metakem solution, with 15 g of Au/liter, is poured into a roughly 1200 mL container and heated to ~65°C. The anode, also purchased from Metakem, is platinized titanium (type B mesh, size 10 × 10 cm). Place the anode mesh vertically into the container so that a part of it is above the solution. The depth of the container should be so that the sample, when suspended vertically in the solution, is completely submerged: any excess solution will be unnecessarily subject to evaporation. Attach the positive alligator clip to the anode mesh outside the solution and the negative clip to the substrate’s gold seed layer (the cathode). The cathode alligator clip usually has to be in contact with the solution for the substrate to be completely submerged. The current should be off when the substrate is submerged and turned on or off gently thereafter. We have found that a 1 mA current does not activate the deposition, but a 20 mA current deposits 6 to 7 microns of gold per 20 min. With a 40 min deposition, 12 to 14 um tall wires can be made. The substrate should be gently agitated while electroplating to promote even plating and suppress the formation of ~5 µm tall towers of gold. After electroplating, the substrate, anode, and container should be rinsed with water. The gold solution can be reused, but should be filtered if flakes of material appear.

Both our group and the Munich group noticed an uneven, shadow-like effect on the cross-sectional height of electroplated wires using the Metakem solution. The section of an exposed wire next to a steep photoresist wall will not electroplate as well if the solution is stirred so that the wall creates a fluidic shadow on the wire: the wire’s cross-section is no longer rectilinear, but rather thins on one side. Reversing the direction of fluid rotation creates wire thickness shadows on the wire’s opposite
side. Agitating the substrate in random directions helps to mitigate this effect, and the Munich group saw that it might be preferential to not stir the solution at all. They also noticed that the use of a fresh batch of solution seems to mitigate this problem.

To prepare for wet etching the seed gold layer away, the photoresist should be removed in a room-temperature acetone bath. Sometimes it is difficult to remove the photoresist between wires spaced only several microns from one another, and in these cases the substrate—while in the acetone—should be placed in an ultrasound for a few minutes. The gold should not peel away since it is attached to the entire substrate surface. After rinsing the acetone away with IPA and methanol, the gold seed layer is removed with a ~15 s wet etch. The chromium adhesion layer should also be wet etched away. Occasionally, the air jet does not remove all of the methanol from the substrate, and tiny drops of methanol can sometimes dry on the leeward side of the wires. This dried methanol acts as a mask for the gold etch, leaving small puddles of seed layer that can short adjacent wires. These puddles can be removed by rinsing with methanol, blow-drying from a different angle, and briefly wet etching a second time. The surface reflectance of the gold is typically diminished after the wet etch, and a mirror fabricated with this gold may not be ideal. A second photolithography step can add photoresist on top of the wires and/or areas of the seed layer to protect them from the wet enchant. The protected seed layer is suitably reflective for forming a mirror MOT.

A surface profilometer, commonly known as an alpha step machine, is quite useful for quickly measuring the height of the wires. Inevitably, a few substrates must be spent optimizing the electroplating process for a specific wire height. Figures 4.5 (a) and (b) show an atom chip-based BEC interferometer that we fabricated by electroplating on an AlN substrate\(^2\). The smallest features are five, 1 mm long wires that are each 3 \(\mu\)m wide, 4 \(\mu\)m tall, and spaced less than 3 \(\mu\)m from one another.

\(^2\)Wire pattern designed by T. Steinmetz and P. Hommelhoff at the MPQ/LMU in Munich. See Chapter 10 for more details.
4.4 Trap fragmentation

In 2002, it was discovered that BECs in an elongated, cigar-shaped trap held within tens of microns from the wire surface can fragment into “sausage-link” sections [93, 94, 95, 62, 96]. This is due to the roughness and meandering of the wire surface which results in the deviation of the wire current away from linear propagation along the wire. An errant magnetic field $10^3$ to $10^4$ times smaller than the trapping field causes the BEC to fragment into local potential valleys. In the last two years, groups determined that electroplating wires is much worse for making smooth wires and is the main culprit behind this fragmentation problem [97, 91]. Thermal evaporation and sputtering are superior for creating smooth wires and should be used in experiments that confine BECs in tight traps near the wire surface.
4.5 Conclusion

The techniques described in this paper provide a basic starting point for the design and fabrication of atom chips. The precise control of atomic position enabled by these chips is quite crucial to many areas of research. Moreover, these devices allow an incredible miniaturization of experiments involving cold atoms. From constructing atom optical elements to studies of BECs and cavity QED, atom chips are proving invaluable to the fields of atomic physics, quantum optics, and quantum computation.