

ANALYSIS AND DESIGN OF CMOS WIDE-BAND LOW
NOISE AMPLIFIERS

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I certify that I have read this thesis and that, in my opinion, it is fully adequate in scope and quality as a thesis for the degree of Engineer.

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Approved for the University Committee on Graduate Studies.

Abstract

The implementation of Low Noise Amplifier (LNA) front-ends is one of the challenging aspects in emerging Ultra Wide-Band (UWB) radio frequency (RF) systems. As it is highly desirable to achieve complete system-on-chip (SoC) integration, several CMOS based LNA implementations have been reported recently. The first part of this thesis presents a comparative study that helps designers understand the merits and demerits of different wide-band LNA implementation choices. In order to enable a quantitative comparison, a Figure Of Merit (FOM) that captures the tradeoffs among linearity, noise figure (NF), power dissipation and utilization of raw technology speed is proposed. The obtained survey results based on this FOM suggest that distributed amplification outperforms approaches that utilize wide-band matching networks or noise cancellation techniques.

The second part of this thesis deals with the design and analysis of low power distributed amplifiers. In order to understand the tradeoffs better, the factors affecting gain, power and bandwidth of a distributed amplifier are discussed in detail. This thesis concludes with the design and simulation of the proposed low power architectures in 0.18μ CMOS technology.

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Chapter 1

Introduction

CMOS Radio Frequency (RF) integrated circuits have gained widespread use because they can be implemented on the same substrate with densely integrated baseband functions. The recent success in the commercialization of single chip Bluetooth and IEEE 802.11 WLAN transceivers [1] suggests that SoC RF circuit integration will continue to play a major role in emerging cost-constraint systems that heavily rely on baseband signal processing. Ultra Wide Band (UWB) transceivers fall into this category, as they promise to deliver an attractive solution for cost efficient and high-performance data transmission for future wireless applications [2].

An irreplaceable component of virtually any RF receiver is a front-end Low Noise Amplifier (LNA). As the first stage of the receiver, LNAs are required to have high gain and low Noise Figure (NF). Many implementations of narrow band LNAs exist in literature (e.g. [3]) and are well understood. From the perspective of a basic MOS two-port, it can be shown that the optimum driving source susceptance for minimum NF is inductive in character, but has a capacitive variation [4]. Furthermore, the optimum driving conductance should vary linearly with frequency. Achieving such a noise match, together with a good source impedance termination is especially difficult for wide-band systems as it involves synthesizing a network that provides these characteristics over a large frequency range.

Recently, several innovative wide-band LNA architectures have been proposed to take on this challenge [5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16]. In this work, we introduce a suitable Figure Of Merit (FOM) that enables a quantitative comparison of CMOS LNA implementations and allows the designer to reason about the involved design tradeoffs. The proposed FOM extends the metric proposed in [17] by including an additional factor that accounts for bandwidth tradeoffs in a given technology. The obtained survey results based on this FOM suggest that distributed amplification outperforms approaches that utilize wide-band matching networks or noise cancellation techniques.

Several CMOS Distributed Amplifier (DA) topologies [10, 11, 12, 13, 14] exist in literature. However conventional DAs suffer from relatively high power consumption. This work focuses on the design and analysis of DAs with emphasis on low power. In order to understand the tradeoffs better, the factors affecting gain, power and bandwidth of a DA are discussed in detail.

This thesis is organized as follows. Chapter 2 briefly reviews existing wide-band LNA implementations. Chapter 3 discusses a FOM tailored for comparison of wide-band LNAs in CMOS technology. FOM results for various implementations are tabulated and discussed. Chapter 4 discusses the existing and the proposed low power DAs. Chapter 5 presents the simulation results of various DA implementations. This thesis ends with a brief conclusion and suggestions for future work in Chapter 6.

Chapter 2

Wide-Band LNAs

A wide-band LNA design must not only match the source impedance over a wide range of frequencies, but also provide low NF, flat gain and high linearity at the same time. This section provides brief overview of existing wide-band LNA architectures that aim to address these design objectives.

2.1 Wide-Band Filter Matching Networks

As mentioned in the introduction, good noise matching requires a source susceptance which is inductive in character with a (negative-) capacitive variation. A lossy resonant circuit can imitate the behavior of a (negative-) capacitor or inductor in the frequency range close to its resonance. Such an input section can be embedded in a multi-section bandpass filter [5] to resonate its reactive part over the whole band. The CMOS implementation in [5] is based on a three section Chebyshev filter prototype (Fig. 2.1). Here, the standard inductive source degenerative topology with a cascode device is used to achieve good impedance matching and low NF. The load is designed to achieve flat gain over a large bandwidth and uses shunt-peaking to compensate for gain roll-off at higher frequencies. Similar work was presented in [15], using SiGe technology.

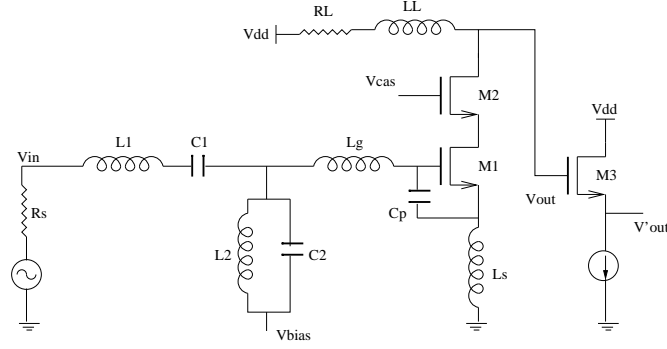


Figure 2.1: Wide-band Filter Matching Network Approach

2.2 Noise Canceling Techniques

A feedforward noise canceling technique [8] has been proposed to achieve low NF and source impedance matching in a shunt feedback architecture. Fig. 2.2a) shows the implementation reported in [8]. The signal voltages at node X and node Y have

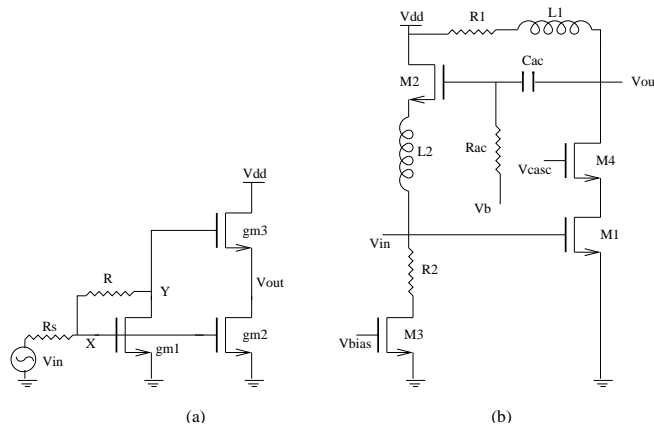


Figure 2.2: a) Feedforward Noise Canceling b) Noise Canceling with Common Drain Feedback

opposite signs, whereas the noise voltages from the matching device g_{m1} have the same sign. With the addition of an appropriately scaled second stage (g_{m2} , g_{m3}), the signal voltages of these nodes are added and the matching device noise is cancelled. Through this effect, it is possible to achieve extremely low NF. Other advantages of this architecture lie in its unconditional stability, small area (no inductors), and good immunity to process spread [8].

Noise cancellation and impedance matching can also be achieved using a common

drain feedback stage [9]. Here, the input impedance is set by the feedback stage which also partly cancels the input transistor noise. Fig. 2.2b) shows one of the pseudo-differential input stages of this implementation. This design reduces the dependence of input impedance on the sizing of the signal path transconductor, which creates an additional degree of freedom for optimization.

2.3 Distributed Amplifiers

High bandwidth, low noise amplification has also been demonstrated using DAs [10, 11, 12, 13, 14]. Conceptually, a DA (Fig. 2.3) consists of a pair of input and output transmission lines coupled by transconductance of MOSFETs. The transmission lines

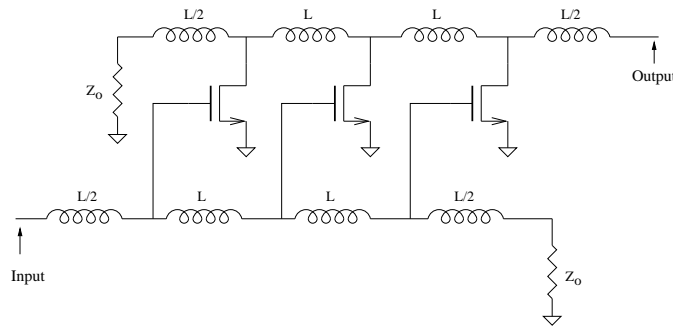


Figure 2.3: Ideal Three-Stage Distributed Amplifier

are formed using lumped inductors and are referred to as the gate and drain lines. The gate line is periodically loaded by the MOSFET gate-source capacitance and is terminated in its characteristic impedance at the end. As the RF signal travels on the gate line, each transistor is excited by the traveling voltage wave and transfers the signal to drain line through its transconductance. If the phase velocities on the gate and drain lines are equal, then the signals on the drain line add in the forward direction as they arrive at the output. The out-of-phase wave traveling in the reverse direction will be absorbed by the drain-line termination.

Due to the typically large number of transconductance stages used, the power

consumption of DAs tends to be higher than that of more conventional one- or two-stage LNAs, at the benefit of potentially superior bandwidth. Another drawback of this approach lies in the large number of area-consuming passive components.

Chapter 3

Figure of Merit

It is interesting to examine the architectures discussed in Chapter 2 in terms of achieved performance, expressed as a single number FOM. Several figures of merit for LNAs have been suggested in literature. [18] uses noise measure ($NM = \frac{F-1}{1-1/G}$), where F is the noise factor and G is the LNA gain. Noise measure captures the trade-offs between noise factor and gain, but does not include information about power consumption, bandwidth or linearity. [19] suggests the use of the product of noise measure and power dissipation. The work in [20] introduces a FOM based on linearity and NF. [21] uses a FOM based on dynamic range, which includes noise measure, linearity and also power consumed. [17] provides a compact FOM using NF, linearity and power consumption. In this thesis, we augment this metric with an additional factor that captures bandwidth tradeoffs.

In wide-band CMOS amplifiers, there exists a fundamental tradeoff between power efficiency and bandwidth. This tradeoff can be understood by considering a single MOS transconductance stage. To first order, assuming a square law transistor model, the obtained transconductance per drain current invested is given by

$$\frac{g_m}{I_D} = \frac{2}{V_{ov}} \quad (3.1)$$

where V_{ov} is the quiescent point gate overdrive $V_{GS} - V_{TH}$ of the device. Unity

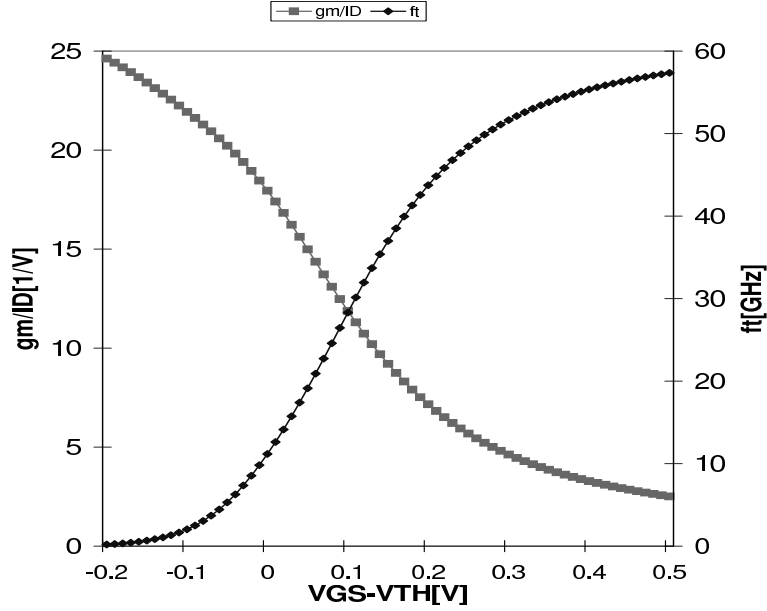


Figure 3.1: $\frac{g_m}{I_D}$ & f_t Vs V_{ov} for $0.18\mu\text{m}$ Technology

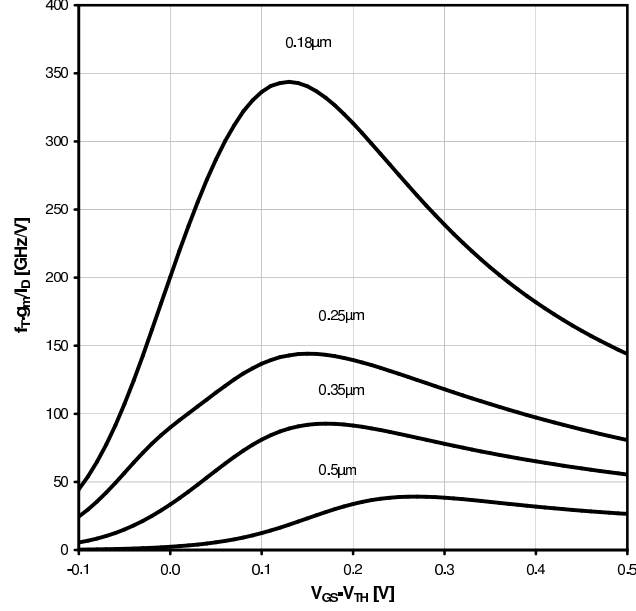
current gain bandwidth, on the other hand, is

$$f_t \approx \frac{\mu \cdot V_{ov}}{L^2} \quad (3.2)$$

$$\frac{g_m}{I_D} f_t \approx \frac{2\mu}{L^2} \quad (3.3)$$

where μ is the channel mobility and L is the channel length. Typically, the available f_t is directly related to the achievable bandwidth of a wide-band LNA, and should therefore be included in figure of merit considerations. From the above equations, it can be seen that the product $\frac{g_m}{I_D} \cdot f_t$ is constant for a given technology, independent of the chosen V_{ov} . Hence, to first order, there exists a linear tradeoff between power dissipation and bandwidth.

Figs. 3.1 and 3.2 plot n-channel simulation data of $\frac{g_m}{I_D}$, f_t and their product versus V_{ov} and for various standard CMOS technologies. These results are based on public domain BSIM3v3 device models from the MOSIS foundry service. This data illustrates that the product of transconductor efficiency $\frac{g_m}{I_D}$ and f_t is not constant,

Figure 3.2: Product $\frac{g_m}{I_D} \cdot f_t$ Vs V_{ov}

but peaks around gate overdrive voltages of 150-200mV. For very small gate overdrive $V_{ov} (< 100mV)$, the device enters a region close to bipolar operation and $\frac{g_m}{I_D}$ is bounded by the value $\frac{1}{n \cdot kT/q}$, where n is the transistor's sub-threshold slope factor. For large overdrive, velocity saturation and mobility degradation cause $\frac{g_m}{I_D}$ to be 10-25% below the square law estimate. Nevertheless, as long as the device is biased near the practical, shallow operating region around the product peak, the bandwidth-power tradeoff is nearly linear.

Based on this observation, we propose a FOM of the following form:

$$FOM = \frac{P_{1dB}}{P_{noise}} \frac{1}{P_{dc}} \frac{f_h}{f_{t*}} \quad (3.4)$$

As in [17], this expression includes the output 1dB compression power (P_{1dB}) as a measure for linearity, DC power consumed (P_{dc}), and output noise power ($P_{noise} = P_{th} \cdot F \cdot Gain$), where $P_{th} (= kT)$ is the thermal noise floor given by -174 dBm/Hz at $T = 290K$. In addition, we introduce a relative measure for bandwidth through a bandwidth utilization factor (BUF) f_h/f_{t*} , where f_h is the upper LNA corner frequency and f_{t*} is the technology f_t around the maxima of Fig. 3.2. The normalization

Table 3.1: f_{t*} for different Technologies at peak $\frac{gm}{I_D} \cdot f_t$

Technology (um)	0.8	0.5	0.35	0.25	0.18
f_{t*} (GHz)	4	5.8	8.13	15.4	33.7

Table 3.2: Comparison of Different Implementations

Impl	Tech (um)	Gain (dB)	BW (GHz)	NF (dB)	P_{1dB} (dBm)	P_{dc} (mW)	FOM (dB-Hz/mW)
[5]	0.18 CMOS	9.3	2.3-9.2	4.0	(-5.7)	9	139.82
[8]	0.25 CMOS	13.7	0.002-1.6	2.4	(4.7)	35	137.33
[9]	0.18 CMOS	12.2	1-7	5.1	(-3)	75	128.13
[16]	0.4 CMOS	24	0.42-1.18	2.3	(0.18)	35	123.60
[11]	0.6 CMOS	7.4	0.5-5.5	6.86	6-8.8	83.4	146.53

with respect to f_{t*} allows a technology independent comparison, and helps quantify how efficiently available device f_t is translated into wide-band LNA performance. Typical data for f_{t*} is summarized in Table 3.1.

The performance and FOM results of several recent CMOS wide-band LNA implementations are summarized in Table 3.2. For Simplicity, the NF used in these comparisons are measured at a single frequency. Note that from a system perspective, it is actually more appropriate to consider the exact frequency dependence of the NF as well [22, 23]. Since some publications did not report P_{1dB} , it is estimated from P_{IIP3} performance using $P_{1dB} = P_{IIP3} - 9.64dB + Gain(dB)$ [20]. The estimated values are indicated using () in Table 3.2.

Fig. 3.3 compares the proposed FOM for different implementations. The work of [5] exhibits only a fair NF and linearity. Nevertheless, the design achieves a good FOM due to a high BUF and low DC power consumption. The noise cancelling technique presented in [8] uses a large P_{dc} to achieve low noise figure and good linearity, and thereby achieves comparable performance to [5]. This topology is, however, fundamentally limited by a low BUF. This can be seen from the circuit diagram shown

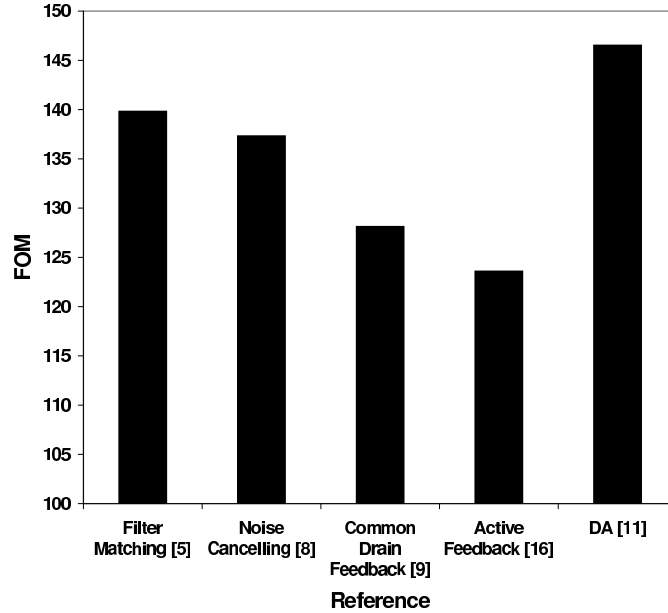


Figure 3.3: Comparison of the Figure of Merit

in 2.2a). In order to achieve noise cancellation and low NF, a large g_{m2} is needed [8]. However, a large g_{m2} not only adds power, but also significantly lowers the dominant pole frequency at node X. The noise cancelling design of [9] achieves higher bandwidth, but also suffers from a very steep tradeoff between NF and P_{dc} . [16] has both a fairly low BUF and, which results a small FOM. The distributed amplifiers presented in [10, 11, 12] have excellent BUFs, but suffer from high P_{dc} because of their distributed nature. However, it is shown later in Chapter 4 that P_{dc} can be reduced with some low power techniques. Still, the design of [11] achieves the highest overall FOM. Unfortunately, the designs of [10, 12] could not be included in this survey, due to the lack of linearity data. Nevertheless, the vastly superior performance of [11] suggests that distributed topologies are well suited for wide-band, low noise amplification.

Chapter 4

Distributed Amplifiers

4.1 Background

The concept of distributed amplification [24] is not new to wide-band amplifier designers. It was first proposed in 1937 by Percival [25] as a means of improving the gain-bandwidth product of wide-band amplifiers by adding the transconductance of individual tubes while separating their capacitances. This way, it was possible to achieve an amplifier with f_h greater than the one that resulted by a simple parallel connection of the tubes. A detailed theoretical paper by Ginzton et al. [26] in 1948 made the concept of distributed amplification popular. Since then, numerous researchers extended the analysis and implemented distributed amplifiers (DAs) using Si MESFETs due to their attractive properties. It was not until recently that researchers started looking into CMOS (MOSFET) implementations of DAs.

Following a first design by Ayasli [27], various architectures of DAs were implemented utilizing GaAs Monolithic Microwave Integrated Circuits (MMIC). Primarily, three kinds of DAs topologies appear in literature

- Basic single transistor gain stage [11] (Figure 4.1)
- Single stage cascaded [14] (Figure 4.2)
- Gain stage using Cascoding [12] (Figure 4.3)

Various derivatives of the above architectures also exist, with features like tapering [13] etc.

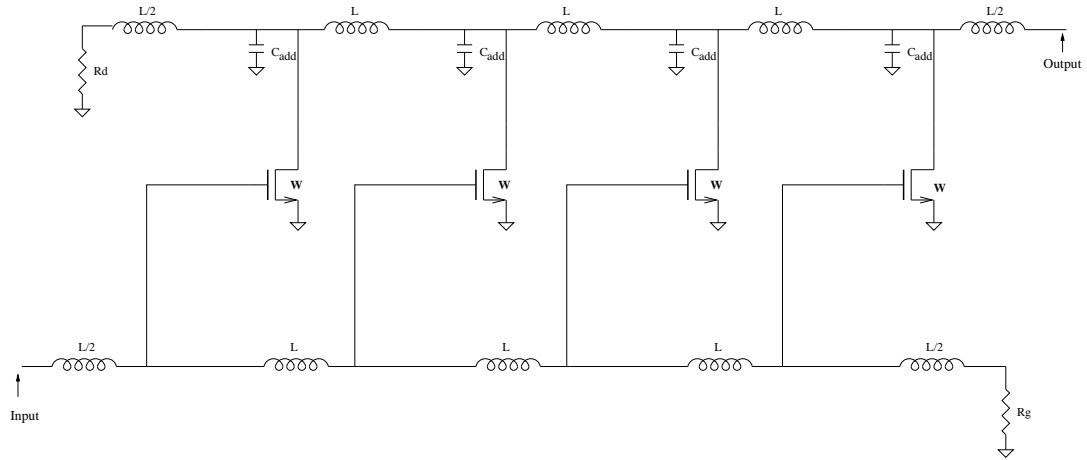


Figure 4.1: Basic Four Stage Distributed Amplifier

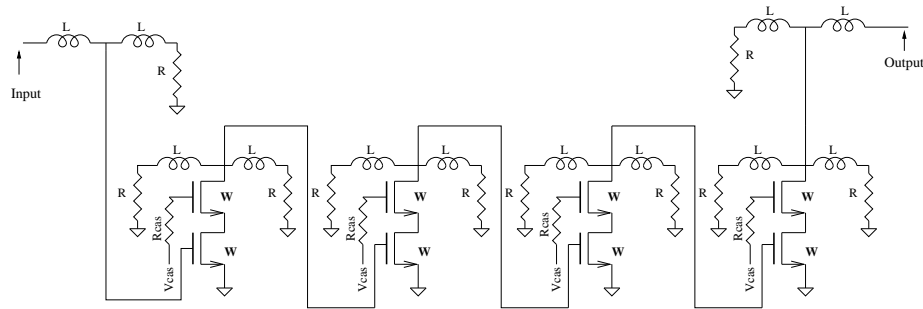


Figure 4.2: Four Stage Single Stage Cascaded Distributed Amplifier

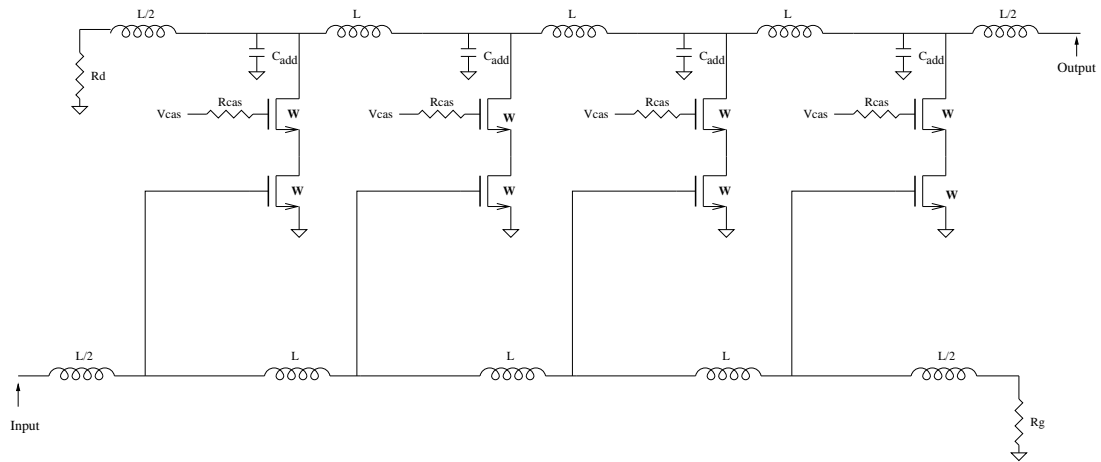


Figure 4.3: Four Stage Distributed Amplifier With Cascode

4.2 Detailed Operation

Conceptually, a DA (Fig. 4.1) consists of a pair of input and output transmission lines coupled by transconductance of MOSFETs. The transmission lines are formed using lumped inductors and are referred to as the gate and drain lines. The gate line is periodically loaded by the MOSFET gate-source capacitance and is terminated in its characteristic impedance at the end. As the RF signal travels on the gate line, each transistor is excited by the traveling voltage wave and transfers the signal to drain line through its transconductance. If the phase velocities on the gate and drain lines are equal, then the signals on the drain line add in the forward direction as they arrive at the output. The out-of-phase wave traveling in the reverse direction will be absorbed by the drain-line termination. The amplified signals at each stage travels towards the load. The signal gets attenuated due to non-zero losses associated with the transmission lines. Finite Q inductors are the primary source of losses in the gate line. Losses in the drain line can be attributed to lossy inductors and the drain-source resistance (r_{ds}).

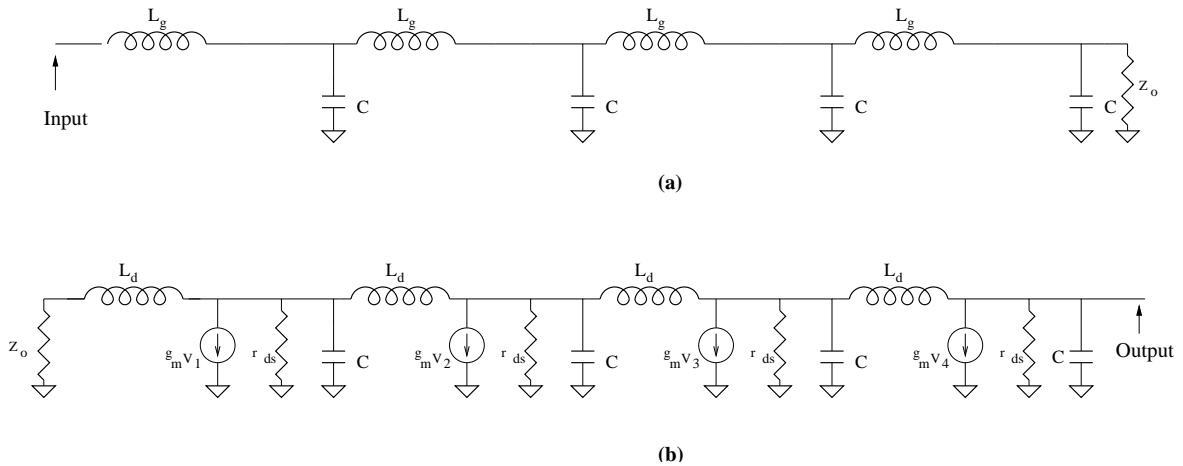


Figure 4.4: a) Gate Line Model b) Drain Line Model

A detailed analysis for a DA using GaAs MESFETs is presented in [28, 29, 30]. This analysis can be used to derive the gain equations for a CMOS DA. The gain equation for a more generalized DA model is given by

$$Gain = \frac{g_m}{2} \sqrt{\frac{Z_1^d Z_2^d}{1 + \frac{Z_1^d}{4Z_2^d}}} \frac{e^{-N \frac{(A_g + A_d)}{2}} \sinh\left[N \frac{(A_d - A_g)}{2}\right]}{\sinh\left[\frac{(A_d - A_g)}{2}\right]} \quad (4.1)$$

Appendix A presents the detailed derivation of the above gain equation.

The gain equation 4.1 assumes the following

- Unilateral MOSFET model (ignores C_{gd})
- Image impedance matched terminations (See Appendix A)
- Equal gate and drain phase velocities

For the DA model shown in Figure 4.4, the various parameters in equation 4.1 can be expressed as

$$Z_1^g = j\omega L_g \quad (4.2)$$

$$Z_2^g = \frac{1}{j\omega C_{gs}} \quad (4.3)$$

$$Z_1^d = j\omega L_d \quad (4.4)$$

$$Z_2^d = \frac{1}{\frac{1}{r_{ds}} + j\omega C_{db}} \quad (4.5)$$

where L_g and L_d are the series gate and drain line inductances. C_{gs} and C_{db} are the gate-source and drain-bulk capacitances of the MOSFET. r_{ds} is the shunt resistance of the MOSFET and ω is the operating frequency. The characteristic impedance (Z_o) and cut-off frequency (f_c) of lossless transmission line are given by

$$Z_o = \sqrt{\frac{L}{C}} \quad (4.6)$$

$$f_c = \frac{1}{\pi\sqrt{LC}} \quad (4.7)$$

For having the same Z_o and f_c , the capacitance and inductance on both the drain and gate lines should be the same. For a MOSFET C_{db} is usually less than C_{gs} , hence a capacitor C_{add} is added in shunt to the drain to make the capacitances equal.

$$L_g = L_d = L \quad (4.8)$$

$$C_{gs} = C_{db} + C_{add} = C \quad (4.9)$$

From Equations 4.1, 4.4, 4.5, 4.2, 4.3, 4.7, the gain of the DA can now be expressed as

$$Gain = g_m \frac{Z_o}{2\sqrt{1 - (\frac{f}{f_c})^2}} \frac{e^{-N\frac{(A_g+A_d)}{2}} \sinh[N\frac{(A_d-A_g)}{2}]}{\sinh[\frac{(A_d-A_g)}{2}]} \quad (4.10)$$

where A_d and A_g are the attenuation of the drain and gate lines. g_m is the transconductance of the MOSFET and N is the total number of stages.

The optimum number of stages that maximizes the gain is simply a function of gate and drain line attenuation. As the signal propagates along the gate line towards the termination, less signal is available for each MOSFET because of attenuation. Hence, the overall gain degrades with further increase in the number of stages. Unfortunately, the optimum number of stages cannot be easily obtained since the gate and drain line attenuations are complex functions and depend on the specific MOSFET parameters and also on the operating and cut-off frequencies. The number of stages for this work is chosen as 4 which was found to be optimum in [28, 29].

The attenuations of the gate and drain line with finite Q inductors is given by

$$A_d = Re\left\{\sqrt{(j2\pi fL + R)\left(\frac{1}{r_{ds}} + j2\pi fC\right)}\right\} \quad (4.11)$$

$$A_g = Re\{\sqrt{(j2\pi fL + R)(j2\pi fC)}\} \quad (4.12)$$

where R is the series resistance of the finite Q inductors.

Further from Equations 4.11 and 4.12, it can be observed that the gate and drain line attenuations are frequency dependent, affecting the flatness of the gain magnitude. It was shown in [13, 28, 29] that this frequency dependence is reduced as the cut-off frequency of the line increases.

The power gain can be calculated from voltage gain as

$$|Gain_P| = |Gain|^2 |Z_o|^2 \quad (4.13)$$

which can be further simplified for a lossless case as

$$|Gain_P^{LL}| = \frac{n^2 g_m^2 |Z_o|^2}{4} \quad (4.14)$$

4.3 Cascode Stage

A cascode stage is added to the DA [12] to decrease the variation in the capacitance seen by the transmission lines which is caused by Miller effect. Also the cascode stage improves the gain and provides isolation from the signal on the drain line coupling back to the gate line.

Figure 4.5a) shows a simple gain stage with MOSFET parasitic capacitances. Figure 4.5b) shows the equivalent capacitances on the gate and drain line because of Miller effect. $A_v (= g_m Z_o)$ is the gain of the stage and is usually high, as one desires high output power. The effective capacitance on the gate line is larger than C_{gs} and the effective Z_o is less than desired, affecting the overall gain. Figure 4.5c) and 4.5d) show the cascode gain stage with the parasitic capacitances. A cascode gain stage helps in reducing the effective capacitance on the gate and drain lines compared to

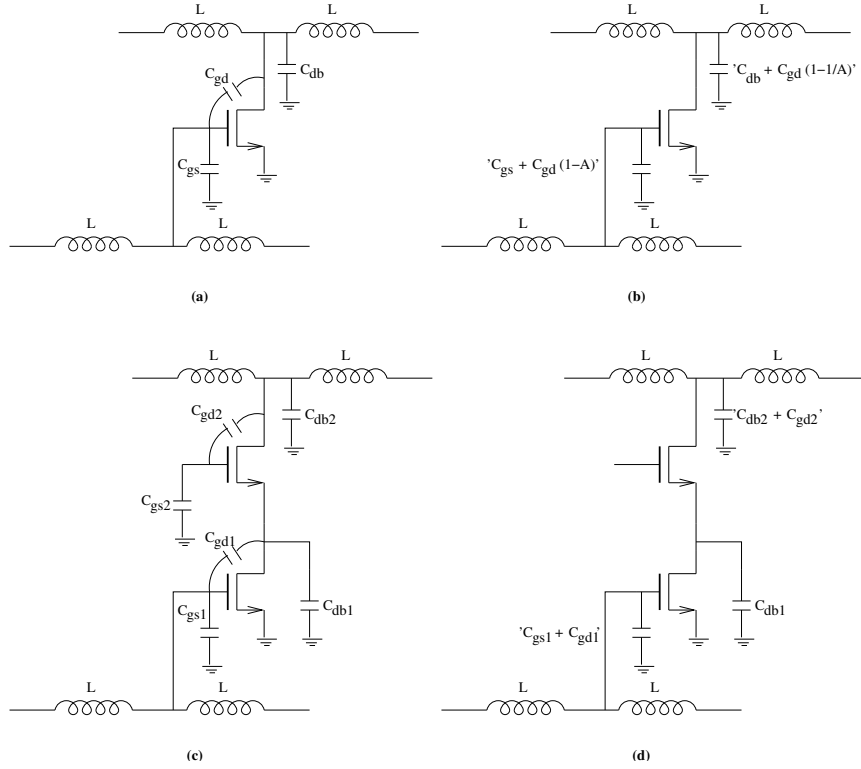


Figure 4.5: a) Simple gain stage b) Simple Gain Stage With Miller Effect c) Cascode Gain Stage d) Cascode Gain Stage With Miller Effect

the simple gain stage. This slight variation in capacitance on both the drain and gate lines causes only a slight variation in Z_o .

4.4 Low Power Technique

Traditionally, DAs have been terminated with an impedance of 50Ω . This requires that the characteristic impedance of the artificial transmission lines be 50Ω to minimize the losses caused by the impedance mismatches. From equation 4.14, the gain of the DA increases with Z_o . Using a higher Z_o to 50Ω helps improving the gain without any increase in power to first order. Considering this technique in detail leads to some interesting conclusions investigated in this section.

C of the gate line comes primarily from the gate capacitance (C_{gs}) of the MOSFET and is given as

$$C = WLC_{ox} \quad (4.15)$$

where C_{ox} is the oxide capacitance per unit area. W and L are the width and length of the MOSFET. C_{ox} is fixed for a given technology and L is fixed considering minimum length devices. Hence from equation 4.15, C is determined by W . The transconductance (g_m) and DC bias current (I_{dc}) of a long-channel MOSFET are given by

$$g_m = \sqrt{\frac{2I_{dc}W\mu C_{ox}}{L}} \quad (4.16)$$

$$I_{dc} = \frac{1}{2} \frac{W}{L} \mu C_{ox} V_{ov}^2 \quad (4.17)$$

$$\frac{g_m}{I_{dc}} = \frac{2}{V_{ov}} \quad (4.18)$$

where V_{ov} is the quiescent point gate overdrive $V_{GS} - V_{TH}$ of the device and μ is the channel mobility.

Further from 4.6, 4.7, Z_o can be expressed in terms of f_c and C as

$$Z_o = \frac{1}{\pi f_c C} \quad (4.19)$$

Some important observations can be made from equations 4.6, 4.7, 4.16, 4.17, 4.18, 4.19

- Power gain can be increased by increasing g_m or Z_o
- Z_o can be increased by increasing L . This comes with a larger attenuation due to the finite Q of the inductors.
- Decreasing C increases both f_c and Z_o , but this comes from a lower width and hence less g_m .

- For a given C , f_c and Z_o are inversely proportional to each other
- Increasing W , increases C which in turn decreases f_c and Z_o
- g_m/I_{dc} can be improved by decreasing V_{ov} or by increasing W
- For a given I_{dc} , Increasing W decreases V_{ov}

The power of the DA can be decreased by biasing the gain stages with optimum overdrive, which is usually closer to sub-threshold as mentioned in Chapter 3. This might have a negative effect on linearity as the the device operation closer to sub-threshold is more non-linear. However, since DAs are known for their excellent linearity [10, 11, 12], it seems possible to exploit this trade-off for lower power.

A two stage gain stage instead of a single stage gain stage can help to solve the problem. The first stage is going to present a lower capacitance to the transmission line and the second stage is the primary gain stage. The gain of the first stage should be greater than or equal to one, so that power consumed by the second stage is kept same as the single stage design. This topology uses additional power for the first stage. However, since the first stage is not the primary gain stage and is used only for impedance matching, the power consumed by it can be kept at minimum.

4.4.1 Source Follower as the First Stage

A source follower is identified to be a good choice for the first stage. Figure 4.6 shows a four stage DA with source follower.

The gain of the source follower is given by

$$|A_{vsf}| = \frac{g_{m1}(|r_{ds1}| \frac{1}{j\omega(C_{gs2}+C_{db1})})}{1 + g_{m1}(|r_{ds1}| \frac{1}{j\omega(C_{gs2}+C_{db1})})} \quad (4.20)$$

where C_{gs2} and C_{db1} are the gate-source and drain-bulk capacitances of the second stage respectively. g_{m1} and r_{ds1} are the transconductance and drain-source shunt resistance of the source follower. As can be inferred from the above equation, the

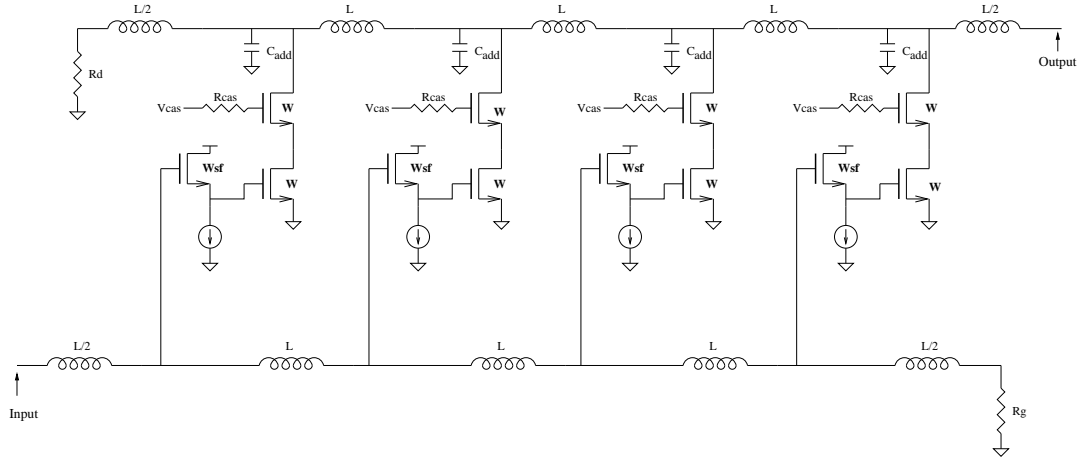


Figure 4.6: Four Stage Distributed Amplifier with Source Follower

gain of the source follower starts decreasing by a significant amount once the output load impedance decreases below a certain value. The second stage acts as a capacitive load (C_{gs2}) to the source follower stage. The g_{m2} of the second stage can be increased by increasing the width W of the transistor. Increasing W , increases the capacitive load (C_{gs2}) for the source follower, which decreases the gain (well below one) at higher frequencies. However, with careful design, and appropriate impedance matching techniques, this topology can be used to achieve low power. An inductance placed between the output of the source follower and the input of the second stage can be used to compensate for the decrease in impedance at higher frequencies. As the frequency increases, the increase in impedance of the inductor compensates for the decrease in impedance of the load capacitor. A series drain inductor used with the cascode stage also helps in improving the gain at higher frequencies. Figure 4.7 shows the four stage DA using source follower with series inductor for both the first and second stage. The values of the series inductors depends on the sizes of the transistors and are usually smaller than L as they only serve to counterbalance the gain roll-off due to relatively small capacitance.

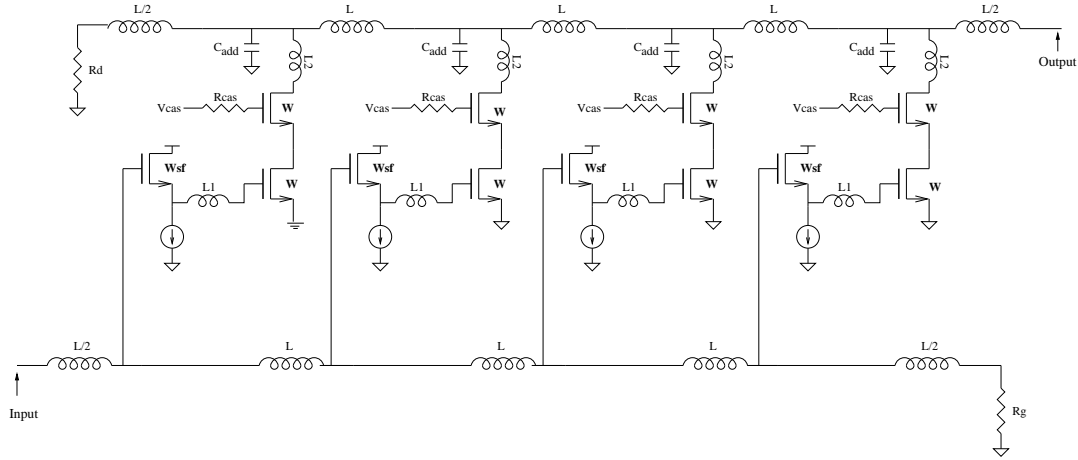


Figure 4.7: Four Stage Distributed Amplifier with Source Follower and Series Inductors

4.4.2 Cascode gain stage as the First Stage

A Cascode gain stage was also considered as the first stage. Figure 4.8 shows the schematic of the four stage DA with two cascode stages in each gain stage. The gain

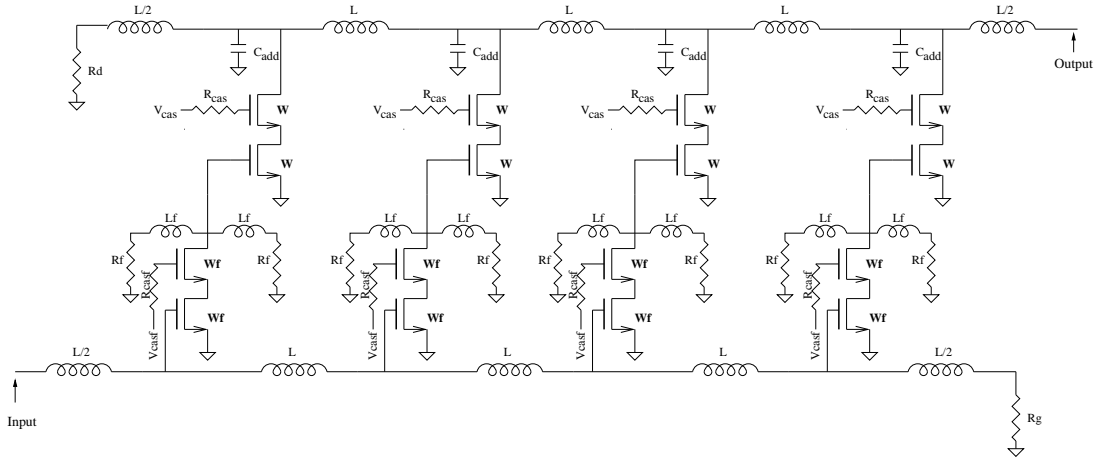


Figure 4.8: Four Stage Distributed Amplifier with Double Stage Cascode

of the first stage which is loaded by the input capacitance of the second stage is given by

$$|A_{vcas1}| = g_{m1}r_{ds1}g_{m2}(|r_{ds2}||\frac{1}{j\omega(C_{gs3} + C_{db2})}|) \quad (4.21)$$

where g_{m1} and r_{ds1} are the transconductance and drain-source shunt resistance of

the main transistor in the first stage. g_{m2} , r_{ds2} and C_{db2} are the transconductance, drain-source shunt resistance and drain-bulk capacitance of the first-stage cascode transistor, respectively. C_{gs3} is the gate-source capacitance of the main transistor of the second stage. As can be inferred from the equation the gain is not constant and decreases with frequency as the impedance due to the capacitors decreases as frequency increases. An intermediate transmission line between the first and second stage provides the required constant gain for the first stage which is given by

$$|A_{vcas1}| = g_{m1}r_{ds1}g_{m2}|Z_{io}| \quad (4.22)$$

where Z_{io} is the characteristic impedance of the intermediate transmission line. The overall gain of the amplifier is given by

$$|A_{vcas}| = g_{m1}r_{ds1}g_{m2}|Z_{io}|g_{m3}r_{ds3}g_{m4}|Z_o| \quad (4.23)$$

where g_{m3} and r_{ds3} are the transconductance and drain-source shunt resistance of the main transistor in the second stage. g_{m4} is the transconductance of the cascode transistor of the second stage.

This topology has three artificial transmission lines, gate, drain and intermediate. This topology has several drawbacks

- The impedance of the artificial transmission line is low. This comes from the fact that the capacitance for the transmission line is the sum of diffusion capacitance for the first stage and the gate capacitance of the second stage. This large capacitance requires a large inductor to have a higher Z_{io} . But this results in a lower cut-off frequency. So, the intermediate transmission line can become the deciding factor for the cut-off frequency. Whereas, a lower Z_{io} for the intermediate transmission means increasing the power to achieve the gain target.
- A higher number of inductors leading to a large die area.

4.4.3 Tapering

Figure 4.9 shows a four stage DA with tapered configuration [13]. [13] proposes a

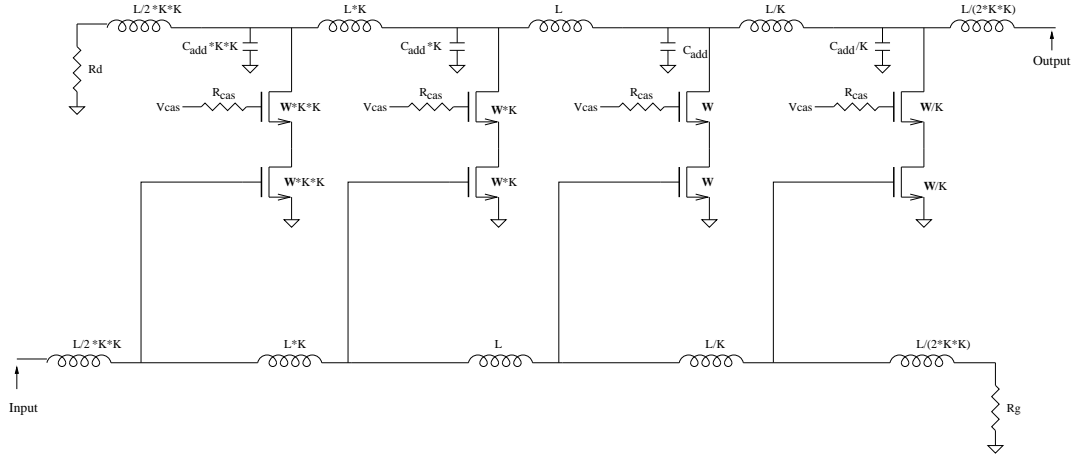


Figure 4.9: Four Stage Distributed Amplifier with Tapering

differential design, however a single ended design is considered for this work. Each stage towards the load are progressively down-sized with a scaling factor K . This causes the transistor parameters (g_m , C_{gs} etc.) of each stage to be K times that of the next stage. The inter-stage inductor of each stage is also scaled down to K times of the next stage. As mentioned in Section 4.4 the attenuation of the gate and drain line effects the bandwidth exponentially and this effect is reduced as the the cut-off frequency of the line increases.

By down-sizing each stage progressively, the cut-off frequency of each stage is increased with respect to the previous stage. This increase in cut-off frequency reduces the affects of attenuation and helps improving the gain-bandwidth product. But with the non-uniform losses of spiral inductors, this topology might not be as efficient as expected.

4.5 Spiral Inductors

Inductors on-chip can be either made as spiral inductors or coplanar wave guide inductors. All the inductors are assumed to be implemented as spiral inductors in

this work. Figure 4.10 shows a spiral inductor model [4] for an inductor between

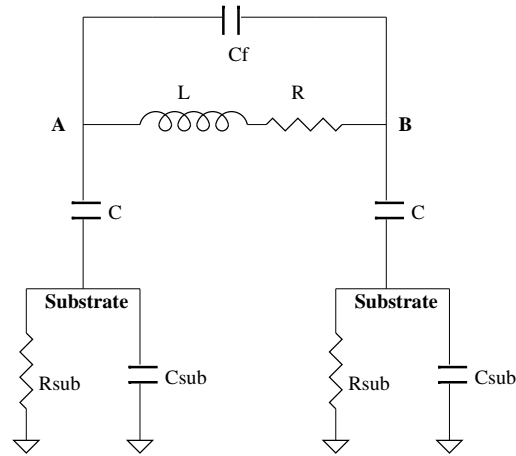


Figure 4.10: Spiral Inductor Model

nodes A and B. L is the inductance, R is the resistive loss, C is the capacitance of the metal to the substrate, R_s and C_s are the equivalent capacitance and resistance of the substrate. Some CMOS processes have low resistive substrates, which causes significant losses in addition to the loss caused by the series resistance R . A technique called patterned ground shield (PGS) [31] helps reduce the effects of the low resistive CMOS substrates. Figure 4.11 shows the model of the spiral inductor with PGS or high resistive substrate. This spiral inductor model is used in all the simulations

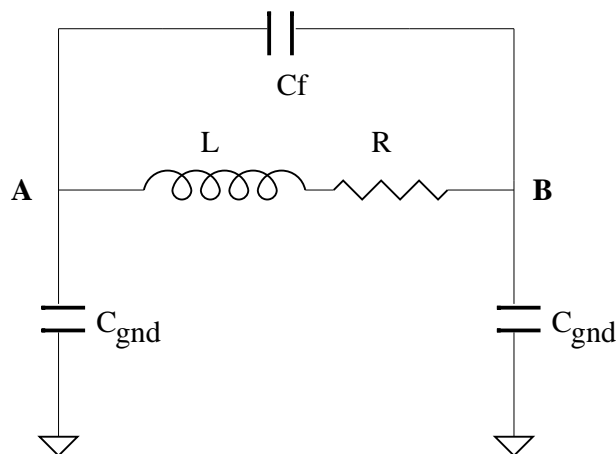


Figure 4.11: Spiral Inductor Model with PGS

reported in this work.

4.6 DA Gain Stage With Spiral Inductors

Figure 4.5d) shows the cascode gain stage with the effective capacitances on the drain and gate lines. Replacing the ideal inductors in Figure 4.5d) by spiral inductor model in Figure 4.11 results in Figure 4.12.

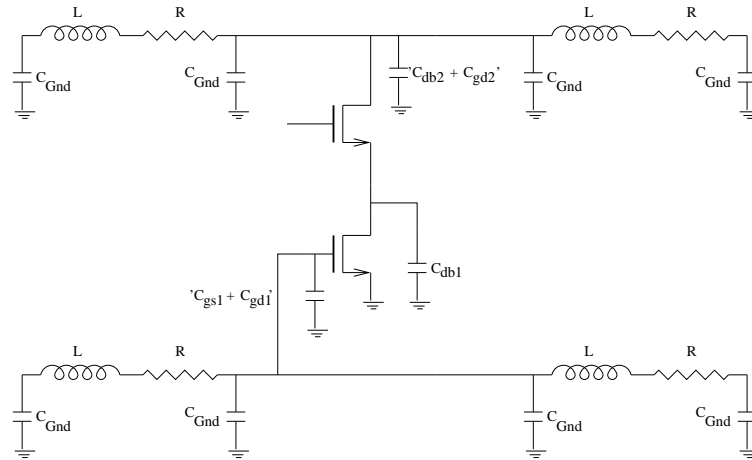


Figure 4.12: Spiral Inductor Model with PGS

Spiral inductors add an additional capacitance C_{Gnd} to both gate and drain lines reducing Z_o and f_c . Hence it is important to include spiral inductor capacitances from the initial phase of design.

Chapter 5

Results

The DA topologies presented in the Chapter 4 are simulated to evaluate the above discussed gain-bandwidth-power tradeoffs. Generic 0.18μ transistor models obtained from MOSIS [32] are used. PGS spiral inductor model is used in the simulations. S21 and S11 are obtained from Hspice [33], whereas Cadence Spectre [34] is used to obtain Noise Figure (NF) and 1dB compression point data. The target design specifications [5, 8, 12] are $|S21| > 10dB$, $|S11| < -10dB$ and $|S22| < -10dB$ over a bandwidth of 10GHz. The results are presented in the following format. Plots for $|S21|$, $|S11|$ and $|S22|$ are obtained from Hspice and are used to compare different designs. Power is calculated from the current consumption ($P_{dc} = I_{dc} * V_{dd}$). Power consumed by the bias circuitry is not included in the calculations and is considered to be minor.

Simulations were done on the following designs

- Single transistor gain stage (Figure 4.1)
- Gain stage with cascode (Figure 4.3)
- Gain stage with source follower (Figure 4.7)
- Gain stage with double cascode (Figure 4.8)
- Gain stage with tapering (Figure 4.9)

Table 5.1: Comparison of Different Implementations with Ideal Inductors

Impl	Gain(dB)	NF(dB)	P_{1dB} (dBm)	P_{dc} (mW)	FOM(dB-Hz/mW)
Simple	10dB	2.3	-0.1	10.8	155.99
Cascode	10dB	2.45	-0.72	4.7	158.83
Source Follower	10dB	4.38	-2.78	7.2	155.35
Double Cascode	10dB	4.6	-9.2	8.33	145.71
Taper	10dB	2	0.34	6.2	159.14

Table 5.1 summarizes the results for the implementations using ideal inductors. NF and 1dB compression point are obtained from Spectre at 5GHz. FOM is calculated for each design to enable better comparison. Table 5.2 summarizes the results for the implementations using spiral inductors.

The primary factor in deciding the transistor sizes is the capacitive loading caused by the transistor on the gate and drain transmission lines. Higher C requires higher L to make Z_o higher. Higher C and L means lower f_c . Transistor sizes can be determined for the targeted f_c and Z_o . f_c is fixed at 10GHz for all the implementations, whereas Z_o and V_{ov} can be varied to meet the required specifications. The capacitive loading caused by spiral inductors also needs to be taken into account while determining the total load on the transmission lines. The implementations presented in this work might not be optimal, but should show the trend in terms of gain, power, linearity, NF etc. Further optimizations might change the absolute values slightly, but might not change the trend in general.

Table 5.3 shows the component values for implementations using ideal inductors. L is the inductance of the transmission line between any two stages. W_1 is the width of first stage NMOS transistor in the gain stage. For the implementations using two stage gain stages (source follower and double cascode), W_2 is the NMOS transistor width of the second stage. V_{ov} is the overdrive voltage, C_{add} is the additional capacitance added to the drain line to match the capacitance on the gate line and Z_o is the characteristic impedance of gate and drain lines. All the values presented

Table 5.2: Comparison of Different Implementations with Spiral Inductors

Impl	Gain(dB)	NF(dB)	P_{1dB} (dBm)	P_{dc} (mW)	FOM(dB-Hz/mW)
Simple	10dB	3	3.24	37.2	153.26
Cascode	10dB	3.15	2.7	12.1	157.44
Source Follower	10dB	4.5	4.3	16.42	156.32
Double Cascode	10dB	6.2	-2.2	25.92	146.18
Taper	10dB	2.5	4.7	24.48	157.03

Table 5.3: Component values of Different Implementations with Ideal Inductors

Impl	L (nH)	W_1 (μm)	W_2 (μm)	V_{ov} (mV)	C_{add} (fF)	Z_o (Ω)
Simple	2.8	50	NA	169	100	140
Cascode	5.6	50	NA	112	100	200
Source Follower	11.2	30	50	60	40	375
Double Cascode	9.8	30	50	157	40	350
Taper	7.2	50	NA	168	100	225

Table 5.4: Component values of Different Implementations with Spiral Inductors

Impl	Inductance				W_1 (μm)	W_2 (μm)	V_{ov} (mV)	C_{add} (fF) (Ω)	Z_o
	L (nH)	R (Ω)	C_{gnd} (fF)	C_{sh} (fF)					
Simple	2.28	10	27	0.85	50	NA	369	100	100
Cascode	3.46	15	30	1.0	50	NA	208	100	125
Source Follower	3.0	9.2	50	1.84	50	100	131	55	110
Double Cascode	3.0	9.2	50	1.84	50	100	206	55	110
Taper	2.75	9.2	45	1.42	100	NA	258	100	85

for the implementation using tapering are for the first gain stage and the subsequent stages are tapered with a factor of $K=1.3$. Table 5.4 shows the component values for implementations using spiral inductors. As shown in the spiral inductor model (Figure 4.11), R is the series resistance, C_{gnd} is the capacitance to ground and C_{sh} is the shunt capacitance.

It can be observed that gain stage with cascode outperforms other designs with

spiral inductors in terms of both power and FOM. It is closely followed by the gain stage using tapering which can be observed to be slightly better than the former with ideal inductors. Although gain stage using tapering consumes twice as much power as the gain stage using cascode. It competes well because of its better linearity (P_{1dB}) which helps its FOM.

It can also be observed from the tables that P_{1dB} of the implementations using spiral inductors is better than the corresponding implementations using ideal inductors. In order to obtain a S21 of 10dB, V_{ov} of the implementations using spiral inductors was chosen to be approximately double the V_{ov} of the corresponding implementations using ideal inductors. As the V_{ov} of the implementations using ideal inductors is chosen to be closer to sub-threshold region, their P_{1dB} is low. The higher V_{ov} required by spiral inductors can be explained from the fact that the spiral inductors come with resistive losses and more V_{ov} is needed to maintain S21 at 10dB.

One more observation that can be made from the results is that the implementations using spiral inductors consume thrice as much power as the corresponding implementations using ideal inductors. This is caused because of two reasons

- Resistive losses of spiral inductors
- Additional capacitive load added to the gate and drain line by the spiral inductors (Figure 4.10). This capacitance decreases the effective Z_o and hence requiring more power to maintain S21 at 10dB

The body and source of the source follower in the above reported simulation are not tied together, hence causing an increase in V_{th} and decrease in gain due to body effect. By connecting the body and source together and adjusting the bias points to maintain S21 at 10dB, power got better by 2.5mW for the design with spiral inductors.

The spiral inductor model (Fig 4.11) used has lumped elements like a single π model. In reality, all the elements of the spiral inductor itself are distributed in

nature. The single π model is replaced by a 3π model for the cascode design. The fluctuations in S21 around 10dB increased along with slight degradation in reflection co-efficients. The total capacitance at the junction of the MOSFET and the spiral inductor ($C_{db} + C_{add} + C_{gnd}/6$) is more than the other parts of the distributed spiral network ($C_{gnd}/3$) causing these mismatches.

Figure 5.1, 5.2, 5.3 and 5.4 show the S21, S11, S22 and NF plots for various implementations using ideal inductors. Figure 5.5, 5.6, 5.7 and 5.8 show the S21, S11, S22 and NF plots for various implementations using spiral inductors.

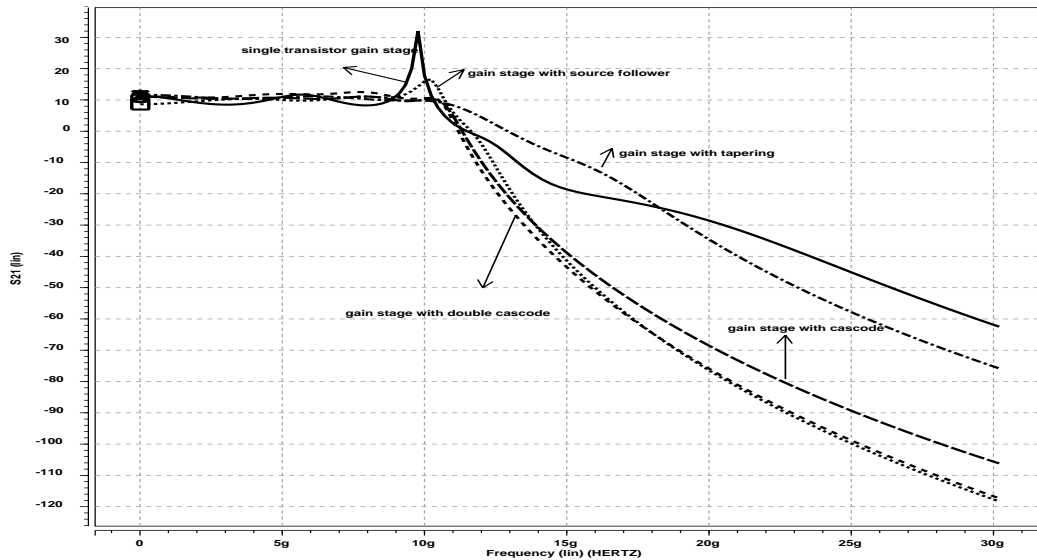


Figure 5.1: S21 of Various Implementations Using Ideal Inductors

As can be observed from the above results, the gain stage with cascode outperforms other implementations. Figures 5.9, 5.10, 5.11, 5.12 compare S21, S11, S22 and NF respectively for the cascode implementation using ideal and spiral inductors. NF with spiral inductors is approximately 1dB greater than the one with ideal inductors. This can be attributed to the noise added by the resistors in the spiral inductors.

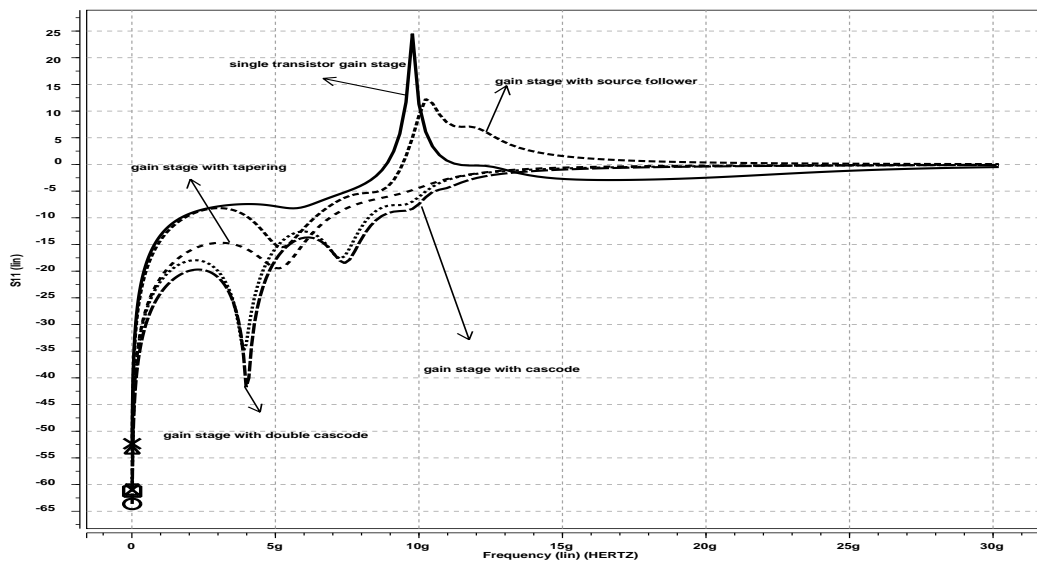


Figure 5.2: S11 of Various Implementations Using Ideal Inductors

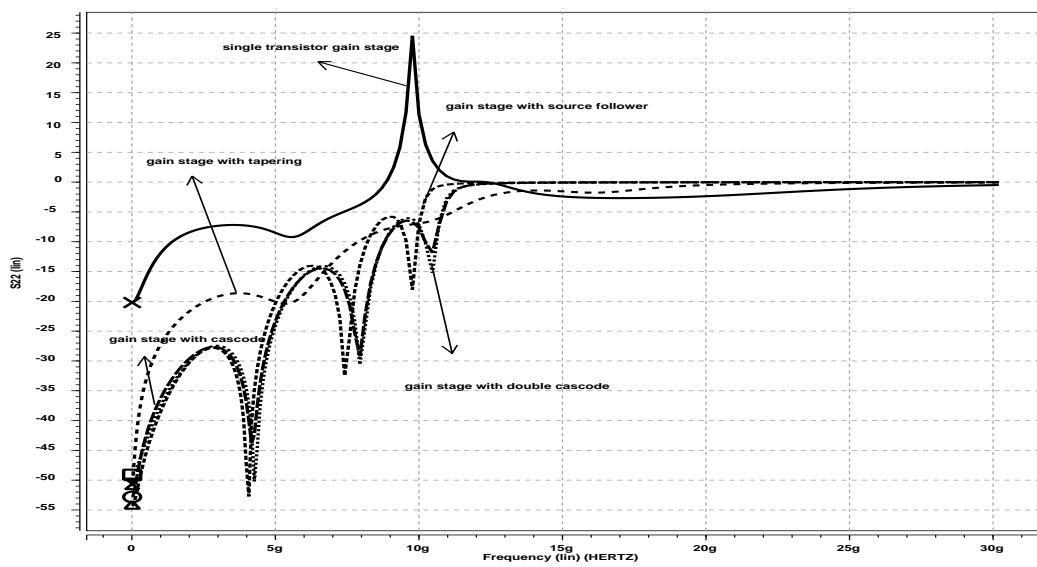


Figure 5.3: S22 of Various Implementations Using Ideal Inductors

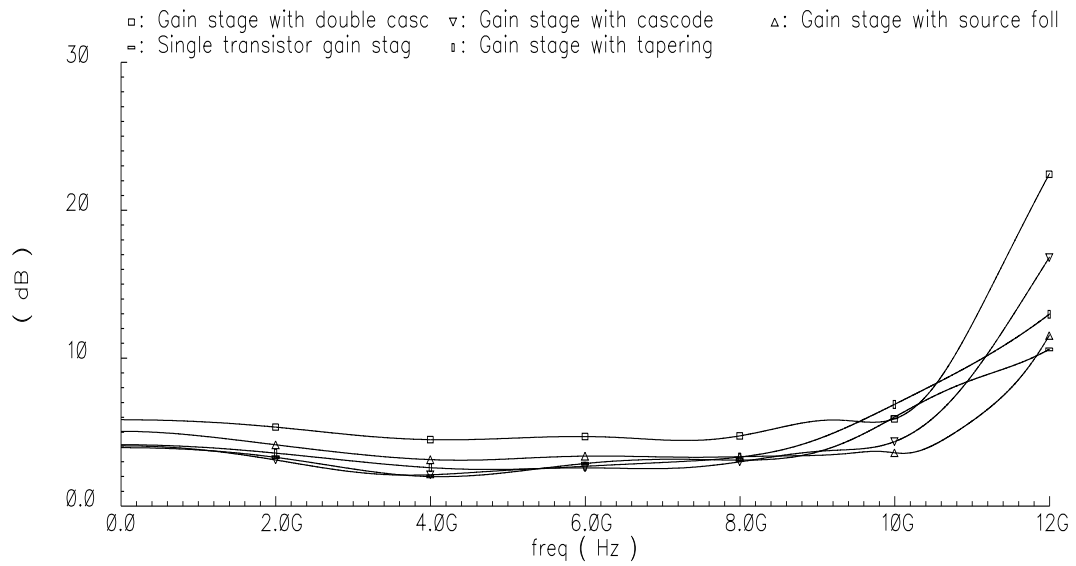


Figure 5.4: NF of Various Implementations Using Ideal Inductors

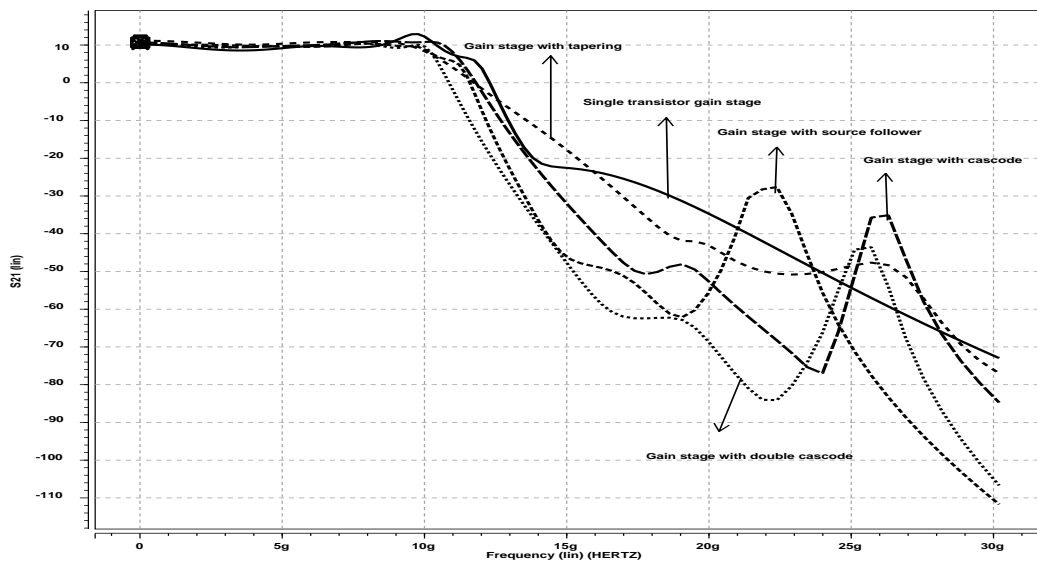


Figure 5.5: S21 of Various Implementations Using Spiral Inductors

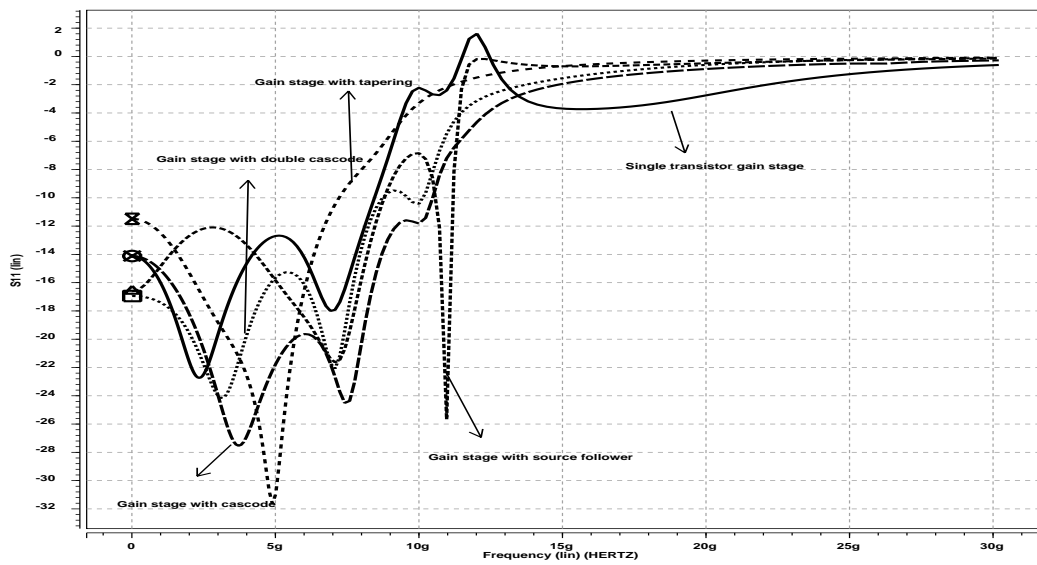


Figure 5.6: S_{11} of Various Implementations Using Spiral Inductors

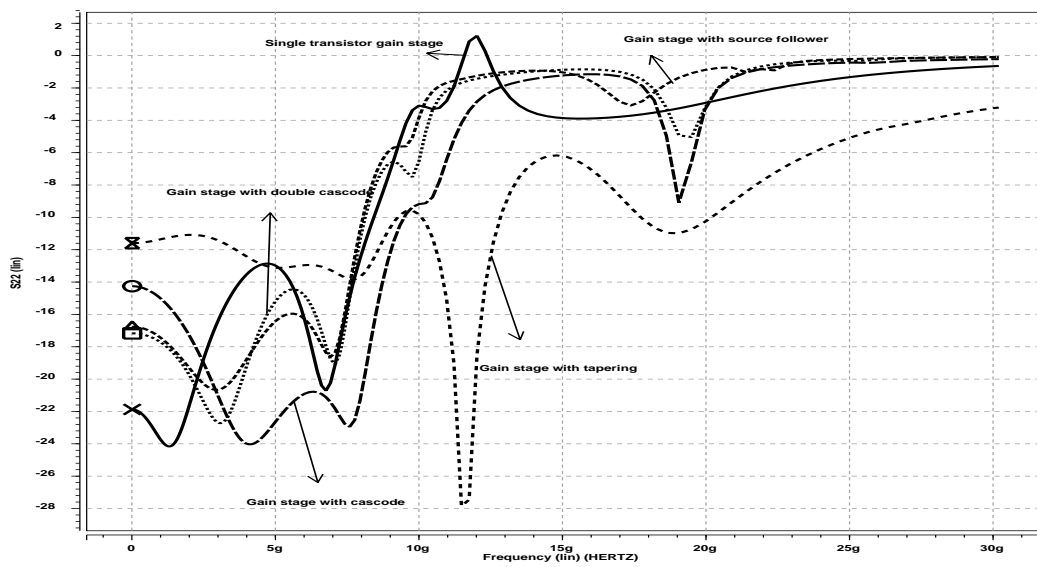


Figure 5.7: S_{22} of Various Implementations Using Spiral Inductors

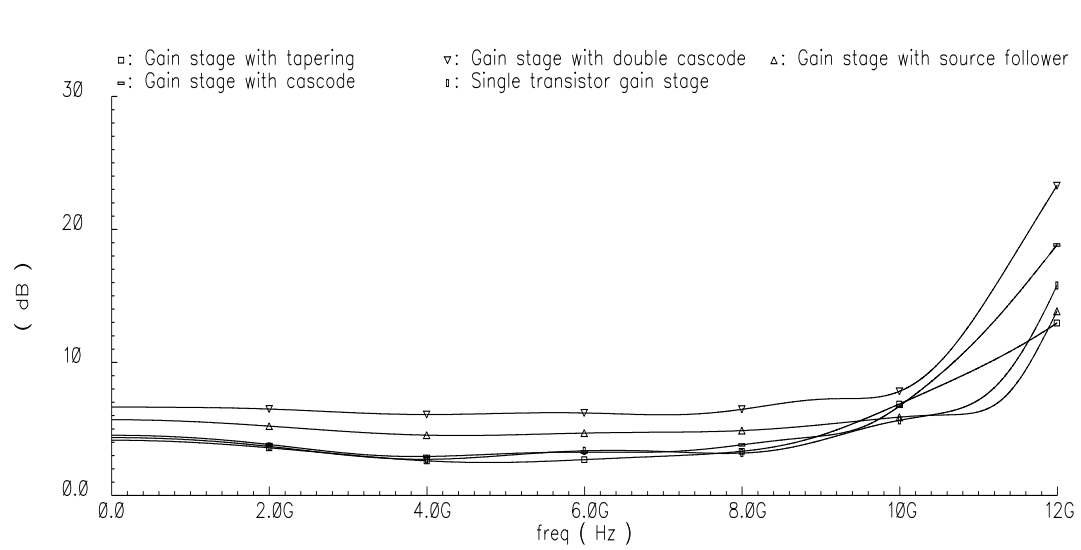


Figure 5.8: NF of Various Implementations Using Spiral Inductors

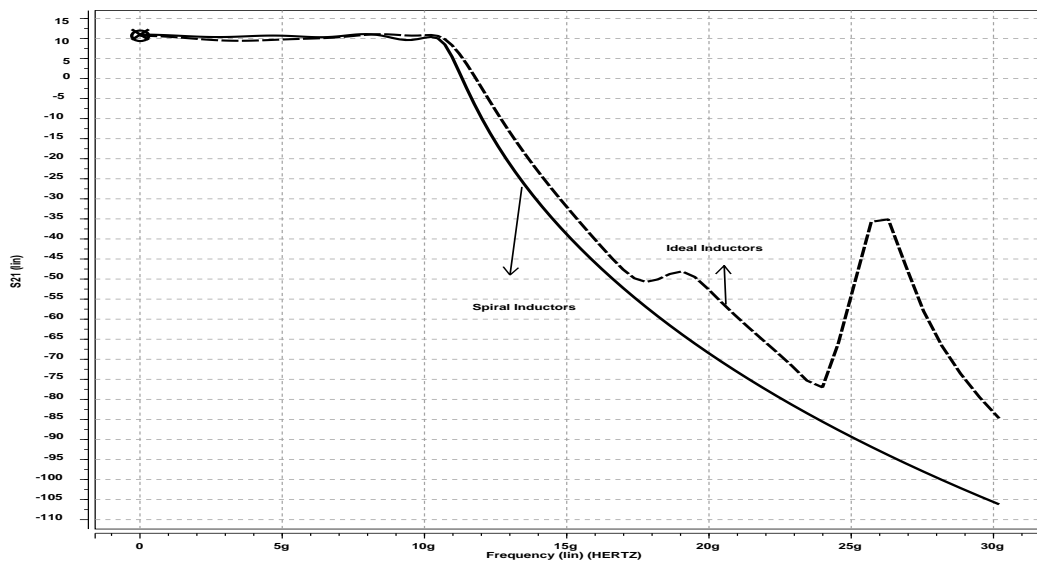


Figure 5.9: S21 of Cascode Implementation With Ideal and Spiral Inductors

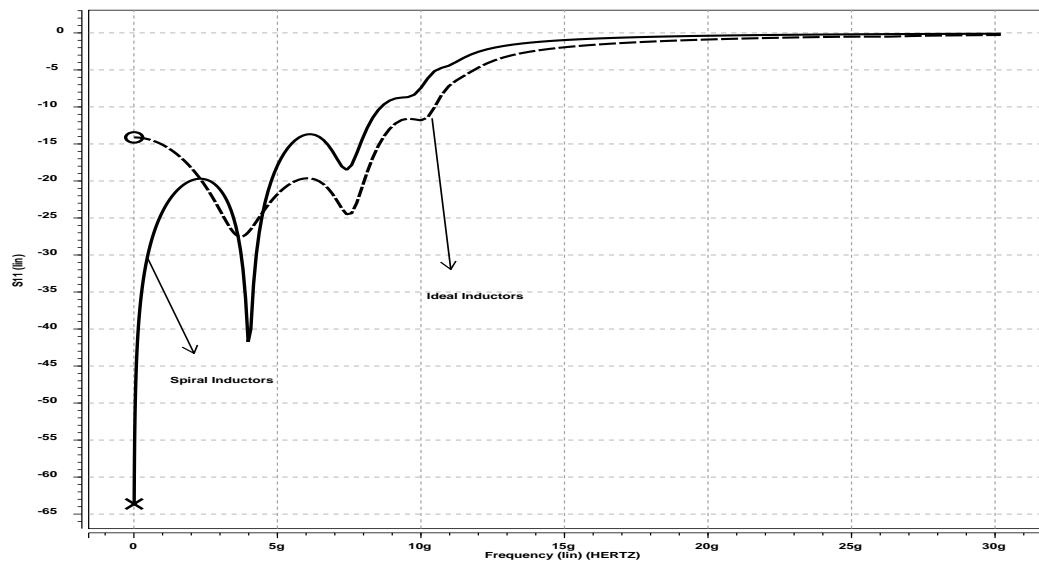


Figure 5.10: S_{11} of Cascode Implementation With Ideal and Spiral Inductors

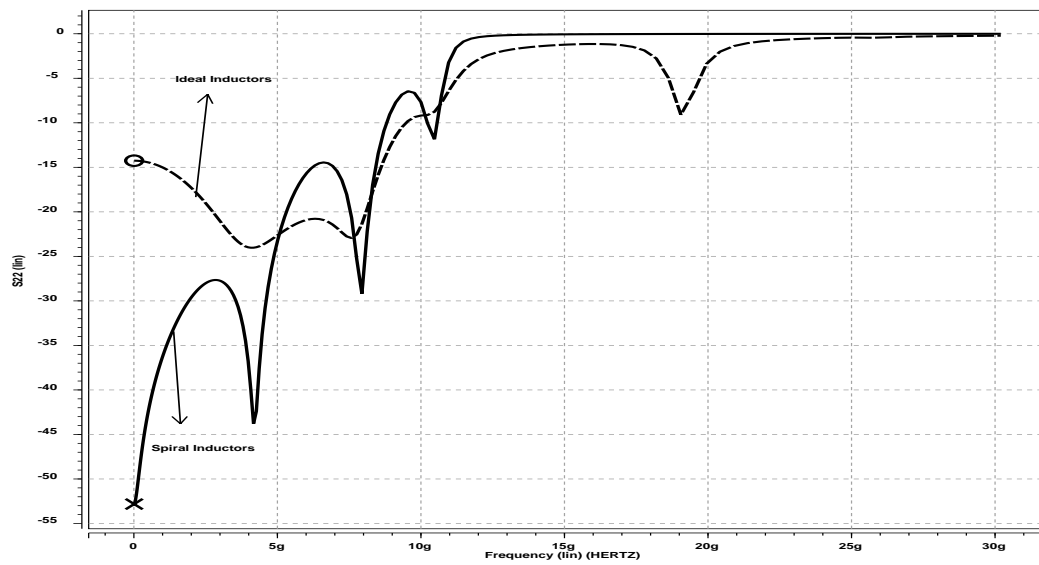


Figure 5.11: S_{22} of Cascode Implementation With Ideal and Spiral Inductors

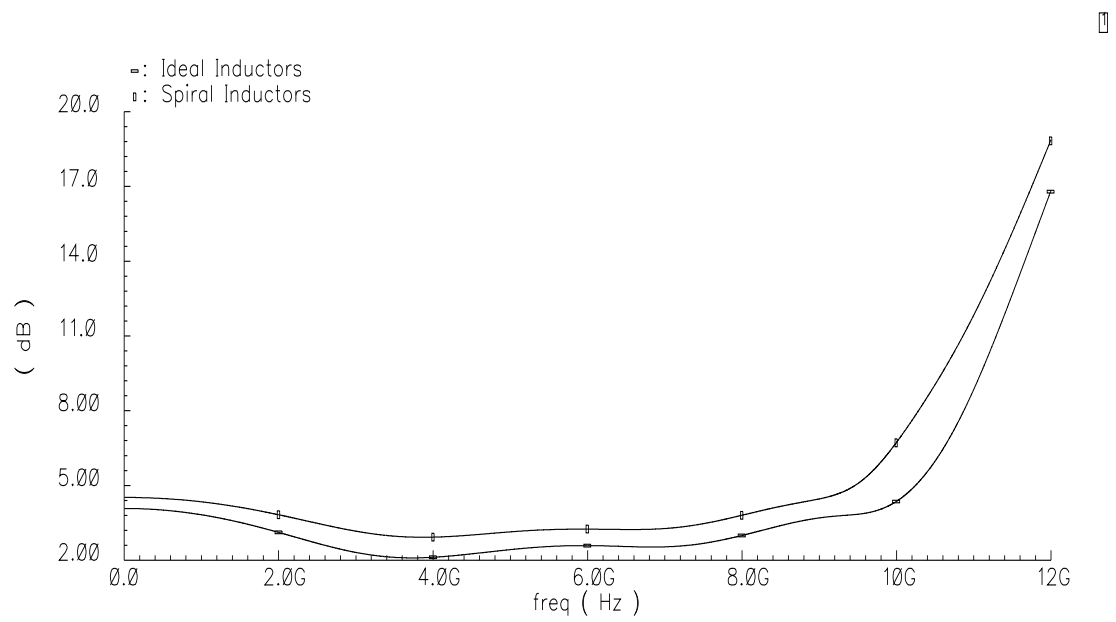


Figure 5.12: NF of Cascode Implementation With Ideal and Spiral Inductors

Chapter 6

Conclusions and Future Work

6.1 Conclusions

This work surveys existing CMOS LNA designs for wide-band systems. A new FOM involving NF, linearity, DC power consumption and a technology bandwidth utilization factor is introduced. Existing wide-band LNA designs are compared using the proposed FOM. The obtained survey results based on this FOM suggest that distributed amplification outperforms approaches that utilize wide-band matching networks or noise cancellation techniques.

Power consumption in DAs can be reduced by using a Z_o higher than the conventional 50Ω . Different DA architectures are simulated to evaluate the gain-bandwidth-power trade-offs. Gain stage using cascode is found to be the best of different implementations presented in this work. The cascode gain stage is closely followed by gain stage with tapering and the one with source follower. The simulations presented in this work show that it is possible to achieve a S21 of 10dB with P_{dc} of only 12mW.

6.2 Future Work

The DA implementations presented in this work are simulated with generic transistor and analytical spiral inductor models. The next step would be to fabricate these proposed designs and verify the results presented in this work.

Appendix A

Distributed Amplifier Gain

This appendix presents a theoretical analysis of the CMOS DA gain. Due to the similarity in the small-signal models of GaAs MESFETS and CMOS FETS, most of the analysis presented here is obtained from [28, 29, 30]. A distributed amplifier is made of constant-k [30] filter sections to form a low pass filter. The theory of image impedance can be used to simplify the mathematical analysis of the DA. Hence it is important to understand the theory of image impedance and propagation functions of the networks used to build a DA.

A.1 General Networks

Figure A.1 a) shows a 2-port network terminated with its image impedances Z_{I1} and Z_{I2} . When the network is image impedance matched, Z_{I1} is the impedance looking into port 1 when port 2 is terminated with Z_{I2} and vice-versa. The propagation function of the network is defined as $\gamma = A + \Phi$, where A is the attenuation and Φ is the phase shift or phase velocity.

The propagation function of a 2-port network is given by [28]. When a voltage source is inserted in series with Z_{I1} . The ratio of the voltages V_1 and V_2 at the two ports is given by the equation A.1, which simplifies to equation A.2 for the case of

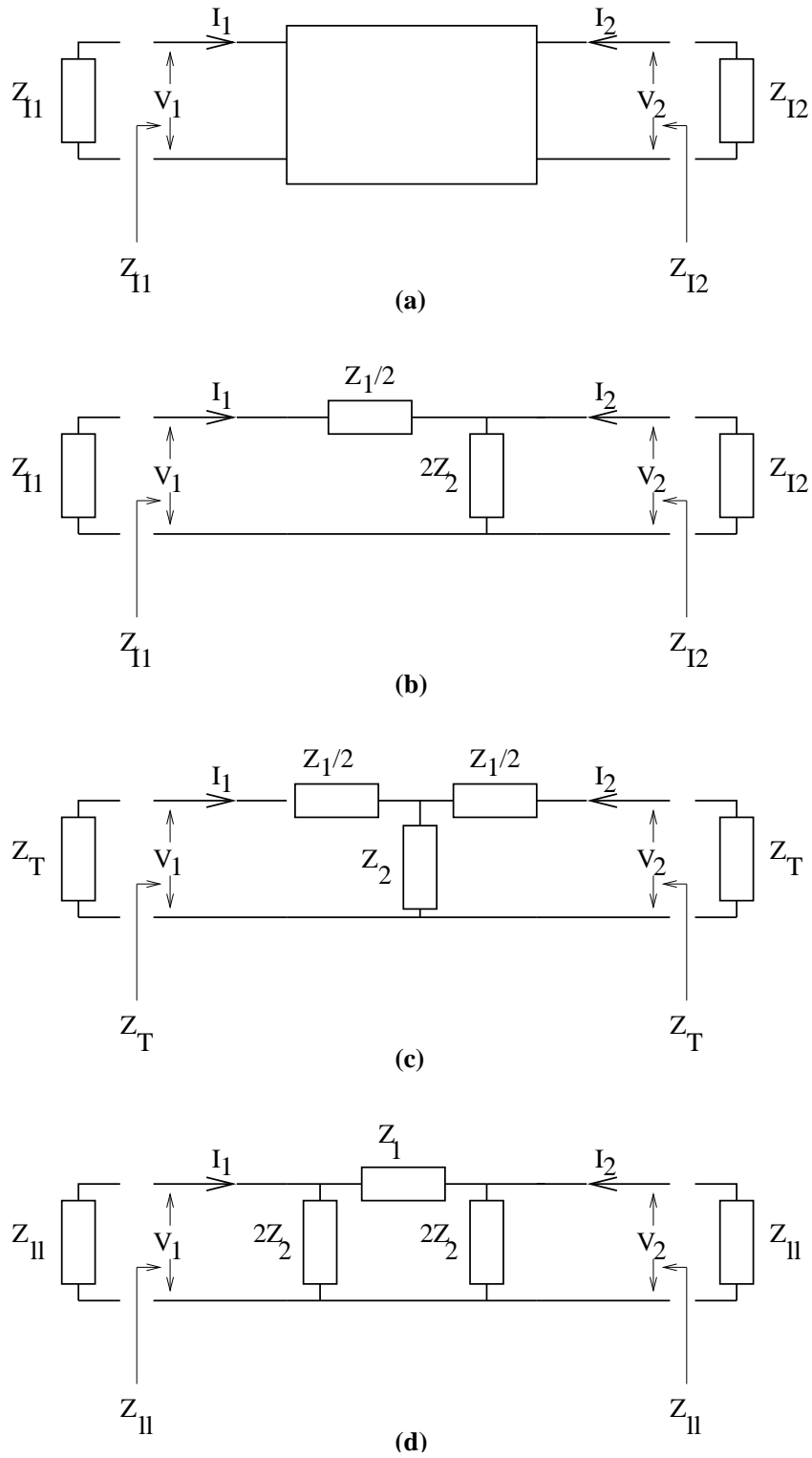


Figure A.1: a) Two Port Network with Terminations b) Half Section c) T Section d) π Section

symmetrical network.

$$\frac{V_2}{V_1} = e^{-\gamma} \sqrt{\frac{Z_{I2}}{Z_{I1}}} \quad (\text{A.1})$$

$$\frac{V_2}{V_1} = e^{-\gamma} \quad (\text{A.2})$$

For symmetrical networks ($Z_{I1} = Z_{I2} = Z_I$) the image impedance is given as

$$Z_I = \sqrt{Z_{sc}Z_{oc}} \quad (\text{A.3})$$

where Z_{sc} and Z_{oc} are the impedances looking into a port when the other port is short-circuited and open-circuited respectively. The propagation function is given by

$$\gamma = \tanh^{-1} \sqrt{\frac{Z_{sc}}{Z_{oc}}} \quad (\text{A.4})$$

A.2 Half Section

A half section is the basic building block of both T and π sections to be discussed later. Hence it is useful to understand the properties of a half section. Figure A.1b) shows the schematic of a half section. The propagation constant of the half section is given by

$$\gamma_H = \tanh^{-1} \sqrt{\frac{Z_{sc1}}{Z_{oc1}}} = \tanh^{-1} \sqrt{\frac{Z_{sc2}}{Z_{oc2}}} \quad (\text{A.5})$$

where the short-circuit and open-circuit impedances of the 2 ports Z_{sc1} , Z_{sc2} , Z_{oc1} , Z_{oc2} are given by

$$Z_{sc1} = \frac{Z_1}{2} \quad (\text{A.6})$$

$$Z_{oc1} = \frac{Z_1}{2} + 2Z_2 \quad (\text{A.7})$$

$$Z_{sc2} = \frac{1}{\frac{1}{2Z_2} + \frac{2}{Z_1}} \quad (\text{A.8})$$

$$Z_{oc2} = 2Z_2 \quad (\text{A.9})$$

The image impedances can be derived as

$$Z_{I1} = \sqrt{Z_1 Z_2 \left(1 + \frac{Z_1}{4Z_2}\right)} \quad (\text{A.10})$$

$$Z_{I2} = \sqrt{\frac{Z_1 Z_2}{1 + \frac{Z_1}{4Z_2}}} \quad (\text{A.11})$$

With some simplification it can be shown that

$$\gamma_H = \frac{1}{2} \cosh^{-1} \left(1 + \frac{Z_1}{2Z_2}\right) \quad (\text{A.12})$$

and the voltage transfer function can be defined as

$$\frac{V_2}{V_1} = \frac{e^{-\gamma_H}}{\sqrt{1 + \frac{Z_1}{4Z_2}}} \quad (\text{A.13})$$

for the converse case, where the generator is inserted in series with port 2, the voltage transfer function can be given by

$$\frac{V_1}{V_2} = e^{-\gamma_H} \sqrt{1 + \frac{Z_1}{4Z_2}} \quad (\text{A.14})$$

A.12, A.13, A.14 are the fundamental equations used to derive the gain of a DA.

A.3 T and π Sections

Both T and π Sections can be formed by cascading two half sections back to back. The schematic of a T section is shown in the Figure A.1 c). The T-section is symmetrical and the image impedance is given by A.10. The voltage transfer ratio of a T-section can be obtained by the product of A.13, A.14 and is given by

$$\frac{V_2}{V_1} = e^{-2\gamma_H} \quad (\text{A.15})$$

The π section is also symmetrical and the image impedance is given by A.11. The voltage transfer ratio of a π -section can be obtained by the product of A.13, A.14 and is given by

$$\frac{V_2}{V_1} = e^{-2\gamma_H} \quad (\text{A.16})$$

It is interesting to note that the voltage transfer functions of both T and π sections are the same.

A.4 Gain of Distributed Amplifier

Figure A.2 shows both the gate and drain artificial transmission lines broken down into cascaded π and half-sections with image impedance matched terminations. The shunt arms $2Z_2^g$ of the gate line are formed by splitting the effective shunt impedance on the gate line into two identical parallel impedances each having twice the impedance of the original shunt impedance. The drain line is similarly constructed except for the fact that gate line coupled transconductances are inserted between each π section. Each of the π and half sections are image impedance matched in both the gate and drain lines. Both ends of drain and gate lines are image impedance matched with the terminations $Z_{IN}^g, Z_T^g, Z_T^d, Z_L^d$. If V_N^d is the voltage across the N^{th} MOSFET, the output voltage V_{out} is given by

$$V_{out} = V_N^d \sqrt{1 + \frac{Z_1^d}{4Z_2^d} e^{-\frac{\gamma_d}{2}}} \quad (\text{A.17})$$

where $\gamma_d = A_d + j\Phi_d$ is the π section propagation function. A_d and Φ_d are the drain line attenuation and phase velocity per section. Z_1^d and Z_2^d are the drain series and shunt arm impedances. One can obtain V_N^d by summing up the contributions

from each MOSFET, yielding

$$V_N^d = \frac{Z_\pi^d}{2} \sum_{k=1}^N I_k^d e^{-(N-k)\gamma_d} \quad (\text{A.18})$$

where Z_π is the image impedance of the π section given by

$$Z_\pi^d = \sqrt{\frac{Z_1^d Z_2^d}{1 + \frac{Z_1^d}{4Z_2^d}}} \quad (\text{A.19})$$

N is the total number of MOSFETS and $I_k^d = g_{mk} V_k^g$ is the current produced by each MOSFET because of its internal transconductance (g_{mk}). V_k^g is the gate-source voltage of the k^{th} MOSFET and can be expressed as

$$V_k^g = V_1^g e^{-(k-1)\gamma_g} \quad (\text{A.20})$$

where $\gamma_g = A_g + j\Phi_g$ is the π section propagation function. A_g and Φ_g are the gate line attenuation and phase velocity per section. V_1^g is the voltage across the first MOSFET and is given by

$$V_1^g = \frac{V_{IN} e^{-\frac{\gamma_g}{2}}}{\sqrt{1 + \frac{Z_1^g}{4Z_2^g}}} \quad (\text{A.21})$$

where V_{IN} is the input voltage, Z_1^g and Z_2^g are the gate series and shunt arm impedances.

From equations A.17, A.18, A.20, A.21 the overall gain can be obtained as

$$Gain = \left| \frac{V_{out}}{V_{IN}} \right| = \frac{Z_\pi^d}{2} \sum_{k=1}^N g_{mk} e^{-\{[2(N-k)+1]\frac{\gamma_d}{2} + (2k-1)\frac{\gamma_g}{2}\}} \quad (\text{A.22})$$

which can be simplified to

$$Gain = g_m \frac{Z_\pi^d}{2} \frac{e^{-N\frac{(\gamma_g+\gamma_d)}{2}} \sinh\left[N\frac{(\gamma_d-\gamma_g)}{2}\right]}{\sinh\left[\frac{(\gamma_d-\gamma_g)}{2}\right]} \quad (\text{A.23})$$

The phase shift per section or the propagation velocity of the gate and drain lines

can be made the same by making the cut-off frequencies of both the lines equal. In order to make the cut-off frequencies equal, Z_1^g and Z_2^g should be made equal to Z_1^d and Z_2^d respectively. This simplifies the propagation functions within A.23 to $\gamma_g + \gamma_d = A_g + A_d + j2\Phi$ and $\gamma_g - \gamma_d = A_g - A_d$. Equation A.23 can be further simplified to

$$Gain = \frac{g_m}{2} \sqrt{\frac{Z_1^d Z_2^d}{1 + \frac{Z_1^d}{4Z_2^d}}} \frac{e^{-N \frac{(A_g + A_d)}{2}} \sinh\left[N \frac{(A_d - A_g)}{2}\right]}{\sinh\left[\frac{(A_d - A_g)}{2}\right]} \quad (\text{A.24})$$

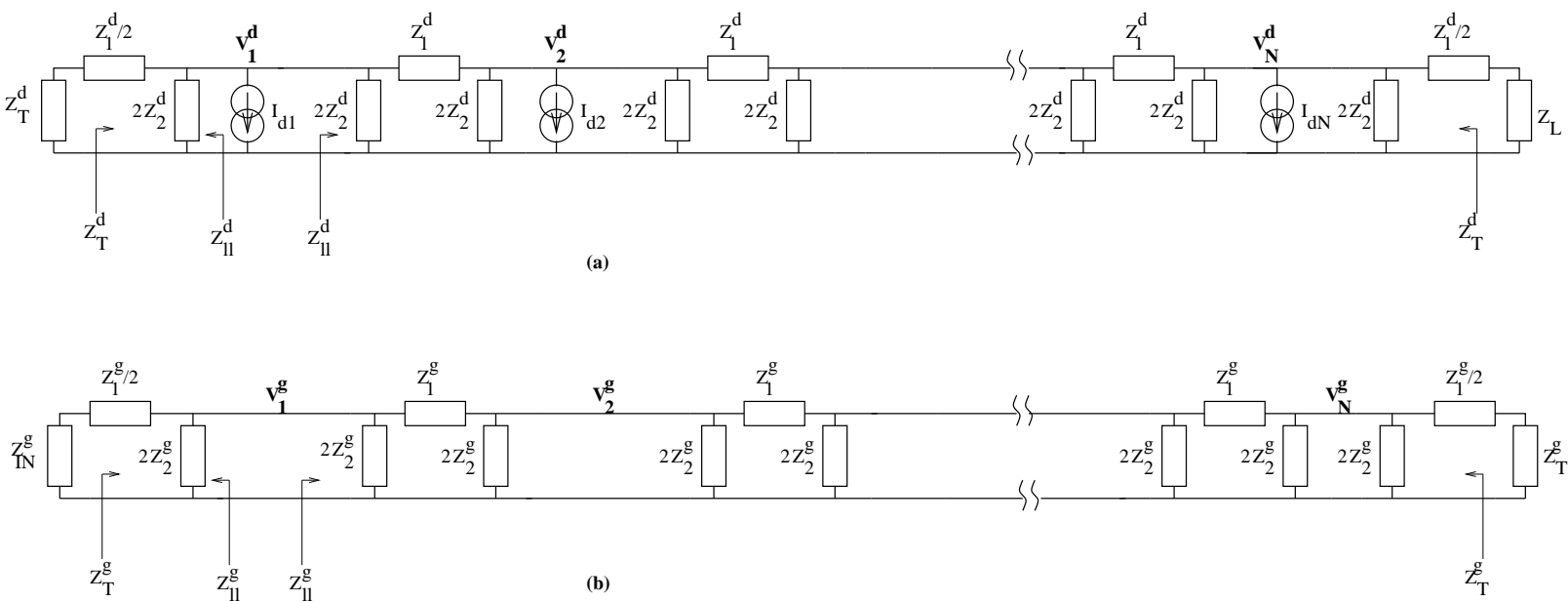


Figure A.2: a) Drain Line b) Gate Line

Appendix B

Simulation Models

B.1 NMOS Model

*T3AZ SPICE BSIM3 VERSION 3.1 PARAMETERS

*SPICE 3f5 Level 8, Star-HSPICE Level 49, UTMOST Level 8

* DATE: Dec 11/03

* LOT: T3AZ WAF: 2002

* Temperature_parameters=Default

```
.MODEL CMOSN NMOS ( LEVEL = 49
+VERSION = 3.1 TNOM = 27 TOX = 4.1E-9
+XJ = 1E-7 NCH = 2.3549E17 VTH0 = 0.3760617
+K1 = 0.5943076 K2 = 1.67355E-3 K3 = 1E-3
+K3B = 3.682806 W0 = 1E-7 NLX = 1.767881E-7
+DVTOW = 0 DVT1W = 0 DVT2W = 0
+DVTO = 1.2316239 DVT1 = 0.3512305 DVT2 = 0.063951
+U0 = 263.9980419 UA = -1.394217E-9 UB = 2.297709E-18
+UC = 5.130071E-11 VSAT = 1.029403E5 A0 = 1.8766173
+AGS = 0.4102712 B0 = -2.37567E-9 B1 = -1E-7
+KETA = -4.974094E-3 A1 = 4.008889E-5 A2 = 0.8813901
```

+RDSW	= 105	PRWG	= 0.5	PRWB	= -0.2
+WR	= 1	WINT	= 0	LINT	= 1.344769E-8
+XL	= 0	XW	= -1E-8	DWG	= -1.143937E-8
+DWB	= 9.970084E-9	VOFF	= -0.0929211	NFACTOR	= 2.2595064
+CIT	= 0	CDSC	= 2.4E-4	CDSCD	= 0
+CDSCB	= 0	ETA0	= 3.074988E-3	ETAB	= 6.426614E-5
+DSUB	= 0.0125687	PCLM	= 0.7841044	PDIBLC1	= 0.1991955
+PDIBLC2	= 1.733639E-3	PDIBLCB	= -0.1	DROUT	= 0.7514474
+PSCBE1	= 2.556879E9	PSCBE2	= 4.835696E-9	PVAG	= 0.0194376
+DELTA	= 0.01	RSH	= 6.7	MOBMOD	= 1
+PRT	= 0	UTE	= -1.5	KT1	= -0.11
+KT1L	= 0	KT2	= 0.022	UA1	= 4.31E-9
+UB1	= -7.61E-18	UC1	= -5.6E-11	AT	= 3.3E4
+WL	= 0	WLN	= 1	WW	= 0
+WWN	= 1	WWL	= 0	LL	= 0
+LLN	= 1	LW	= 0	LWN	= 1
+LWL	= 0	CAPMOD	= 2	XPART	= 0.5
+CGD0	= 7.91E-10	CGS0	= 7.91E-10	CGB0	= 1E-12
+CJ	= 9.844556E-4	PB	= 0.8	MJ	= 0.3815244
+CJSW	= 2.398346E-10	PBSW	= 0.8	MJSW	= 0.1086216
+CJSWG	= 3.3E-10	PBSWG	= 0.8	MJSWG	= 0.1086216
+CF	= 0	PVTH0	= -1.728579E-4	PRDSW	= -3.5480489
+PK2	= 6.801178E-4	WKETA	= 3.767259E-3	LKETA	= -0.010533
+PU0	= 29.3769437	PUA	= 1.243843E-10	PUB	= 1.106551E-24
+PVSAT	= 1.561162E3	PETA0	= 1.003159E-4	PKETA	= -4.59777E-3)

B.2 Spiral Inductor

```

** On-chip spiral inductor

.subckt spind a b shield n=4 davg=100u rho=0.5

.param _u0='1.257e-6'
.param _sigma='3.5e7'
.param _omega='6.3e9'
.param _s='2u'
.param _t='1.2u'
.param _tox='3.5u'
.param _eox='3.97*8.854e-12'
.param _delta='sqrt(2/(_omega*_u0*_sigma))'
.param _l='4*n*davg'
.param _w='(davg*rho-(n-1)*_s)/n'
.param _c1='1.27'
.param _c2='2.07'
.param _c3='0.18'
.param _c4='0.13'

Cp  a b 'n*_w*_w*_eox/(1*_tox)'
Ls  a 1 '_u0*n*n*davg*_c1/2*(log(_c2/rho)+_c3*rho+_c4*rho*rho)'
Rs  1 b '_l/(1*_w*_sigma*_delta*(1-exp(-t/_delta)))'
C1  a shield '_w*_l*_eox/(2*_tox)'
C2  b shield '_w*_l*_eox/(2*_tox)'

.ends

```

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