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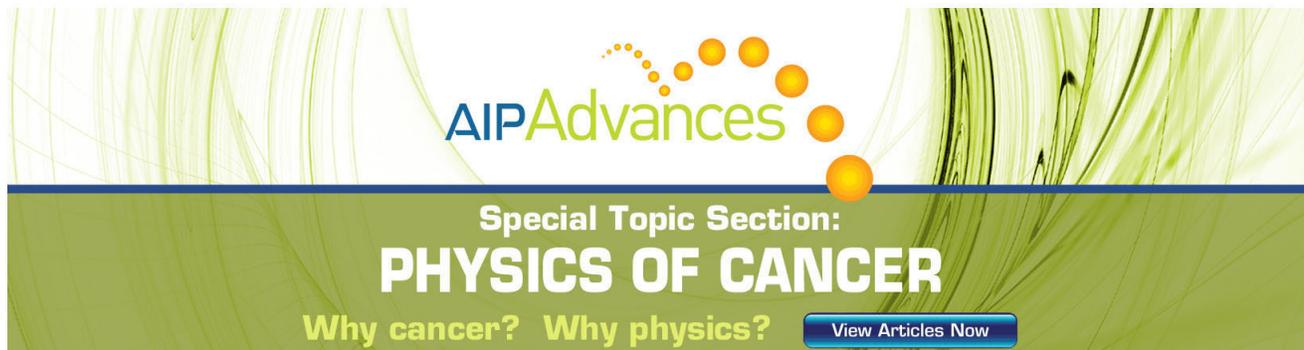
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Electrical properties of GaAs photonic crystal cavity lateral p-i-n diodes

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We investigate conduction and free-carrier injection in laterally doped GaAs p-i-n diodes formed in one and two-dimensional photonic crystal (PC) nanocavities. Finite element simulations show that the lateral geometry exhibits high conductivity for a wide range of PC parameters and allows for precise control over current flow, enabling efficient carrier injection despite fast surface recombination. Thermal simulations indicate that the temperature increase during steady-state operation is only 3.3 K in nanobeams and 0.29 K in L3 defect nanocavities. The results affirm the suitability of lateral doping in PC devices and indicate criteria for further design optimization.

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The strong light-matter interaction in photonic crystal (PC) nanocavities makes them a promising platform for efficient and compact optical devices. The high quality (Q) factors and small mode volumes demonstrated in such cavities lead to large Purcell factors, lowering laser thresholds and increasing the achievable modulation rate.^{1–3} These properties have been exploited to make high-speed and low-energy lasers,^{4–8} chemical and mechanical sensors,^{9,10} strongly coupled quantum dot cavity systems,¹¹ and optomechanical crystals.¹²

The majority of these devices, however, rely on optical excitation and control. Electrical injection using a vertical p-i-n structure has been demonstrated, but relies on complex fabrication and limits the cavity Q.¹³ Recently, we have demonstrated a number of GaAs PC nanocavity sources and modulators with a lateral p-i-n geometry,^{14–17} fabricated using an electron beam lithography and masked ion implantation process¹⁴ which is versatile and readily adapted to work in new materials. In this letter, we model the electrical properties of laterally doped GaAs 1D (“nanobeam”) and 2D (“L3” defect) PC nanocavity devices. We find that the electrical characteristics of the devices are relatively insensitive to the PC design parameters, and that selective-area doping allows the devices to efficiently inject free carriers into the active region despite fast surface recombination in the PC mirrors. Finally, self-heating in the devices is modeled and found to be minimal under normal operating conditions. These results pave the way for further efficiency improvements in low-power electrical control of PC nanocavity devices.

Figure 1(a) displays the geometry and doping profiles for the lateral p-i-n 1D “nanobeam” PC design. The beam dimensions are $9.66 \mu\text{m} \times 600 \text{ nm} \times 220 \text{ nm}$ $l \times w \times h$, making room for ten PC periods on each side of a five-hole taper defect¹⁸ (lattice parameter $a_1 = 322 \text{ nm}$ to $a_2 = 266 \text{ nm}$); hole radii follow $r = 0.23 \times a$. Uniform doping on either side of the cavity center leaves an intrinsic region length of 400 nm; “control” devices with $5 \mu\text{m}$ intrinsic lengths were also considered. The structure of the 2D PC (L3) devices is shown in Figure 1(b). The membrane has dimensions $5.91 \mu\text{m} \times 8.37 \mu\text{m} \times 220 \text{ nm}$ $l \times w \times h$, and contains a triangular lattice structure with a three-hole linear defect.¹⁹

A 400 nm long intrinsic region is aligned with the cavity to avoid lattice damage-induced Q degradation. Starting two PC periods from the edges of the defect, the intrinsic region is expanded to a maximum width of $5 \mu\text{m}$ to limit leakage current through the mirror regions. “Control” membranes did not include the trapezoidal doping regions and maintained a constant $5 \mu\text{m}$ intrinsic length. Dopant densities for both structures are set to experimentally realized values¹⁴ of $N_D = 6 \times 10^{17} \text{ cm}^{-3}$ and $N_A = 2.5 \times 10^{19} \text{ cm}^{-3}$, with a background impurity density of $N_{A,\text{intrinsic}} = 10^{15} \text{ cm}^{-3}$. Only the suspended GaAs device layer was modeled; simulated electrical contacts were placed where the undercut structure came into contact with the sacrificial AlGaAs layer and GaAs substrate present in previously reported devices.^{14–17}

We performed numerical simulations of the Poisson and carrier drift-diffusion equations in the devices using the Sentaurus software suite. Nanobeam structures were modeled in three dimensions while the much larger L3 nanocavity membranes were simulated in two dimensions due to software limitations on device complexity. Only the areas of the devices shown in Figure 1 were analyzed; additional effects due to non-ideal electrical contacts and current leakage paths not confined to the suspended structure were not considered. The structural deformations and InAs quantum dot layers present in previously reported devices were not modeled. Dopant densities were assumed to be uniform both vertically and in-plane

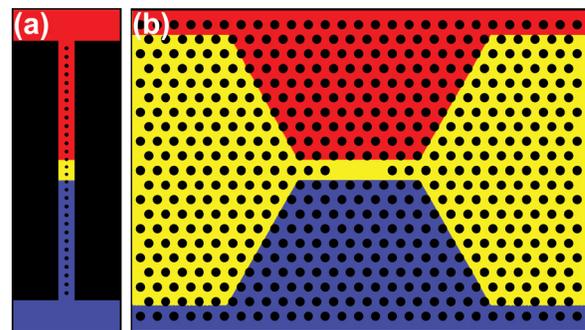


FIG. 1. Top-down schematic view of nanobeam (a) and L3 (b) nanocavity devices. Colors indicate n-type (red), p-type (blue), and intrinsic (yellow) regions.

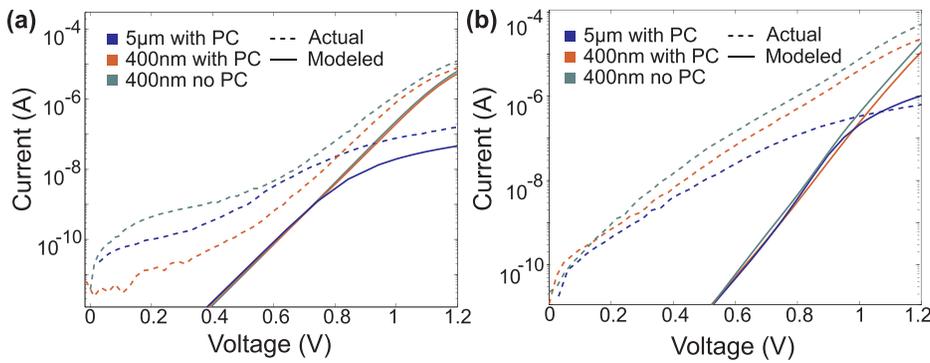


FIG. 2. Modeled nanobeam (a) and L3 (b) current-voltage characteristics for devices with $5\mu\text{m}$ and 400nm intrinsic regions, with and without PC holes. Experimentally measured curves (dashed; Refs. 15 and 17) are shown for comparison with model (solid lines).

within the doped regions and complete dopant ionization was assumed. Bandgap narrowing was implemented with the Slotboom model.²⁰ Carrier mobilities were modeled after Arora²¹ and Caughey-Thomas²² with parameters chosen to match measured values (Ref. 14) for both carrier types in their respective doping regions ($\mu_e = 1930\text{ cm}^2/\text{Vs}$, $\mu_h = 126\text{ cm}^2/\text{Vs}$).

GaAs exhibits a high surface recombination velocity at air interfaces, possibly further exacerbated by increased roughness from dry-etch processing.^{23,24} Two levels of surface states are responsible for this phenomenon and were introduced into the simulation: acceptor states at 0.7 eV and donor states at 0.35 eV above the valence band.²⁵ Trap state densities were determined from surface recombination velocities (S) reported²³ in similar structures via $S = \sigma v_{th} N_{trap}$, where $\sigma = 10^{-15}\text{ cm}^2$ is the trap cross-section, v_{th} is the thermal velocity, and N_{trap} is the surface trap density. The resulting value $N_{trap} = 5 \times 10^{13}\text{ cm}^{-2}$ agrees well with published GaAs surface state densities.²⁶ Bulk nonradiative recombination in the devices was modeled with a Shockley Read Hall term using the measured $\sim 100\text{ ps}$ bulk lifetime for both carrier types.¹⁶ Due to the very fast ($\sim 6\text{ ps}$) nonradiative recombination rate measured in the PC regions of these devices,¹⁶ radiative recombination was deemed negligible in determining overall carrier dynamics.

We performed self-heating simulations of the studied devices by using the Sentaurus suite to solve the hydrodynamic (energy-balance) carrier transport equations. Both Joule heating and recombination/generation energies were accounted for. Thermal contacts at 300 K were placed at the borders of the simulated device areas, corresponding to the points of contact between the suspended structures and the bulk of the substrate. Bulk values were used for the thermal conductivity, and any effects due to thermionic emission were neglected.

Current-voltage curves for simulated nanobeam and L3 structures are plotted in Figures 2(a) and 2(b). Previous experimental results are included for comparison,^{15,17} as are simulated and experimental results for devices without etched PC holes and control devices with $5\mu\text{m}$ intrinsic regions. There is reasonable agreement between simulated and experimental results; experimental values are slightly higher due to differences between the modeled and the fabricated devices. At low voltages in particular, the experimental results are dominated by leakage currents through substrate layers which were not included in the simulations.¹⁴ As expected, “control” devices with wider intrinsic regions exhibit increased series resistance and decreased current; at

higher voltages, the series resistance dominates conduction through these devices, reducing currents by almost two orders in nanobeam devices. Interestingly, the presence of PC holes has a minimal impact on the IV characteristics of the devices; the reduction in cross-sectional surface area caused by the etching of holes is balanced by an increase in recombination current across the junction.

The steady-state carrier densities at the central plane of nanobeam devices under 1.2 V bias are presented in Figures 3(a) and 3(b). Injected minority carrier densities up to $4 \times 10^{15}\text{ cm}^{-3}$ can be seen within the cavity defect, limited primarily by fast trap-assisted recombination at nearby surfaces. Fermi pinning causes an accumulation of holes and slight depletion of electrons near GaAs-air interfaces in the N-doped portion of the device. Due to the differing spatial distributions of majority hole and electron populations, the resulting injected carrier distributions are non-uniform along vertical cross-sectional planes. Figures 3(c) and 3(d) map the electron and hole carrier densities on a cross-sectional plane in the I-region near the N-I junction, where this phenomenon is the most pronounced. Figure 3(e) displays the electron and hole densities at the central device plane and 10 nm below the top surface, both measured 100 nm from the beam central axis; Fermi pinning is observable both at the etched PC holes and near the top device plane. The current density at the central plane is depicted in Figure 3(f). Current flow follows regions of high carrier density, with current densities reaching as high as 10 kA/cm^2 in the beam sidewalls. We find short carrier diffusion lengths of only 200 nm for electrons and 40 nm for holes. As a result, recombination accounts for 95% of current across the p-i-n junction, with only 5% of injected carriers diffusing completely across the junction. Steady-state device temperatures due to self-heating appear in Figure 3(g). Heating in the device is dominated by carrier recombination in the cavity region, resulting in a symmetric temperature distribution. Maximum temperature increase approaching 3.3 K appears near the cavity region. The cavity peak wavelength λ is expected to shift as $\delta\lambda/\lambda = \delta n/n$ with changes δn to the nominal refractive index n . Near $\lambda = 1.3\mu\text{m}$, the thermal dependence of the refractive index of GaAs ($n = 3.5$) is given by $\delta n = 2.7 \times 10^{-4}\text{ K}^{-1} \times \Delta T$.²⁷ Thus, the expected $\delta\lambda$ for the structure is only 330 pm .

Figures 4(a) and 4(b) map the steady-state carrier densities for L3 devices under 1.2 V bias. Fermi pinning is again observed in the N-doped and also the intrinsic region. The 2D PC p-i-n structure supports injection levels of

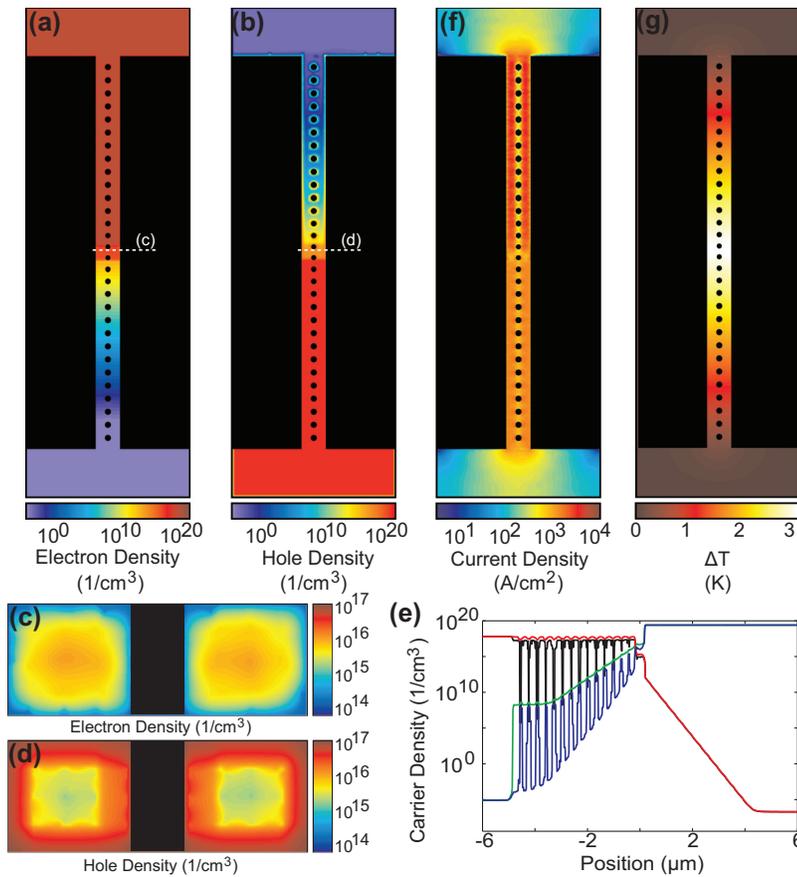


FIG. 3. Nanobeam device properties under steady-state 1.2 V bias. (a) Electron and (b) hole carrier density maps at the central plane. (c) Electron and (d) hole carrier density maps taken on a cross-sectional plane in the I-region 100 nm from the N-I junction. The black portion corresponds to the cross-section of the PC hole at that position. (e) Electron (red, black) and hole (blue, green) carrier densities along the length of the device, 100 nm from the device axis, measured in the central device plane and 10 nm below the device surface, respectively. (f) Current density map at the central device plane. (g) Change in temperature ΔT at the central plane, relative to 300 K ambient. Maximum ΔT is 3.3 K.

$2 \times 10^{16} \text{ cm}^{-3}$ near the center of the cavity region, showing good agreement with previously estimated levels.¹⁶ The increase in injection densities over those in the nanobeam structure can be explained by the reduced recombination current due to the absent PC holes. Because of this reduction, recombination accounts for only 90% of current across the p-i-n junction; 10% is due to carrier

diffusion. The steady-state current density under 1.2 V bias is shown for membrane devices in Figure 4(c). Leakage through the PC mirror edges is minimized by the tapered doping design; 64% of the current is channeled through the center third of the device, within three PC lattice periods of the defect. Interestingly, the regions of highest current density do not correspond to the region

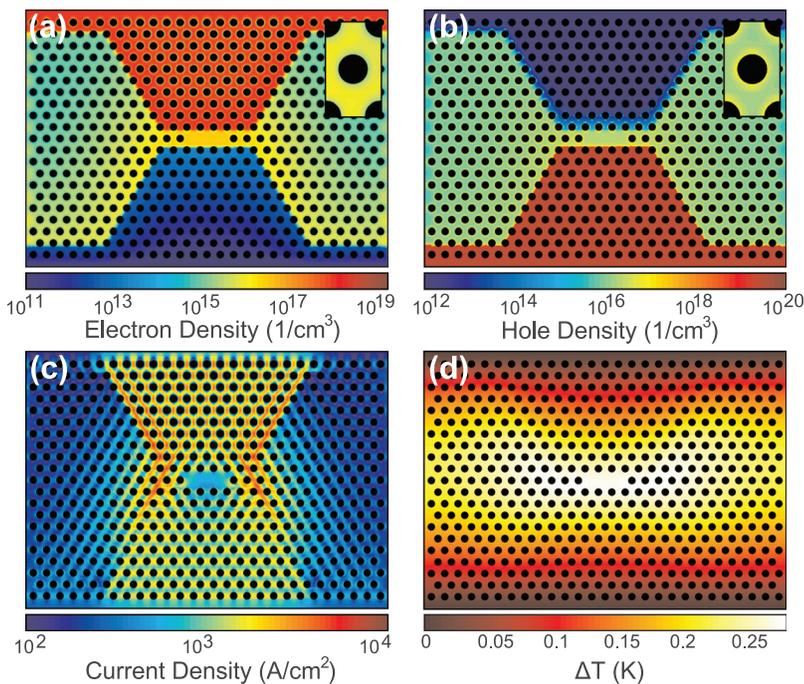


FIG. 4. (a) Electron and (b) hole steady-state carrier densities in L3 devices under 1.2 V bias. Insets enlarge the third hole from the cavity edge, showing electron depletion and hole accumulation due to Fermi pinning. (c) Current density at steady-state in an L3 device under 1.2 V bias. (d) Steady-state change in temperature ΔT under 1.2 V bias and 300 K ambient temperature. Maximum ΔT is 0.29 K.

with highest carrier density; two high-current paths form just outside of the cavity defect due to a current crowding effect caused by the tapering of the doping regions. Peak current densities occur between the second and third photonic crystal holes outside the defect region. Despite this, for operating currents of 1–10 μA , the injected carrier densities at the cavity center still show a linear dependence on the total device current. Steady-state device temperatures due to self-heating appear in Figure 4(d), reaching 0.29 K at maximum and corresponding to a wavelength shift $\delta\lambda$ of only 29 pm.

Injected carrier densities in both devices are limited primarily by the rapid surface recombination. Even a tenfold increase in dopant concentrations ($N_D = 6 \times 10^{18} \text{ cm}^{-3}$, $N_A = 2.5 \times 10^{20} \text{ cm}^{-3}$) results in only a twofold increase in injection levels. Reduction of the surface trap density by a factor of ten (e.g., through surface passivation) increases injected carrier densities by a factor of ~ 4 at 1.2 V; however, the L3 devices become significantly less resistive above 1.2 V, causing achievable injection levels at 1.5 V to rise from $8 \times 10^{16} \text{ cm}^{-3}$ ($N_{\text{trap}} = 5 \times 10^{13} \text{ cm}^{-2}$) to $2 \times 10^{18} \text{ cm}^{-3}$ ($N_{\text{trap}} = 5 \times 10^{12} \text{ cm}^{-2}$).¹⁴

Due to the high current densities supported by the doped regions, the addition of etched PC holes does not substantially affect the IV characteristics of the device; current-voltage curves for L3 cavity devices with varying hole sizes are presented in Figure 5(a). The IV curves remain mostly unaffected for hole radii up to $r = 0.4 \times a$, at which point the device is operating with an 80% reduced cross-section in directions perpendicular to the PC lattice vectors. Figure 5(b) presents series resistance values inferred from simulation IV characteristics and normalized to the $r = 0$ case. The resistance values are compared to the expected resistance of a PC membrane, calculated under the assumption of uniform resistivity. For $r \leq 0.3 \times a$, the simulated devices exhibit series resistances below approxi-

mately 3 k Ω , in agreement with experimentally measured values¹⁴ and sufficiently small to not significantly affect device IV characteristics near the operating voltage of 1.2 V.

Although the doping design for the L3 device already directs nearly two-thirds of the total current into the cavity, further improvements can be made by reducing the width of the doping region near the cavity defect, as presented in Figure 5(c). Up to a 45% increase in injected carrier density is obtained under constant bias current conditions, as shown in Figure 5(d). Reduced current leakage through the PC mirrors is also observed as 71% of the device current passes through the active region. Further reductions in the doping region width could be useful in designs using single-point-defect cavities; narrowing the trapezoidal regions and lengthening the 5 μm portion of the intrinsic region can increase the current through the active region to 98% of the total. However, doing so also reduces the current-crowding effect and thereby reduces the maximum injected carrier densities to values comparable to those in a similarly sized nanobeam device ($6 \times 10^{15} \text{ cm}^{-3}$).

In summary, we have modeled the electrical properties of laterally doped GaAs p-i-n diodes formed in photonic crystal nanocavities. These results extend our prior experimental work with these structures and indicate avenues for future improvements. The devices exhibit minimal self-heating and have robust electrical performance over a wide range of PC designs. In 2D PC membranes, lithographic definition of doping can be used to minimize leakage currents through the PC mirror regions and optimize carrier injection. Future designs should focus on slowing non-radiative recombination to raise injection levels and improve device efficiency. Electrical control of PC nanocavity devices as modeled in this paper is an important step towards creating compact highly integrated, low-power laser sources, modulators, and sensors.

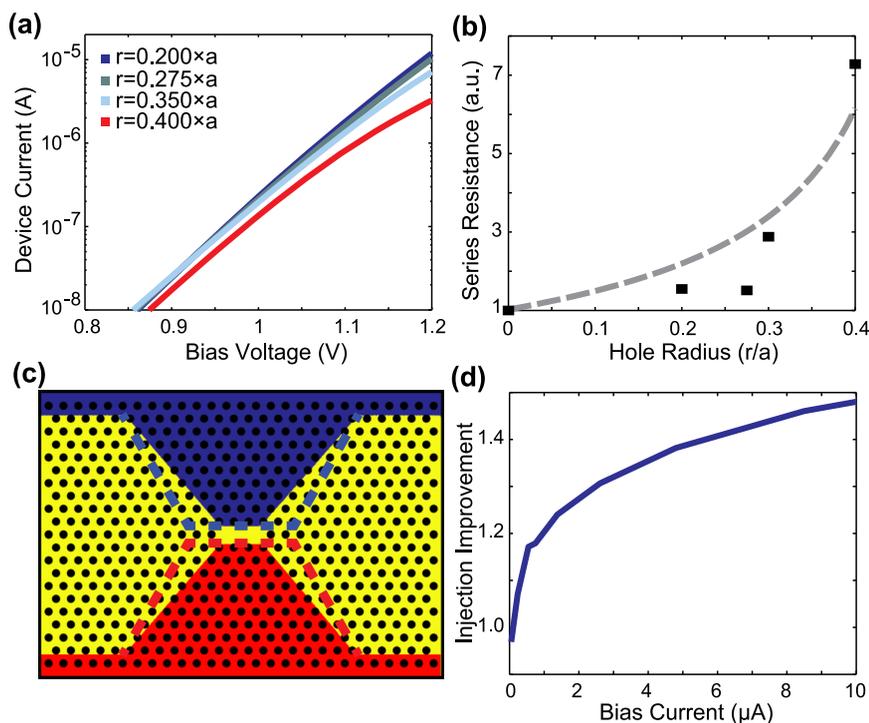


FIG. 5. (a) L3 device current-voltage characteristics for devices with PC hole sizes ranging from to $r = 0.2 \times a$ to $r = 0.4 \times a$, where r is the hole radius and a is the lattice parameter. Note that $r = 0.4 \times a$ corresponds to hole diameters equal to 80% of the hole center-to-center distance. (b) Series resistance plotted against hole radius. Dashed line indicates expected series resistance due to removal of GaAs. (c) Doping region design for increased carrier injection. Dashed lines indicate the original design. (d) Increase in hole injection densities compared to the original doping layout, calculated by taking the quotient of the injected densities in the new and the original designs, plotted against device bias current.

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