Technical Report (part of this work was submitted to DAC 2009) – updated 2/14/2009

Carbon Nanotube Circuits in the Presence of Carbon Nanotube Density Variations

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Abstract

Carbon Nanotubes (CNTs) are grown using chemical self-assembly. As a result, it is extremely difficult to ensure exact positioning and uniform density of CNTs. Density variations in CNT growth can compromise reliability of Carbon Nanotube Field Effect Transistor (CNFET) circuits, and result in increased delay variations. A parameterized model for CNT density variation is presented based on experimental data extracted from aligned CNT growth. This model is used to quantify the impact of such variations on design metrics such as noise margins and delay variations of CNFET circuits. Finally, we analyze correlation that exists in aligned CNT growth, and demonstrate how the reliability of CNFET circuits can be significantly improved by taking advantage of such correlation.

Keywords

Carbon Nanotube, CNT, CNT Density Variation, CNT Correlation.

1. Introduction

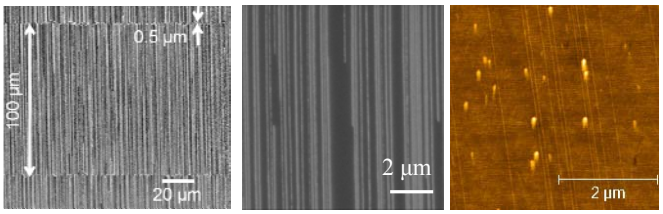
Carbon Nanotube Field Effect Transistors (CNFETs) show promise as extensions to Silicon CMOS. Ideal CNFET circuits show 13X better Energy-Delay Product (EDP) advantage over 32 nm Silicon CMOS [Deng 07a]. This analysis assumes that the CNFETs consist of multiple aligned semiconducting Carbon Nanotubes (CNTs) with a uniform density of 250 CNTs/μm [Deng 07a]. However, current CNT synthesis processes are far from being perfect:

1. A third of the CNTs are grown as metallic [Kang 07], creating source-drain shorts in the CNFETs causing excessive leakage and reduced noise margins in CNFET circuits. Hence, metallic CNTs (m-CNTs) must be removed [Zhang 06, Collins 01]. However, current m-CNT removal techniques are not perfect as they do not remove all m-CNTs and also inadvertently remove some s-CNTs.
2. Although CNT growth on quartz yields a large fraction (> 99%) of aligned CNTs [Kang 07, Patil 08a], there exists a non-negligible fraction of misaligned and mis-positioned CNTs which may cause incorrect logic functionality [Patil 08b]. Layout design principles described in [Patil 08b] can enable CNFET circuits immune to such misaligned and mis-positioned CNTs.
3. The average density of CNTs obtained today is 10-50 CNTs/μm [Kocabas 07]. Advances in CNT synthesis are essential to improve this average density from this value to the required density of 250 CNTs/μm. However, mere increase in average CNT density is not enough. Large variations are present in the CNT density. CNFETs fabricated using these CNTs not only have large variation in their performance but also have a significant probability of complete failure in the case when there is no CNT present in the CNFET, since the locations of the CNTs cannot be determined during layout design. The presence and removal of m-CNTs introduce additional variations resulting in increased performance (delay) variations and also increased probability of failure.

In this paper, we characterize CNT density variations using Scanning Electron Microscopy (SEM) and Atomic Force Microscopy (AFM) images (e.g., Fig. 1.1) of aligned CNTs grown on quartz. The impact of these variations on CNFET circuits is analyzed. Since the CNTs are aligned over long distances (>100 μm), correlation exists between CNFETs at different locations. We show that such correlations in CNTs can be effectively utilized to design CNFET circuits with significantly improved noise margin characteristics and reduced delay variations.

The key contributions of this paper are:

1) Characterization of CNT density distributions from SEM and AFM images of aligned CNT growth samples.
2) A parameterized model based on renewal theory [Cox 62] for CNT density variations fitted to experimental data.
3) Quantitative analysis of the impact of non-uniform CNT density distribution, together with m-CNT growth, and m-CNT removal, on circuit performance metrics such as noise margin and delay variations.
4) Special layout design guidelines for CNFET-based circuits in the presence of CNT density variations by utilizing CNT density correlation.



(a) (b) (c)

Figure 1.1. (a) SEM image of aligned CNTs on quartz with catalyst stripes of size 0.5 μm. SEM (b) and AFM (c) images of aligned CNTs between catalyst stripes.

2. Characterization and Modeling of CNT Density Variations

In order to characterize CNT density variations, we analyzed SEM and AFM images (Fig. 1.1) of aligned CNTs grown on single crystal quartz wafers. Aligned CNTs were grown on single-crystal quartz wafers using Fe nanoparticles as the catalyst patterned at predefined stripes using lithography as shown in Fig. 1.1a [Kang 07, Patil 08a]. In this paper, we focus on the CNTs between catalyst stripes. We performed image processing on such SEM and AFM images (e.g. Fig. 1.1b and 1.1c) to extract the locations of ~1,500 CNTs. Further, a parameterized analytical model is derived and fitted to the experimentally extracted CNT density distribution. We assume that the CNT density distribution does not vary across the CNT sample.

2.1. CNT Count and Spacing Distribution

We can represent a CNFET as a box with width W and length L[1] with CNTs aligned along the L direction (Fig. 2.1a). *CNT count* is defined as the number of CNTs that completely bridge the upper and the lower sides of the box (and is, hence, equal to the number of CNTs that connect source and drain contacts in the corresponding CNFET). We denote CNT count by *N(W, L)* since it is a function of width (W) and length (L). *N(W, L)* is a random variable that depends on the location of this box.

To simplify the analysis, we consider the 1-D limit of the function *N (W, L)* as L approaches 0:

$$N(W) = \lim_{L \to 0} N(W, L) \qquad (2.1)$$

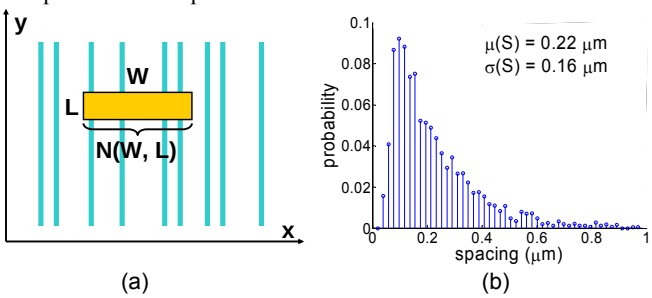
Such simplification is acceptable because, for relatively aligned CNT growth and small channel-length[2] (Length(CNT) >> L) CNFETs, the difference between the number of CNTs passing through the upper side of the box and the number of CNTs passing through the lower side of the box is negligible.

[1] The length (L) of the box is equal to sum of CNT channel length and the lengths of the source and drain doped CNTs regions.

[2] Aligned CNT growth processes produce CNTs with lengths > 100 μm [Kang 07].

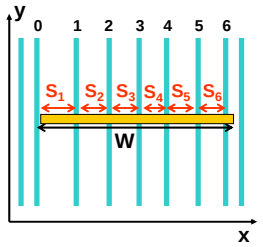
CNT spacing, denoted by *S*, is defined as the distance between neighboring CNTs measured perpendicular to the direction of *L* as *L* approaches 0. Figure 2.1b shows the CNT spacing distribution extracted from SEM images of CNTs (e.g., Fig. 1.1) by considering all possible pairs of CNTs in the images.

We number the CNTs in the box from 1 through *N*. The CNT immediately outside the box to the left is numbered 0. Let S_j (j = 1, 2, 3…) be the spacing random variables from the $(j-1)^{th}$ CNT to the j^{th} CNT (Fig. 2.2). Figure 2.2 shows the correlation coefficients (ρ) between pairs of these CNT spacings extracted from the images. Chi-squared independence test [Ross 05] on the pairs of CNT spacing (Fig 2.2) shows that hypothesis that the CNT spacing is independent is accepted.



(a) (b)

Figure 2.1. (a) CNT count model. (b) CNT spacing distribution.



	correlation coefficient	p-value of χ^2 test
S1, S2	0.0517	0.93
S1, S3	-0.0025	0.90
S1, S4	-0.0408	0.60
S1, S5	0.0054	0.79
S1, S6	-0.0033	0.91

Figure 2.2. Correlation Coefficient and χ^2 independence test results for CNT spacing.

2.2. Derivation of CNT Count Distribution from Spacing Distribution

The distribution of CNT count, *N(W)*, is important for characterizing the statistical performance of CNFETs because it decides the drive current of a CNFET. However, extracting the distribution of *N(W)* experimentally can be time-consuming since this distribution can be dependent on *W*. Spacing distribution, on the other hand, is width independent and easy to extract experimentally. Renewal theory [Cox 62, Cameron 98] can be applied to derive CNT count distribution from CNT spacing distribution.

Based on the results from Sec. 2.1, we assume that CNT spacing, S_j (j = 1, 2, 3 …) is identical and independently distributed (i.i.d), with probability density function (pdf) $f_S(s)$, cumulative distribution function (cdf) $F_S(s)$, mean μ_S and standard deviation σ_S.

Let SS_n denote the sum of n successive CNT spacings:

$$SS_n = \sum_{j=1}^{n} S_j \qquad (2.2)$$

The pdf of SS_n can be extracted experimentally or derived by convolving the individual distributions:

$$f_{SS_n}(w) = f_{S1}(w) * f_{S2}(w) * \ldots * f_{Sn}(w) \qquad (2.3)$$

where $f_{S1}(s) = f_{S2}(s) = \ldots = f_{Sn}(s) = f_S(s)$.

First, we will consider the case when the left side of the box is to the right of CNT 0 by an infinitesimal amount, as shown in Fig. 2.2, then.

$$\begin{aligned} \text{Prob}(N(W) <= n) &= \text{Prob}(SS_{n+1} > W) \\ &= 1 - F_{SS_{n+1}}(W) \end{aligned} \qquad (2.4)$$

where Prob(*I*) represents the probability of event *I*, and $F_{SSn}(W)$ the cumulative distribution of SS_n. From (2.4), it is clear that the probability distribution of *N(W)* is

$$\text{Prob}(N(W) = n) = F_{SS_n}(W) - F_{SS_{n+1}}(W) \qquad (2.5)$$

$F_{SS_0}(W)$ is defined as 1 so that (2.5) holds for all non-negative integers *n*.

Equation (2.5) calculates the distribution of *N(W)* for the cases when the left side of the box is to the right of CNT 0 by an infinitesimal amount as shown in Fig. 2.2a. In reality, the left side of the box corresponding to a CNFET can be at any random position. In this case, the spacing distribution of the spacing from the left side of the box to the first CNT inside the box, denoted by S_1*, is not necessarily equal to the original distribution of S_1. [Cox 62] found that the pdf of S_1* is given by

$$f_{S1*}(t) = \frac{1}{\mu_S}\int_t^{\infty} f_{S1}(x)dx \qquad (2.6)$$

If (2.6) is used in place of $f_{S1}(w)$ in (2.3), a more strict result can be derived in place of (2.5) [Cox 62]. It can be shown that the only case when S_1* has the exact same distribution as S_1 is when the spacing distributions are exponential. In this case, *N(W)* follows Poisson distribution with parameter W/μ_S.

2.3. Asymptotic Count Distribution

The methodology discussed in Sec. 2.2 can be used to derive the distribution *N(W)* for arbitrary *W*. When $W \to \infty$, the asymptotic distribution of *N(W)* can be shown [Cox 62] to follow a Gaussian distribution as a result of the central limit theorem. The asymptotic mean and variance of *N(W)* are derived [Cox 62] as

$$\lim_{W->\infty} \mu[N(W)] = \frac{W}{\mu_S} \qquad (2.7)$$

$$\lim_{W->\infty} \sigma^2[N(W)] = \frac{W\sigma_S^2}{\mu_S^3} \qquad (2.8)$$

Therefore, we have

$$\lim_{W->\infty} N(W) \sim Gauss\left(\frac{W}{\mu_S}, \frac{W \cdot \sigma_S^2}{\mu_S^3}\right) \qquad (2.9)$$

In practice, we find that *W* does not need to be very large to reach this asymptotic limit. Figure 2.3 shows the experimental count distribution *N* for a box of *W* = 2 μm along with the predicted distributions derived by both the exact calculation (2.5) and Gaussian approximation (2.9). Both predictions give similar results when compared with the experimentally extracted distribution when used in the analysis of CNFET circuits (Sec. 4). In this case, the average CNT count under this gate is only 8.9. Since the growth of m-CNTs and their removal make CNFETs with fewer CNTs unreliable for VLSI integration (more details in Sec. 3), the Gaussian approximation is appropriate for most practical cases.

As shown in (2.9), the only growth characteristics needed to derive the asymptotic CNT count distribution are the mean (μ_S) and variance (σ_S) of CNT spacing. In count data analysis, the *index of dispersion* or *Fano factor* is defined as the ratio of variance to the mean [Cameron 98]. The index of dispersion of the CNT count distribution can be calculated from the coefficient of variation of the inter-CNT spacing ($\gamma = \sigma_S / \mu_S$) as given in (2.10).

$$\frac{\sigma^2[N(W)]}{\mu[N(W)]} = \left(\frac{\sigma_S}{\mu_S}\right)^2 = \gamma^2 \qquad (2.10)$$

The index of dispersion is an important factor in determining the variation in CNFET circuit. In our extracted data, the index of dispersion

equals 0.50. For a Poisson distribution the index of dispersion is equal to 1. This implies that the experimental CNT count distribution has less variation than that of a Poisson distribution.

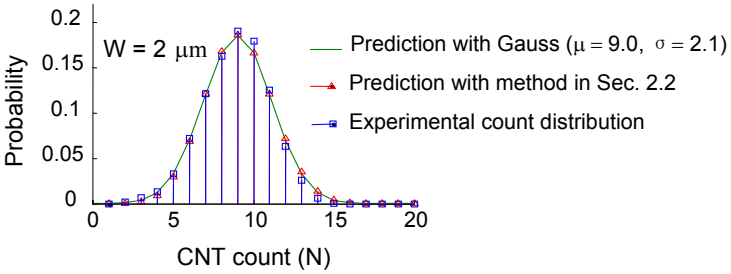


Figure 2.3. Experimentally extracted CNT count distribution compared to predicted distributions (exact method and Gaussian approximation).

2.4. Count and Spacing Distributions for Semiconducting CNTs

The discussion in Sec. 2.1 to 2.3 applies to all CNTs, regardless of their types (s- or m-CNTs). In practice, m-CNTs must be removed and the distributions of interest after m-CNT removal are the spacing and count distributions of the s-CNTs. We derive such distributions by assuming that the probability of any CNT being an m-CNT (s-CNT) is p_m (p_s), independent of the types any of its neighboring CNTs, with $p_m + p_s = 1$.

Consider the spacing between two s-CNTs separated by a random number of m-CNTs. We label the first s-CNT as CNT 0 and the subsequent s-CNT as CNT M (with M-1 m-CNTs between the two s-CNTs). Then according to the above assumption, M is a geometrically distributed random variable [Ross 01]. The spacing between the two s-CNTs can be modeled as the following stochastic sum of the original spacing distribution:

$$S_{s-CNT} = \sum_{i=1}^{M} S_i \quad with\ M \sim Geometric(p_s) \qquad (2.11)$$

In general, this distribution can be derived from its moment generating function, which is the composite function of the moment generating functions of M and S. But for the asymptotic case described in Sec. 2.3, we only need to find the mean and variance of the s-CNT spacing distribution

$$\mu(S_{s-CNT}) = \mu(M)\mu(S) \qquad (2.12)$$

$$\sigma^2(S_{s-CNT}) = \sigma^2(M)\mu^2(S) + \mu(M)\sigma^2(S) \qquad (2.13)$$

where $\mu(M) = \frac{1}{p_s}$ and $\sigma^2(M) = \frac{1-p_s}{p_s}$

Using (2.9), the s-CNT count distribution can be approximated from $\mu(S_{s\text{-}CNT})$ and $\sigma^2(S_{s\text{-}CNT})$. Then the index of dispersion ($\gamma^2_{s\text{-}CNT}$) of s-CNT count distribution can be derived as

$$\gamma^2_{s-CNT} = p_s\gamma^2 + p_m \qquad (2.14)$$

where γ is the coefficient of variation of the inter-CNT spacing for all CNTs. $\gamma^2_{s\text{-}CNT}$ is a weighed average of γ^2 and 1 with weights p_s and p_m respectively. The experimentally extracted value for γ is 0.50 (Sec. 2.3). For a p_m of 1/3, $\gamma^2_{s\text{-}CNT}$ equals 0.67. Thus, m-CNTs increase the variation of the CNT count distribution in the case of our experimentally extracted CNT density distribution.

2.5. Spatial Correlation in Count distribution

For analyzing the circuit level impact of CNT density variations, it is also necessary to characterize the spatial correlation of the CNT count distribution. We find that the spatial correlation of CNT count for aligned CNT growth is direction-dependent.

1) Count distribution in the x-direction is highly uncorrelated.

Figure 2.4a plots the correlation coefficient of CNT count as a function of the x distance (shown in the figure) between two boxes with the width of both boxes equal to 1 μm, caculated based on experimentally extracted data. When the x distance between the two boxes is less than 1 μm, the two count distributions exhibits positive correlation since they share some CNTs. However, when the x distance increases beyond the width of boxes, the correlation coefficient drops to around 0.

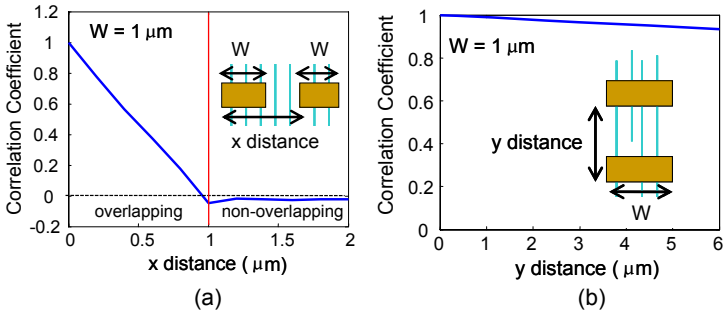


Figure 2.4. CNT correlation in x-direction (a) and y-direction (b). Based on experimentally extracted data.

2) Count distribution in the y-direction is highly correlated

Figure 2.4b shows the correlation coefficient of CNT count as a function of the y distance between the two boxes. As shown in Fig. 2.4b, the correlation coefficient remains above 0.9 up to a y distance of 6 microns. This is a direct result of well-aligned CNT growth. The gradual decrease in the correlation coefficient is mainly due to CNTs terminating in the middle of the two boxes (Fig 2.4b).

Note that Fig. 2.4 only shows the case for local correlations for the within catalyst stripes (Fig 1.1b). For larger y distances between boxes that spans across catalyst stripes, e.g. for larger circuits, a change in correlation should be expected. For chip level statistical analysis, such change must be carefully characterized and modeled. For this paper, we focus on CNFET circuits between catalyst stripes.

3. Impact of CNT Density Variation on CNFET Reliability

An important failure case of a CNFET is when there is no s-CNT left in the CNFET [Zhang 08]. We can derive the probability of such failure using the CNT density distributions derived in Sec. 2. In the case of *ideal removal* of m-CNTs (all m-CNTs are removed without removing any s-CNTs), each CNT has a probability $p_f = p_m$ of not being an s-CNT. In situations when there is inadvertent removal of s-CNTs, this probability increases to

$$p_f = p_m + p_s p_{rs} \qquad (3.1)$$

where p_{rs} is the probability that an s-CNT will be inadvertently removed. We generalize the above discussion by considering p_f as the failure probability for each CNT. Then, for a CNFET with N independent CNTs (before any removal), the failure probability for the CNFET (p_F) is given by

$$p_F = p_f^N \qquad (3.2)$$

Equation (3.2) shows that the failure probability of a CNFET exponentially decreases with the number of CNTs. When CNT density variation is taken into account, p_F is derived below based on the notion of conditional probability

$$p_F = \sum_{N_i} p_f^{N_i} \mathrm{Prob}[N(W) = N_i] \qquad (3.3)$$

where W is the width of the CNFET.

For a given CNFET width, CNT density variation (or equivalently variation in $N(W)$) always results in a higher probability of failure (p_F) compared to the case with uniform CNT density. To prove this, the arithmetic mean-geometric mean inequality can be applied to (3.3), which gives

$$p_F = \sum_{N_i} p_f^{N_i} \text{Prob}[N(W) = N_i] \geq \left[\prod_{N_i} \left(p_f^{N_i} \right)^{\text{Prob}[N(W)=N_i]} \right]^{1/\sum_{N_i} \text{Prob}[N(W)=N_i]} = p_f^{\mu[N(W)]} \quad (3.4)$$

The right hand side of inequality in (3.4) is the failure probability of the uniform density case[3].

To quantify such degradation in p_F due to CNT density variation, we can define N_{min} as the minimum average CNT count $\mu(N(W))$ for a target value of failure probability (p_F). Such definition of N_{min} corresponds to the minimum CNFET width circuit designers must satisfy for a certain average inter-CNT spacing of the given technology. Table 3.1 shows the values of N_{min} with varying p_m and p_{rs} for uniform CNT density as well as in the presence of CNT density variation using Gaussian approximation. As shown in the table, CNT density variation significantly increases N_{min} for all cases especially for small values of CNT failure probability (p_f).

Table 3.1. Minimum average number of CNTs per CNFET (N_{min}) for CNFET failure probability (p_F) = 10^{-8} with uniform CNT density and in the presence of CNT density variation.

p_m	33%	33%	10%	10%
p_{rs}	16%	0%	16%	0%
p_f	43.7%	33%	24.4%	10%
N_{min} (uniform density)	23	17	13	8
N_{min} (with density variation)	29	24	20	18

4. Circuit Level Impact of CNT Correlation

4.1. CNT Count Correlation between CNFETs

The correlation of CNT counts between two arbitrary CNFETs (shown in Fig. 4.1) is considered in this section. We assume the following two simplifications based on the results in Sec. 2.5:

1) CNT counts from non-overlapping sections of the CNFETs along the x-direction are completely uncorrelated (Fig 2.4a);
2) CNT counts from equally-sized overlapping sections of CNFETs along the x-direction are completely correlated independent of their y-locations. Figure 2.4b shows that this correlation in fact decreases with increasing y-distance between the 2 CNFETs. This slight decrease in correlation is neglected in this part and more detailed models can be used to extend the results shown below.

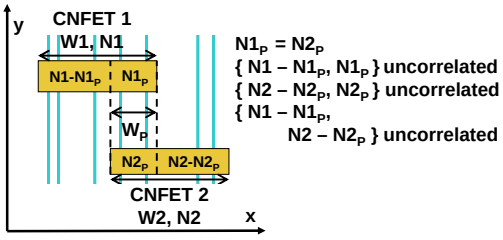


Figure 4.1. CNT count correlation between arbitrary CNFETs.

Let $W_1(W_2)$, $N_1(N_2)$ represent the width and CNT count of CNFET 1(2), and W_P, $N_{1P} = N_{2P}$ represent the width and CNT counts of the overlapping CNFET sections in the x direction. Then

$$\begin{aligned} \mu(N_1 N_2) &= \mu[(N_{1P} + N_1 - N_{1P})(N_{1P} + N_2 - N_{1P})] \\ &= \mu(N_{1P}^2) + \mu(N_1 - N_{1P})\mu(N_2 - N_{1P}) + \\ &\quad + \mu(N_{1P})\mu(N_2 - N_{1P}) + \mu(N_{1P})\mu(N_1 - N_{1P}) \end{aligned} \quad (4.1)$$

It can be further shown that the covariance between N_1 and N_2 is given by:

$$\begin{aligned} Cov(N_1, N_2) &= \mu(N_1 N_2) - \mu(N_1)\mu(N_2) \\ &= \sigma^2(N_{1P}) = \sigma^2(N_{2P}) \end{aligned} \quad (4.2)$$

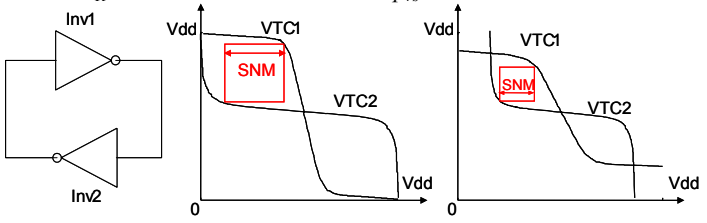
where $\sigma^2(N_{1P})$ or $\sigma^2(N_{2P})$ can be calculated using (2.8). The correlation coefficient between N_1 and N_2 is then:

$$\rho(N_1, N_2) = \frac{Cov(N_1, N_2)}{\sigma(N_1)\,\sigma(N_2)} = \frac{\sigma^2(N_{1P})}{\sigma(N_1)\,\sigma(N_2)} = \frac{W_P}{\sqrt{W_1 W_2}} \quad (4.3)$$

4.2. Utilizing CNT Correlation to Optimize Layout of Cross-Coupled Inverters

In this section, we describe a way to utilize the correction discussed in Sec 4.1 to improve the reliability of CNFET circuits. We consider a non-ideal m-CNT removal process which removes m-CNTs with probability p_{rm} and inadvertently removes s-CNTs with probability p_{rs}. Consider a pair of cross-coupled inverters (Fig. 4.2) each with a p-type CNFET (*PFET*) and an n-type CNFET (*NFET*). Static noise margin (*SNM*), defined as the maximum nested square between the normal and mirrored voltage transfer curves (*VTC*s) for the two inverters [Lohstroh 83], is used as a metric for the robustness of the cross-coupled inverters (Fig 4.2b). When m-CNTs are present, the inverters do not give a full rail-to-rail output, which reduces the gain as well as the noise margin (Fig. 4.2c).

Suppose that SNM_R is the required static noise margin that such cross-coupled inverters must satisfy. Given the CNT density distribution, CNT processing parameters (p_{rm},p_{rs}) and the width of the CNFETs (W), we can calculate the probability that a gate will fail to satisfy this SNM requirement. We refer to this as *PNMV* or *probability of noise margin violation*. We show that the layout of such cross-coupled inverters can be optimized to reduce the PNMV by up to three-orders of magnitude. Five different layout styles are studied as shown in Fig. 4.3. The different styles have different degrees of correlation among the four CNFETs comprising the cross-coupled inverters. The symmetries in VTCs caused by such correlation are also shown in Fig 4.3. Style 1 (Fig. 4.3a) has perfect correlation among the drive strengths of all four CNFETs. Style 2 (Fig. 4.3b) has perfect correlation between the PFET and NFET of each inverter, while the CNFETs in the different inverters are uncorrelated. Style 3 (Fig. 4.3c) has perfect correlation between the PFET of one inverter and the PFET of the second inverter and similarly for the NFETs. Style 4 (Fig. 4.3d) has perfect correlation between the PFET of one inverter and the NFET the other and vice versa. Style 5 (Fig. 4.3e) has completely uncorrelated CNTs. A CNFET SPICE model [Deng 06] with a 32 nm CNFET technology is used to simulate the VTCs. This SPICE model has been calibrated to experimental data with 90% accuracy [Amlani 06]. We assume a uniform CNT diameter of 1.5 nm and p_m = 1/3. SNM_R is assumed to be Vdd / 4 and p_{rs} = 16%[4]



(a) (b) (c)

Figure 4.2 Cross-coupled CNFET inverters (a) with Voltage Transfer Curves without m-CNTs (b) and with m-CNTs (c).

[3] Even with uniform CNT density, the CNT count distribution of a CNFET is actually bimodal with possible values of N = [W/s]-1 and [W/s]+1, where s is the uniform inter-CNT spacing. However, the failure probability of this case is very close to the unimodal case and all the discussions are valid.

Figure 4.4 shows the PNMV for the 5 layout styles as a function of the survival probability of m-CNTs ($1 - p_{rm}$). Symmetry in the VTCs of the two CNFET inverters, introduced by correlation among CNFETs, plays an important role in determining the PNMV. Layout styles 1, 2 and 3 ensure symmetry between the two "eye-openings" of the VTC curves and therefore have low PNMV values. Style 4 has the highest PNMV for all values of p_{rm} because of the anti-symmetry in the VTC curves (Fig. 4.3d). Style 5 has no inherent symmetry because all the CNFETs are uncorrelated and has intermediate values of PNMV.

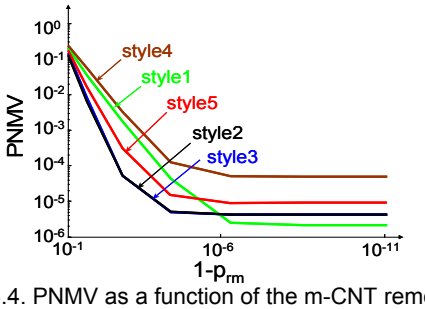


Figure 4.4. PNMV as a function of the m-CNT removal rate for five different layout styles shown in Fig. 4.3. Gaussian approximation of CNT count distribution is used with μ(N) = 20.

When the removal probability of m-CNTs is very high ($1- p_{rm} < 10^{-6}$), there are negligible number of surviving m-CNTs. In this limiting case, failure of this circuit is due to no CNTs left in the CNFETs because of either inadvertent removal of s-CNTs or CNT density variation as discussed in Sec. 3. PNMV value in this case for layout styles 1, 2, 3 and 5 (style 4 is an exception because of its anti-symmetry) can be given by

$$PNMV = 1-(1-p_F)^k \approx kp_F \quad (4.4)$$

where k is number of uncorrelated CNFETs in the circuit and p_F is the failure probability for each one of them, calculated using equation (3.4). Style 1 is has the lowest PNMV because of perfect correlation between the 4 CNFETs ($k = 1$). Styles 2 and 3 ($k = 2$) and style 5 ($k = 4$) have higher values of PNMV.

For lower probabilities of m-CNT removal ($1 - p_{rm} > 10^{-6}$), the presence of m-CNTs can no longer be ignored and becomes the dominant factor in PNMV. In this case, style 1 does not perform as well as styles 2, 3 and 5, since the presence of m-CNTs will cause equal degradation of all four correlated CNFETs in style 1, while such equal degradation is unlikely in the case of uncorrelated CNFETs in styles 2, 3 and 5.

4.3. Delay Variations

Suppose inverter I_1 has N_1 s-CNTs, driving inverter I_2 with N_2 s-CNTs. We assume that the NFET and PFET of each inverter are perfectly correlated, similar to layout style 2 (Fig. 4.3b) discussed in Sec. 4.2. The first order delay model can be written as:

$$d_{1\to 2} = \frac{C_{load}V_{dd}}{I_{drive}} = \frac{C_I + N_2C_0}{N_1I_0}V_{dd} \quad (4.5)$$

where C_I is the interconnect capacitance, C_0 is the capacitance per CNT, I_0 is the drive current per CNT. Second order effects such as diameter dependence of CNT capacitance and current drive, and the charge-screening effect are not included [Deng 07b, Kshirsagar 08].

With a first order Taylor expansion ([Chang 03]), (4.5) can be written as

$$d_{1\to 2} = d^0_{1\to 2} + \left(\frac{\partial d_{1\to 2}}{\partial N_1}\right)_0 \Delta N_1 + \left(\frac{\partial d_{1\to 2}}{\partial N_2}\right)_0 \Delta N_2 \quad (4.6)$$
$$= d^0_{1\to 2} - \frac{C_I + N_2C_0}{N_1^2I_0}\Delta N_1 + \frac{C_0}{N_1I_0}\Delta N_2$$

The variance of the delay caused by CNT density variation is then

$$\sigma^2(d_{1\to 2}) = \left(\frac{C_I + N_2C_0}{N_1^2I_0}\right)^2 \sigma^2(N_1) + \left(\frac{C_0}{N_1I_0}\right)^2 \sigma^2(N_2) \quad (4.7)$$
$$-2\left(\frac{C_I + N_2C_0}{N_1^2I_0}\right)\left(\frac{C_0}{N_1I_0}\right)Cov(N_1,N_2)$$

The covariance term in (4.7) can be calculated using (4.2). Note that a positive correlation between N_1 and N_2 helps in reducing the overall delay variation. As an example, consider two inverter chains with all inverters equally sized:

1) Correlated inverter chain: CNTs in the PFETs and NFETs of all inverters are perfectly correlated. For example, all the inverters are laid out along in y-axis in Fig. 4.1.

2) Uncorrelated inverter chain: The NFET and the PFET within each inverter are still perfectly correlated but there is no correlation between CNTs in different inverters. For example, all the inverters are laid out along in x-axis in Fig. 4.1.

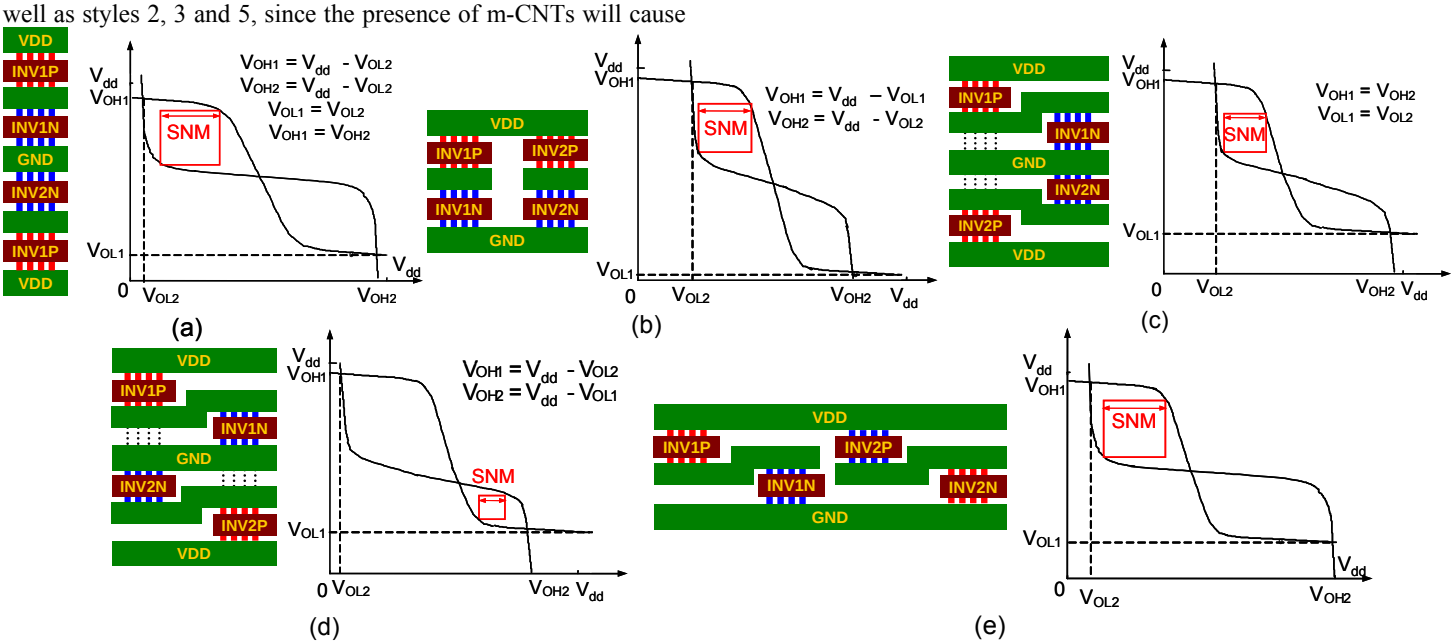


Figure 4.3. CNFET cross-coupled inverter layout styles 1 – 5 (a through e) with varying degrees of CNT correlation.

Using the same CNFET SPICE model described in Sec. 4.2, we performed Monte-Carlo simulations, each with 2000 samples, of these two inverter chains with different number of stages in the presence of CNT density variation and ideal m-CNT removal (defined in Sec. 3). Table 4.1 shows the simulation results using both the experimentally extracted CNT count distribution and the Gaussian approximation to CNT count distribution. The Gaussian approximation gives less than 5% error when compared to the results using the experimentally extracted CNT count distribution.

Table 4.1 Simulated delay variations for correlated and uncorrelated inverter chains (W = 3 μm for all CNFETs) using 2000 sample Monte Carlo simulations with experimentally extracted CNT count distribution. Results in parenthesis use the Gaussian CNT count distribution.

	Correlated			Uncorrelated		
No. of stages	3	5	10	3	5	10
μ(delay) (ps)	2.93 (2.93)	4.89 (4.88)	9.77 (9.77)	2.98 (2.98)	4.97 (4.97)	9.93 (9.93)
σ(delay) (ps)	0.06 (0.06)	0.10 (0.09)	0.20 (0.19)	0.13 (0.13)	0.15 (0.15)	0.19 (0.18)
σ(delay) / μ(delay) (%)	1.97 (1.90)	2.02 (1.93)	2.04 (1.97)	4.49 (4.31)	3.07 (2.91)	1.88 (1.83)
Average σ(delay) / μ(delay) per stage (%)	1.97 (1.90)	2.02 (1.93)	2.04 (1.97)	8.90 (8.53)	8.72 (8.49)	8.57 (8.50)

The following observations can be made from the simulation results presented in Table 4.1:

1. The correlated inverter chain gives lower per-stage variation. This effect can be shown from (4.7) since the covariance term is positive. In the limiting case when $C_l \rightarrow 0$, the per-stage variation drops down to zero. However, the multiple stages are perfectly correlated, so the σ/μ for the delay per stage is the same as the σ/μ for the total delay.
2. The uncorrelated inverter chain gives higher per-stage variation because the covariance term in (4.7) is zero. However, it can be shown that the delays of successive stages are negatively correlated resulting in faster than $\sqrt{N}$ drop in delay variation as number of stages increases. Therefore, when logic depth is high, the variability is similar to what we can achieve in the correlated case.

5. Conclusion

Since CNTs are grown using chemical self-assembly, it can be extremely difficult to guarantee perfect alignment, positioning and uniform density of CNTs. Hence, we have to design circuits that can tolerate CNT imperfections. This paper shows that, in addition to imperfections caused due to mis-positioned CNTs and metallic CNTs, density variations in CNT growth result in compromised reliability and increased delay variation in CNFET circuits. To be able to analyze the effects of such CNT density variations, parameterized models supported by experimental data are needed. This paper presents such a model fitted to data from images of aligned CNTs. This model, with appropriate data input to account for CNT correlation, can be applied to statistical timing analysis or yield analysis of VLSI circuits. The correlation in aligned CNT growth has a significant impact on design metrics such as noise margin and delay variation. The reliability of CNFET circuits can be significantly improved by taking advantage of the correlation in aligned CNTs.

6. References

[Amlani 06] Amlani I., *et al.*, "First Demonstration of AC Gain From a Single-walled Carbon Nanotube Common-Source Amplifier," *Proc.IEDM*, pp. 1-4, 2006.

[Cameron 98] Cameron A. C. and P. K. Trivedi, *Regression Analysis of Count Data*, Cambridge University Press, 1998.

[Collins 01] Collins P., S. Arnold, P. Avouris, "Engineering carbon nanotubes and nanotube circuits using electrical breakdown", *Science*, vol. 292, pp. 706 – 709, 2001.

[Chang 03] Chang H. and S. Sapatnekar, "Statistical timing analysis considering spatial correlation in a PERT-like traversal," *Proc. ICCAD*, pp. 621-625, 2003.

[Cox 62] Cox, D. R., *Renewal Theory*, Methuen & Co, 1962.

[Deng 06] Deng J., H.-S. P. Wong, "A Circuit-Compatible SPICE model for Enhancement Mode Carbon Nanotube Field Effect Transistors", *Proc. SISPAD*, pp. 166 – 169, 2006.

[Deng 07a] Deng J., *et al.*, "Carbon Nanotube Transistor Circuits: Circuit-Level Performance Benchmarking and Design Options for Living with Imperfections", *Proc. ISSCC*, pp. 70-588, 2007.

[Deng 07b] Deng J., and H. -S. P. Wong, "A Compact SPICE Model for Carbon Nanotube Field Effect Transistors Including Non-Idealities and Its Application — Part I: Model of the Intrinsic Channel Region", *IEEE Trans. Elec. Dev.*, pp.3186-3194, 2007.

[Kang 07] Kang S. J., et al., "High-Performance Electronics Using Dense, Perfectly Aligned Arrays of Single-Walled Carbon Nanotubes", *Nature Nanotechnology*, vol. 2, pp. 230-236, 2007.

[Kocabas 07] Kocabas C., et al., "Improved Synthesis of Aligned Arrays of Single-Walled Carbon Nanotubes and Their Implementation in Thin Film Type Transistors", *Journal of Physical Chemistry C* 111(48), 17879-17886 (2007).

[Kshirsagar 08] Kshirsagar C., H. Li, T. Kopley, and K. Banerjee, "Accurate Intrinsic Gate Capacitance Model for Carbon Nanotube-Array Based FETs Considering Screening Effect", *IEEE Electron Device Letters*, Vol. 29, No. 12, pp. 1408-1411, 2008.

[Lohstroh 83] Lohstroh, J., E. Seevinck, and J.D. Groot, "Worst-Case Static Noise Margin Criteria for Logic Circuits and Their Mathematical Equivalence", *JSSC*, No.6, pp. 803-806, 1983.

[Narendra 01] Narendra S., et al., "Scaling of Stack Effect and its Application for Leakage Reduction", *Proc. ISLPED*, pp. 195-200, 2001.

[Nieuwoudt 07] Nieuwoudt A., and Y. Massoud, "On the Impact of Process Variations for Carbon Nanotube Bundles for VLSI Interconnect," *IEEE Transactions on Electron Devices (T-ED)*, Vol. 54, No. 3, 2007

[Patil 08a] Patil N., *et al.*, "Integrated Wafer-scale Growth and Transfer of Directional Carbon Nanotubes and Misaligned-Carbon-Nanotube-Immune Logic Structures," *Symp. VLSI Technology*, pp. 205-206, 2008.

[Patil 08b] Patil N., *et al.*, "Design Methods for Misaligned and Mis-positioned Carbon-Nanotube-Immune Circuits," *IEEE Trans. Computer-Aided Design*, pp. 1725-1736, 2008.

[Ross 01] Ross, S. M., *A First Course in Probability*, Prentice Hall, 2001.

[Ross 05] Ross, S. M., *Introductory Statistics*, Academic Press, 2005.

[Zhang 06] Zhang G., *et al.*, "Selective Etching of Metallic Carbon Nanotubes by Gas-Phase Reaction", *Science*, Vol. 314, pp. 974 – 977, 2006.

[Zhang 08] Zhang J., N. Patil, and S. Mitra, "Design Guidelines for Metallic-Carbon-Nanotube-Tolerant Digital Logic Circuits", *Proc. DATE*, pp. 1009 – 1014, 2008.