

Real-Time Software Receiver Using Massively Parallel Processors for GPS Adaptive Antenna Array Processing

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Possible aviation application: Protecting GBAS ground facility

Receiver Architecture: Initial Phase Alignment

[De Lorenzo et al., ION GNSS 2010]

Computational Cost

	Single-antenna L1 receiver	4-antenna adaptive beamsteering L5 receiver
Sampling rate	4 Msps X	(10 40 Msps
Number of channels	12 ×	x 5 60
	T: Computational cost 12-channel L1 software	st for $50 \text{ T} \rightarrow 100 \text{ T}$ re receiver
Synthesis of 4-antenna data	None Bearri	ation gost .7 T x 12 beams = 20 T
Covariance calculation	None Adaptive	e processing 15 T
Sample resolution	2 bits No bit-W (About twice fast	Nise parallelism 14 bits ter [Decinea et al., 2003])

Objective: Real-time 4-antenna adaptive beamsteering L5 software receiver (85 of integer-correlation L1 receivers; 135 of bit-wise-parallel-correlation L1 receivers)
Don't: Have hardware support such as FPGA or ASIC
Do: Use a desktop computer with commercial-off-the-shelf processors

Commercial-off-the-shelf desktop parallel processors

Hardware Setup

Raw IF data collection setup (4 sets)

Demonstrate real-time computational capability for L5 processing

global memory, gmem (green)

Time

Hardware Parallelism

17

18

Real-Time Receiver Demo (Recorded)

Real-Time Receiver Demo (Recorded)

Objective:

- Real-time, 4-antenna, all-in-view, adaptive beamsteering GPS software receiver capable of L5 signal processing and running on a desktop computer

Results:

- Developed an optimized parallel computation architecture for the beamsteering receiver on cost-efficient CPU & GPU
- Confirmed real-time computational capability and anti-jamming performance under a synthetic CDMA jammer
- Demonstrated that cost-efficient commercial-off-the-shelf hardware and processors would be enough to implement an adaptive beamsteering GPS receiver

