Radiation-hardened Wideband LNA and ADC for Space-based Measurements

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Introduction

Recently, efforts to investigate the nature of wave particle interactions within the Van Allen belts of the Earth’s magnetosphere have intensified [1]. While of particular appeal for further study in applications ranging from defense tactics such as radiation-belt remediation to the plasma physics underlying modern consumer electronics, this region is notoriously inhospitable to high-fidelity scientific instrumentation on account of the strong doses of ionizing radiation to which circuits are exposed as a result of large fluctuations in trapped energetic particles. In particular, plasma wave receivers for in-situ electric-field measurements must withstand such particle fluxes while still capturing signatures of impulsive natural phenomena over much of the ULF-MF portion of the spectrum (100 Hz - 1 MHz, as shown in the figure to the right) with sufficient linearity and dynamic range.

This work demonstrates a custom, plasma wave receiver composed of two application-specific integrated circuits (ASICs), as shown in the block diagram to the left: a preamplifier comprising a radiation-hardened low-noise amplifier (LNA) and anti-aliasing filter (AAF), and an analog-to-digital converter (ADC). As opposed to existing receivers which, at any point in time, can only capture signals over some subset of the frequency and/or magnitude range depicted above, this architecture is able to process the full complement of waves simultaneously on account of the wide bandwidth and linear dynamic range of the ASICs.

LNA Architecture

To realize a passband gain whose accuracy remains stable over the lifetime of the pair, so that the standard error of the measured data is consistent even as the gain itself is maintained between -20 and 0 dB, the LNA cannot assume an open-loop topology. Furthermore, we augment a traditional passive outer feedback loop with an active inner feedback loop around the transistors that generate the open-loop gain such that its sensitivity is significantly reduced. To realize this strategy, the topology of the LNA is adapted from [3] in the context of instrumentation amplifiers and shown in the figure below.

The converter also employs radiation hardness by design techniques, including the use of enclosed terminal NMOS layouts on key switches, extensive guard-ringing, care to prevent floating nodes during operation, and others.

ADC Architecture

The ADC is a 6-stage, fully-differential, switched-capacitor pipeline converter with a dedicated track and hold. It is built using only the MOSFET layers of the BICMOS process. Offset cancellation techniques are used to improve the low frequency noise response. A self-calibration algorithm is deployed on the first three stages to improve converter linearity. Conceptually, the calibration measures the DAC codes of a stage using the down-stream stages; with these more accurate DAC codes, the converter can provide 90-dB SFDR with only a 12-bit digital reconstruction; this is seen to right.

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Enclosed Terminal Devices

Under radiation, NMOS devices display increased source-to-drain leakage current through breakdown of parasitic edge devices under the soft-restart passivation oxide. To prevent this, these designs deploy a non-standard NMOS layout that extends the thin gate oxide to completely enclose the source/drain leakage path now passes underneath hard-thin gate oxide [4]. This is deployed on select NMOS devices.

LNA TID Radiation Results

Under both 1Co γ-ray and 50-MeV H+ exposures, the DC gain is stable to ±0.65 dB up to 1 Mrad, and the flatness of the passband gain (as measured by the 3 dB-ripple), is preserved to within 0.19 dB over the same range. This marked improvement over the ∼3 dB degradation in peak gain for the ngn devices in this work highlights the efficacy of our feedback techniques. Similarly, the drop in the 3-dB bandwidth at 1 Mrad TID is approximately 15% for both sources, confirming that the predominant TID damage mechanisms consist of interface states and oxide trapped charge; displacement damage is negligible.

Single-Event Latchup

These BiCMOS ASICs are fabricated on a non-epi substrate, making them susceptible to single-event latchup (SEL). To mitigate this, extensive guard-ringing (i.e. use of well and substrate contact rings) is deployed liberally throughout the design; to left is an example. To assess SEL, the devices were subjected to heavy-ion testing at the 88 inch cyclotron facility at Lawrence Berkeley National Laboratories (LBNL). Both AC and DC input signal agitation was applied for both ASICs. All SEL testing was done at room temperature. Neither the preamplifier ASIC nor the ADC demonstrated latchup for LETs as high as 58 MeV cm²/mg, the highest energy ion available in the 10 keV cocktail.

Conclusions

We have validated the utility of a class of architectural, implementation-level, and layout-based hardness-by-design techniques by illustrating the robust TID and SEL performance of the LNA and ADC for γ-ray, H+, heavy ion, and pulsed-laser irradiations. Their robustness, coupled with their high-linearity, wide bandwidth, low power consumption, and minimal weight, make these ASICs well-suited for many space applications, including plasma wave receivers for interferometric experiments via nano-satellite clusters.

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References