RF notch filter architecture

The filter chosen for this work is based on the simple Q-enhanced technique shown below where the resonance frequency of the on-chip inductors is directly tuned by the temperature coefficient of the varactors. The degree of parasitic capacitance in the varactor decreases the effective Q. The effective Q of the Q-enhanced resonators is increased leading to a so-called Q-enhanced resonator [1]. It was shown by Wiser et al. [2] that Q-enhancement can be successfully implemented to achieve even multi-stage bandpass filters in RF CMOS with arbitrary filter response. In this poster, a new notch filter architecture based on Q-enhanced resonators is proposed that resembles the shape of SAW filters more closely.

RF filter layout

The layout of the RF filter is shown in the figure below. A MOSFET varactor diode allows tuning of the LC tank circuit. Care has been taken in the design of the spiral inductors such that parasitic capacitance is minimized to achieve a high quality factor.

Application 1: Direct RF-sampling GNSS receiver

Bandpass sampling architectures, also called subsampling architectures, exhibit several advantages over super-heterodyne architectures. First, the complexity of subsampling architectures is significantly lower since no Phase-Locked-Loop (PLL) is required. A direct consequence is that downconversion from RF to IF can be achieved with significant power savings as compared to the super-heterodyne architecture. Another significant benefit of such architectures is the capability to process multiple signals at the same time. The property to simultaneously handle multiple carriers makes subsampling architectures particularly suited for GNSS applications, as downconversion of multiple frequency bands is required in GNSS environments. With the advent of the new civilian GPS signal L2C and L5 in 2007 and 2009, respectively, and the cost of the new Galileo signal, a receiver that can process multiple signals simultaneously without adding complexity is highly desired. In fact, a bandpass sampling GNSS receiver front-end made of discrete components was proposed and investigated by Akos et al. [3], [4], a strategy for determining the optimum sampling frequency for such a GNSS receiver was found by Piski et al. [5]. As Piski showed, it is possible to downconvert the GPS frequencies L1, L2 and L5 and the Galileo signals simultaneously with a sampling frequency of 55.51, 77.33 or 99.23 MHz. It is evident that subsampling receivers, in theory, do not deliver sufficient performance as compared to super-heterodyne receivers. However, a major obstacle is that such architectures require good bandpass filtering before the digitization to prevent noise and interference aliasing. The proposed RF filter can be used as a component in such architectures to reduce the Noise Figure of the system and to suppress unwanted interference.

Application 2: Replacement of off-chip SAW filter

The on-chip RF bandpass filter architecture proposed in this poster can be used to replace the off-chip SAW filter or to relax the requirements on the SAW-filter. The magnitude response of the on-chip RF bandpass filter is shown in the picture. The bandwidth of the filter is approximately 15 – 20 MHz and the attenuation can be greater than 30 dB. It is possible to achieve even higher attenuation through tuning. The gain of the filter is roughly 30 dB. The noise figure of this filter can be greater than 15 dB. Therefore, it should be placed after a LNA with sufficient gain.

Conclusion

A fully integrated BICMOS RF filter suitable for GNSS and GPS receiver front-ends was presented. The filter can be employed in an integrated direct RF or integrated bandpass sampling architecture as well as part of a traditional heterodyning architecture. It provides excellent interference suppression and can also be used to relax the requirements on the off-chip SAW filter.