Optimization of Phase-Locked Loop Circuits via Geometric Programming

Outline

• Motivation

• Geometric programming (GP)

• GP compatible transistor models

• Clock generation PLL topology

• PLL design in GP form

• Silicon results
Simulation-based methods

W1 = 1
W2 = 2
:     :
L8 = 1

- General purpose
- Long design cycles
- Needs circuit expert
- Needs optim. expert

Power = 1
Gain = 500
Geometric programming-based method

Gain $> 100$

$BW > 10\text{MHz}$

$0.13\text{μm CMOS}$

Gain $= f_1(R, M_1, I_b)$

$BW = f_n(R, M_1, I_b)$

$M_1.gm=f_1(W, L, \ldots)$

$M_1.Cgs= f_n(W, L, \ldots)$

Numerical GP Optimization Solver
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Geometric programming

• A monomial function $g(x)$ has the form
  \[ g(x) = cx_1^{\alpha_1} x_2^{\alpha_2} \cdots x_n^{\alpha_n} \quad (c > 0) \]

• A posynomial function $f(x)$ is a sum of monomials
  For example,
  \[ f(x) = 2x_1 x_2^{-0.7} + 0.5 x_1^2 x_3^5 \]

• Geometric program (GP) is
  \[
  \begin{align*}
  \text{minimize} & \quad f_0(x) \\
  \text{subject to} & \quad f_i(x) \leq 1 \quad i = 1, \ldots, m \\
  & \quad g_i(x) = 1 \quad i = 1, \ldots, p \\
  & \quad x \geq 0
  \end{align*}
  \]

GPs can be easily transformed into convex problem
Solving GP’s

New *interior point* methods for GP

- are *extremely fast*
- find *globally optimal* solution or provide proof of infeasibility
- are *independent* of starting point

For PLL synthesis: 40k optimization variables and 150k constraints takes ~90 minutes on 2GHz PC
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GP electrical models

\[ I_{DS} = k \frac{W}{L} (V_{GS} - V_T)^2 \]
\[ I_{DS} = k W^1 L^{-1} V_{OV}^2 \]
\[ V_{DS} \geq V_{GS} - V_T \]

\[ g_m = 2k \frac{W}{L} (V_{GS} - V_T) \]
\[ g_m = c_2 W^1 L^{-1} V_{OV}^1 \]
\[ C_{gs} = \frac{2}{3} C_{OX} W L + C_{OX} W L_D \]

- Complex GP models can be developed including short-channel effects, finite output impedance, etc..., e.g.,

\[ g_m = \sum c_i I_{DS}^{\alpha_1,i} L^{\alpha_2,i} W^{\alpha_3,i} V_{DS}^{\alpha_4,i} V_{SB}^{\alpha_5,i} \]
GP models – Id vs. Vds, 0.18μm
GP physical models

Placement and Routing
- Symmetry Constraints
- Mirroring Nets
- Net Matching
- Alignment
- Capacitance Constraints
- Shielding
- EM/IR drop considerations
- Dummy poly for matching and STI

Posynomial expressions for Width and height, e.g.,

\[ \text{Height} = 2x_0 + x_1 + W \]

AD, AS, PD & PS, e.g.,

\[ AD = N_f (W + 2W_D) (L_D + L_{DIF} + H_{DIF}) \]
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PLL topology

Charge pump (CP) Loop filter (LF) Voltage-controlled oscillator (VCO)

- Charge pump PLL with low-power programmable dividers (12 bit, >2GHz)
- Variables include device dimensions (W,L) and # of ring oscillator stages (S)
Charge pump topology

Example current mirror equalities (monomial):

\[ L_{M5c} = L_{M5b} \]

\[ V_{gov,M5c} = V_{gov,M5b} \]
VCO topology

Example saturation margin inequalities (posynomial):

\[ V_d \geq V_{\text{gov},M1v} \]
\[ V_d \leq V_{dd} - V_{\text{gov},M3v} \]
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Second-order PLL system-level equations, in monomial form

\[ \omega_n = \sqrt{\frac{K_{cp}K_{VCO}}{2\pi NPC_1}}, \quad \zeta = \frac{\omega_n RC_1}{2} \]

\[ K_{cp} = I_{ref} \left( \frac{W_{M5c}L_{M5b}}{W_{M5b}L_{M5c}} \right) \]

\[ K_{VCO} = g_{m,M1v} \left( \frac{W_{M3v}}{W_{M2v}} \right) \left( \frac{\partial \omega_{VCO}}{\partial I_{ring}} \right) \]
Power consumption (posynomial)

\[ Power = Power_{CP} + Power_{VCO} + Power_{digital} < Power_{spec} \]

\[ Power_{CP} = V_{dd} (4I_{ref} + I_p) + Power_{Acp} \]

\[ Power_{VCO} = V_{dd} (I_{d,M2v} + I_{ring}) + Power_{Avco} \]
Accumulated jitter, $T_{aj}$ (posynomial)

\[ T_{aj}^2 = \sigma_{j,pk}^2 < \left( T_{aj,\text{spec}} \right)^2 \]

\[ \sigma_{j,pk}^2 = \left( \kappa_{LF}^2 + \kappa_{VCO}^2 \right) \frac{1}{2\zeta \omega_n} \]

From McNeil (JSSC 1997):

\[ \kappa_{LF}^2 = 4kTR \left( \frac{K_{VCO}^2}{2\omega_{VCO}^2} \right) \]

Using Hajimiri’s phase noise model (JSSC 1998):

\[ \kappa_{VCO}^2 = \left( \frac{\Gamma_{\text{rms}}}{C_L V_{\text{d}} \omega_{VCO}} \right)^2 \left( \frac{4kT \gamma}{2} \right) \left( g_{m,Mn} + g_{m, Mp} \right) S + \left( \frac{\partial \omega_{VCO}}{\partial I_{\text{ring}}} \right)^2 \left( \frac{1}{2\omega_{VCO}} \right) 4kT \gamma \left[ g_{m,M3v} + \left( \frac{W_{M3v}}{W_{M2v}} \right)^2 \left( g_{m,M1v} + g_{m,M2v} \right) \right] \]
Static phase error, $T_{\text{err}}$ (posynomial)

Using Pelgrom’s mismatch model (JSSC 1989):

$$T_{\text{err}}^2 = \sigma_{I_p}^2 \frac{t_{r, \text{PFD}}^2}{I_p^2} < (T_{\text{err}})^2$$

$$\sigma_{I_p}^2 = \frac{I_p}{I_{\text{ref}}} \left( \sigma_{I_{d, M5b}}^2 + \sigma_{I_{d, M7b}}^2 \right)$$

$$\sigma_{I_{d, M5b}}^2 = \left( \frac{\sigma_{\beta I_{d, M5b}}}{\sqrt{W_{M5b} L_{M5b}}} \right)^2 + \left( \frac{\sigma_{V_{t g m, M5b}}}{\sqrt{W_{M5b} L_{M5b}}} \right)^2$$
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### GP vs. Silicon – 0.18um PLL arrays

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- Good agreement between GP and silicon meas.
### GP vs. Silicon – 0.13um PLL arrays

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- Good agreement between GP and silicon meas.
Acc. jitter vs. $\Delta F_{vco}$ trade-off analysis
Power vs. $\Delta F_{\text{vco}}$ trade-off analysis

![Graph showing the relationship between power and VCO frequency range.](image-url)

- **Y-axis:** Power (mW)
- **X-axis:** VCO frequency range (MHz)

As the VCO frequency range increases, the power required also increases.
Automated design does not translate into performance degradation

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Simulated 0.13μm, worst case PVT (FF, -40C or 125C) with 10% step on Vdd

Comparison to Literature

- **0.10 %Tvco/%Vdd** for 2.5V, 800-1400MHz PLL
  (M. Mansuri, ISSCC 2003)

- **0.08 %Tvco/%Vdd** for 2.0V, 800-1330MHz PLL with voltage regulator
  (V. Van Kaenel, JSSC 1998)

Room temperature with 10% step on Vdd
Conclusions

- First demonstration of fully-automated PLL design, from specification to GDSII
- PLL design problem cast in GP form reduces design time from weeks to hours
- Measured 0.18 μm and 0.13 μm CMOS PLL arrays agree with GP predictions (e.g. 1.9 GHz, 11 mW PLL with 5.8 ps long-term jitter)
- Robust, systematic, and efficient PLL design