RESISTIVE MEMORY DEVICES

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Outline

Existing Memory Technology
- Flash Memory, SRAM, DRAM
  - Working Principle, Advantages and Disadvantages

Need for New Technology

Next Generation Memory Devices
- Commercially Available: MRAM, PCRAM, CBRAM, FeRAM
  - Working Principle, Advantages and Disadvantages
- Infant memories: STT-RAM, SONOS, Millipede, NRAM
  - Working Principle, Advantages and Disadvantages

Comparison

Current state of the new technology memory devices

Acknowledgements and References
Flash Memory: Working Principle

- Floating gate
  - No charge => 1
  - Trapped Electrons => 0
- Read: $V_T$ of the transistor increases due to trapped electrons
  - $V_{T0} < WL < V_{T1}$; pre-charge BL; binary o/p (sense amplifier)
- Write: Electrons can tunnel across the oxide under high voltage (Hot electron injection)
  - Large voltage is applied to gate (WL), BL is pulled high
  - Program/Erase depending on polarity of gate voltage
Advantages and Disadvantages

Advantages

• Non-volatile
• High density: Stacked memory, Multi-level cells

Disadvantages

• Block erase and re-write: lacks 0 \rightarrow 1 bit-wise alterability
  • Solution: Flash type file systems
• Memory wear: finite number of P/E cycles
  • Solution: Writes with dynamic remapping, level wear algorithms
• Read disturb
  • Solution: Periodic re-write after fixed number of reads
• Slow writes (Charge pump takes time to build up charge)
• High write power
• Write Amplification
SRAM: Working Principle

- Data is stored on mutually reinforcing inverters
- Read: WL is driven high BL pre-charged and then connected to Sense Amplifier
- Write: Bit lines are connected to strong drivers and then WL is driven high
- 1T, 3T, 4T, 6T, 8T, 10T, 12T SRAM also exist
  - 1T, 3T SRAM – Not really static – Pseudo DRAM (Require refresh)
  - 4T SRAM – Static power dissipation
Advantages and Disadvantages

**Advantages**

- Very fast (used as cache memory)
- Data refresh is not required
- Low power consumption
- Memory wear does not occur
- Low operating voltages

**Disadvantages**

- Volatile
- Not compact (6T, 8T, 10T, 12T cells)
- Costly
DRAM: Working Principle

- Data is stored as charge on a storage capacitor
- Read: BL is pre-charged WL is set to 1.
- The capacitor does/doesn’t discharge the bit line depending on the capacitor state.
- Read operation is destructive
- Write: Bit line is driven to required logic level, then WL = 1

- 3T DRAM – Reads are not destructive, more chip area
Advantages and Disadvantages

**Advantages**

- Very compact (1T-1C)
- Simple structure
- Cheap (used in main memory in computers)

**Disadvantages**

- Volatile
- Data needs to be refreshed periodically
- Destructive Reads (solved by use of sense amplifier)
- High power consumption while idling
- As the cell size decreases, the refresh rate required for reliable memory operation increases
Need for New Memory Technology

• The new memory should aim at combining the advantages of various existing memories into a single memory

• Requirements for a memory to act as “Universal Memory”
  • Fast read, write (low latency)
  • Low read, write power and zero idling power
  • Non-volatility
  • Refresh should not be required
  • Compact, simple structure
  • Cheap
  • Reliable operation even at high temperatures
Conventional MRAM: Working

Two thin ferromagnetic, conducting films with a non-magnetic, conducting spacer

\[ GMR(\%) = \frac{\Delta R}{R_{\uparrow\uparrow}} = \frac{R_{\uparrow\downarrow} - R_{\uparrow\uparrow}}{R_{\uparrow\uparrow}} \]

10-80% decrease in electrical resistance

Albert Fert and Peter Grünberg (1988)
Working Principle

• Tunnel MagnetoResistance: Extension of GMR concept
  • Spacer: Thin insulating tunnel barrier (rather than non-ferromagnet)
  • Much larger MR value (up to 10 times GMR at room temperature)
• Ferromagnets have spin dependent densities of states
• Spin of electrons is conserved during tunneling
• Tunnelling of spin up / spin down electrons are independent processes
• Electrons in a spin state in the first ferromagnetic film are accepted by unfilled states for the same spin in the next film
• This gives rise to spin dependent resistance for electrons flowing through a ferromagnet
Working Principle: Spin Valve GMR

**Hard layer**: magnetization is fixed.

**Soft layer**: magnetization is free to rotate.

Spacer material Cu (copper) and ferromagnetic layers NiFe (perm alloy).

Effective resistance is much lower in the parallel case since electrons with parallel spin can tunnel very easily.
Working Principle

- Bottom layer: Fixed or pinned layer
  - Inter-layer exchange coupling between ferromagnetic and anti-ferromagnet.
- The equivalent circuit is MTJ is series with a transistor
Read / Write process

- **Read**: Resistance measurement.
  - The transistor is turned ON
  - Sense current is passed through the cell to ground

- **Write Process**:
  - Transistor is “OFF” and current is passed through the write lines, an induced magnetic field is created at the junction, which alters the polarity of the free layer.
Writing process

In order to change the polarity of the free layer, both fields are necessary.

Only the bit in which current is applied in both hard and easy axis will be written. The other bits will remain half-select.
Advantages and Disadvantages

<table>
<thead>
<tr>
<th>Advantages</th>
<th>Disadvantages</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Non-volatile</td>
<td>• Half select (write disturb) problem</td>
</tr>
<tr>
<td>• No refresh needed</td>
<td>• Scalability issue</td>
</tr>
<tr>
<td>• Small cell size</td>
<td>• High write power</td>
</tr>
<tr>
<td>• High speed read / write</td>
<td>• Need for a new technology fab</td>
</tr>
<tr>
<td>• Simple architecture</td>
<td></td>
</tr>
<tr>
<td>• Memory wear does not occur</td>
<td></td>
</tr>
</tbody>
</table>
Spin Torque Transfer MRAM: Working

• STT (Spin Torque Transfer) RAM is a next generation MRAM

• STT-RAM uses current flow of spin-coherent electrons to switch the state of the ferromagnet

• Polarised current is achieved using Nano magnets
Advantages and Disadvantages

• Advantages
  • Non-volatile
  • No refresh needed
  • Small cell size
  • High speed read / write
  • Simple architecture
  • Memory wear does not occur

• Removes disadvantages of conventional MRAM
  • Half select problem solved
  • Scalability issue solved
  • Write power about same as read power

• Disadvantages
  • Need for a modern, new technology fab
  • Still has challenges in terms of materials used
Phase Change Memory: Working

- Material: Chalcogenide glass (CG)
  - Usually alloy of Ge, Se, Te in ratio 2:2:5
- Dramatic change in electrical resistance with change in physical state
  - Crystalline (1): Low resistance state
  - Amorphous (0): High resistance state
- Recent memories allow 2 bits of storage per cell:
  - Crystalline (11), Mostly crystalline (10)
  - Mostly amorphous (01), Amorphous (00)
Reading / Writing

• Read:
  Simple resistance measurement

• Write:
  0: CG is heated to high temperature (600°C) and cooled rapidly to get amorphous state
  1: CG is heated above the crystallisation point but below the melting point giving crystalline CG
    • High temperature for quick crystallisation
    • Temperature below melting point to avoid amorphous state CG
Advantages and Disadvantages

Advantages

- Very high speed
- Non-volatile

Disadvantages

- Needs high quality material
- High power consumption
- Temperature sensitive operation
  - device heat-up issue
  - Current leakage through dielectric at high temperature
- Slow cell degradation
Conduction Bridge RAM (CBRAM/PMC)

- Two Electrodes
  - Electrochemically active (Ag, Cu etc.)
  - Relatively inert (W)
- Writing: Positive bias to active electrode
  - Continuous nanowire
  - Deposition Islands
- Erasing: Negative bias to active electrode
- Reading: Resistance measurement

Advantages
- Non-volatile
- Low read / write power
- High speed
- Simple structure
- Easily scalable

Challenge
- The material needs to withstand high temperature to be processed in standard CMOS fabs
FeRAM: Working

• Similar to DRAM (1T-1C)

• Ferroelectric instead of dielectric

• Data is stored as polarity of residual dipole

http://www.spectrum.ieee.org/images/jul08/images/umix01.jpg
Read / Write

- **Write**: Similar to DRAM
  - Voltage of appropriate polarity is applied to capacitor plates
- **Read**: Destructive
  - Voltage of known polarity is applied to the capacitor plates
  - Data is interpreted from presence / absence of current spike
Advantages and Disadvantages

- **Advantages**
  - Non-volatile
  - Density, cost, r/w power similar to DRAM
  - No refresh
  - Faster writes than DRAM
  - High endurance

- **Disadvantages**
  - Destructive read
  - Failure
    - Polarisation fatigue
    - Retention loss
    - Imprint
SONOS

- SONOS: Similar to flash
- Floating poly-S is replaced by nitride
- Disadvantages
  - Electrons get strongly trapped in ONO layer
- Advantages
  - Better interface
  - Nitride is non-conducting leading to better resistance to shorting faults in the oxide
  - Hence, inferior quality oxide acceptable
  - Less number of oxide fabrication steps
  - Less insulation implies more compact
  - Much lower write voltage, no charge pump
  - Faster writes, no write disturb
  - Longer cell life
Millipede: Working

- Data is stored as pits on a thin polymer
- Write: MEMs probe
  - Heat the probe tip above glass transition temperature (GTT) (acrylic glass: 400°C)
  - Dent for 1, pull out for 0 (surface tension)
- Read: Resistance change
  - Heat the probe tip below GTT
  - Rate of cooling depends on data stored
  - Probe has temperature dependent resistance
Advantages and Disadvantages

- Disadvantages
  - High r/w power

- Advantages
  - Very high density
  - Simple structure
  - Parallel r/w
    - Multiple heads
    - High r/w speed
Nano RAM (Nantero)

- **Read**: Resistance Measurement
  - $0 \rightarrow 1$: Electrostatic attraction
    - Van der Waal’s force ($E_a = 5eV$)
  - $1 \rightarrow 0$: Phonon driven
    - Young’s Modulus ($E_a \gg 5eV$)

- **Write**:

- **Advantages**
  - Dense, easily scalable
  - Non-volatile, no refresh
  - Low r/w power
  - Fast r/w
  - Good resistance to external interference
Memristor

- Fourth basic element \( M(Q) = \frac{d\phi_m}{dQ} \)
- \( V = \frac{d\phi_m}{dt} \) and \( I = \frac{dQ}{dt} \) \( \Rightarrow \) \( V = M(q) \cdot I \)
- Resistance depends on charge that has flowed through
- Titanium – Titanium Dioxide – Platinum cell (HP)
  - Movement of oxygen vacancies under applied electric field
- Silicon dioxide based ReRAM (University College of London)
  - Formation of silicon filaments due to applied electric field [1]
- Advantages
  - Lower read/write energy and faster than Flash, non-volatile
- Still in experimental phase
<table>
<thead>
<tr>
<th>Memory Type</th>
<th>Read Access Time</th>
<th>Write Access Time</th>
<th>Data Retention</th>
<th>Cell Area</th>
<th>Scalability</th>
<th>Read Voltage</th>
<th>Write Voltage</th>
<th>Write Energy</th>
<th>R/W Cycles</th>
</tr>
</thead>
<tbody>
<tr>
<td>NAND Flash</td>
<td>110ns / 30ns</td>
<td>2 ms / 0.3ms</td>
<td>&gt;10 years</td>
<td>4</td>
<td>18 nm</td>
<td>2V</td>
<td>15V</td>
<td>10 fJ/bit</td>
<td>1.E+05</td>
</tr>
<tr>
<td>NOR Flash</td>
<td>10ns</td>
<td>1 µs / 10 ms</td>
<td>&gt;10 years</td>
<td>10</td>
<td>18 nm</td>
<td>2V</td>
<td>12V</td>
<td>10 fJ/bit</td>
<td>1.E+05</td>
</tr>
<tr>
<td>SRAM</td>
<td>0.4ns</td>
<td>0.4ns</td>
<td>ON</td>
<td>120</td>
<td>13 nm</td>
<td>1.1V</td>
<td>1.1V</td>
<td>0.7 fJ/bit</td>
<td>1.E+16</td>
</tr>
<tr>
<td>DRAM</td>
<td>30ns</td>
<td>30ns</td>
<td>64ms</td>
<td>6</td>
<td>15-20 nm</td>
<td>2V</td>
<td>2V</td>
<td>5 fJ/bit</td>
<td>1.E+16</td>
</tr>
<tr>
<td>MRAM</td>
<td>20 ns</td>
<td>20 ns</td>
<td>&gt;10 years</td>
<td>15-20</td>
<td>90 nm</td>
<td>1.5V</td>
<td>1.5V</td>
<td>70 pJ/bit</td>
<td>1.E+16</td>
</tr>
<tr>
<td>PCRAM</td>
<td>60ns</td>
<td>50ns</td>
<td>&gt;10 years</td>
<td>5</td>
<td>18 nm</td>
<td>3V</td>
<td>3V</td>
<td>5 pJ/bit</td>
<td>1.E+08</td>
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<tr>
<td>FeRAM</td>
<td>45ns</td>
<td>10ns</td>
<td>&gt;10 years</td>
<td>20-25</td>
<td>65nm</td>
<td>1-3V</td>
<td>1-3V</td>
<td>30 fJ/bit</td>
<td>1.E+14</td>
</tr>
<tr>
<td>NAND SONOS</td>
<td>*</td>
<td>100-150 ns</td>
<td>&gt;10 years</td>
<td>4</td>
<td>18 nm</td>
<td>2V</td>
<td>5-8V</td>
<td>3-5 fJ/bit</td>
<td>1.E+09</td>
</tr>
<tr>
<td>NOR SONOS</td>
<td>*</td>
<td>50 ns</td>
<td>&gt;10 years</td>
<td>10</td>
<td>18 nm</td>
<td>2V</td>
<td>5-8V</td>
<td>3-5 fJ/bit</td>
<td>1.E+09</td>
</tr>
<tr>
<td>STTRAM</td>
<td>20ns</td>
<td>20ns</td>
<td>&gt;20 years</td>
<td>10</td>
<td>50 nm</td>
<td>0.7V</td>
<td>1V</td>
<td>4 fJ/bit</td>
<td>1.E+12</td>
</tr>
<tr>
<td>STTRAM</td>
<td>20ns</td>
<td>20ns</td>
<td>&gt;20 years</td>
<td>6</td>
<td>7-10 nm</td>
<td>&lt;0.5V</td>
<td>1V</td>
<td>0.1 pJ/bit</td>
<td>1.E+16</td>
</tr>
<tr>
<td>CBRAM</td>
<td>100ns</td>
<td>50ns</td>
<td>&gt;10 years</td>
<td>(1.4)</td>
<td>180nm</td>
<td>1.6V</td>
<td>1.6V</td>
<td>NA</td>
<td>1.E+06</td>
</tr>
<tr>
<td>CBRAM</td>
<td>10ns</td>
<td>10ns</td>
<td>&gt;10 years</td>
<td>(1.4)</td>
<td>10nm</td>
<td>0.5V</td>
<td>0.5V</td>
<td>(0.1 fJ/bit)</td>
<td>1.E+16</td>
</tr>
<tr>
<td>NRAM</td>
<td>3 ns</td>
<td>3 ns</td>
<td>~days</td>
<td>10</td>
<td>&lt;65 nm</td>
<td>1.5V</td>
<td>1.5V</td>
<td>NA</td>
<td>1.E+12</td>
</tr>
<tr>
<td>NRAM</td>
<td>3 ns</td>
<td>3 ns</td>
<td>&gt;10 years</td>
<td>5</td>
<td>5-10 nm</td>
<td>0.7V</td>
<td>1.5V</td>
<td>NA</td>
<td>1.E+16</td>
</tr>
<tr>
<td>Millipede</td>
<td>0.1-1 ms **</td>
<td>0.1-1ms **</td>
<td>&gt;10 years</td>
<td>4</td>
<td>10 nm</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
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<td>Millipede</td>
<td>0.1-1 ms **</td>
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<td>4</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

*Similar to flash; **Inadequate data; Red - Projected

Current Status...

- **Conventional MRAM**
  - In production, size 64Mb or less
- **STT-RAM**
  - Prototype phase, size 2Mb or less
- **Phase Change Memory**
  - February 2012: Samsung presented 20nm 1.8V 8Gb PRAM [16]
  - July 2012: Micron announced availability of Phase-Change Memory for mobile devices - the first PRAM solution in volume production [17]
- **Conductive Bridge RAM/Program Metallization Cell**
  - Experimental stages
- **FeRAM**
  - FeRAMs are produced in line widths of 350 nm at Fujitsu and 130 nm at Texas Instruments (2007)
...Current Status

- **SONOS**
  - Philips is one of the groups working on SONOS devices, [18] and have produced small 26-bit demonstrators with excellent lifetimes at a 120 nm line width

- **Millipede**
  - Experimental stage

- **Nano RAM (NRAM)**
  - Nano-RAM is a proprietary computer memory technology from the company Nantero
  - Second generation of NRAM is currently in production

- **Due to heavy investments in Flash and other types of conventional memories (including specially designed fabs), new technologies memories have not been able to replace the conventional ones, so far.**
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