Assessing circuit design parameters for lower-power clinically-viable intracortical brain-computer interfaces

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***Abstract* — Clinically-viable intracortical brain-computer interfaces (iBCIs) require a large number of recording electrodes, amplifiers and ADCs, as well as wireless communication for transcutaneous real-time data transfer. This requires power which is a limited resource for any implantable system. For implantable neural devices, such as iBCI, power saving is even more crucial since heat is also a major concern. iBCI designs typically focus on providing high performance and robustness, but this can lead to inadvertent over-design at the expense of power consumption. Here we ask, how to consider designing nearly as high performance and high robustness iBCI, which is still clinically viable, but consumes considerably less power. We base this design assessment on our experimental iBCI measurements in rhesus macaque. Our findings suggest that design parameters can be relaxed considerably, thereby reducing power consumption by up to two orders of magnitude compared to conventional iBCI designs.**

I. Introduction

iBCIs recording from motor cortex have shown promising results in FDA pilot clinical trials in people with paralysis (e.g., [1]). There is considerable industrial and academic interest in advancing all aspects of iBCI design, and here we focus on two: (1) the increasing requirements for analog front ends (AFEs) and ADCs for the dramatic scale-up happening in the number of recording electrodes (thousands or more), and (2) the increasing bandwidth requirements placed on implantable wireless data-transmission circuits. These increasing requirements typically require larger circuits with higher power consumption.

Current iBCIs record and transmit wide-bandwidth signals with high resolution, which enables the use of a variety of signals including action potentials (spikes) which are used in the highest-performing systems. However, in recent years, most iBCIs operating on spikes merely perform a (1 bit) thresholding operation (e.g., at -4.5 RMS) as the decoded information loss is ~5% (e.g., [1,2]). This is as opposed to neural measurements for basic science which requires low noise, high-speed sampling, high quantizer resolution, and low bit-error rate (BER) of the transmitter, all of which contribute to the power budget.

Here, we evaluate neural signals from our iBCI experiments in rhesus macaque to assess which design specifications might be relaxed without sacrificing substantial performance.

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II. Results

We assessed gold-standard data from our lab and found that a standard iBCI Kalman-filter decoder (for clinical applications), which predicts the animal's hand movements, is robust to noise. It was robust to spikes error (accidental detection or miss of a spike in a given ms bin) rates of up to 10^{-2} (much lower than the common BER of the communication systems, e.g., < 10^{-4}) which resulted in minimal performance decline (less than ~ 7%).

Next, we assessed the iBCI decoder robustness to the four main AFE and ADC specifications: the filtered frequency band (f_0 and f_1), the input referred noise ($V_{in,rms}$), the sampling frequency (f_s) and the bit resolution (B). Analysis and simulation revealed that iBCI performance can be sustained also when the parameters are loosened dramatically (Table 1). These new relaxed specifications reduce the total power consumption (AFE, ADC and transmitter) by over two orders of magnitude compared with a conventional (over-designed) system. The proposed system is now power limited by the first block in the acquisition chain (AFE - 68%) as opposed to the last one in conventional systems (transmitter - 67%), which is usually a symptom of a highly optimized acquisition chain.

Parameters	***Conventional***	***Proposed***
$V_{in,rms}$	1-5 μV_{rms}	5-10 μV_{rms}
f_0	<1 Hz	0.5-1 kHz
f_1	5-10 kHz	1-4 kHz
f_s	15-30 kHz	3-12 kHz
B	10-16 bit	4-8 bit

Table 1: Conventional and proposed neural interface parameter comparison.

III. Conclusion

Our findings suggest that iBCIs for clinical use can consume substantially less power than what a basic-science influenced (i.e., over-designed) iBCI might use. Minimizing power is critical in the face of the necessary exponential increase in the number of recording electrodes that is underway. If designs motivated by this assessment are implemented and validated in real-world iBCI experiments, this could meaningfully increase the clinical-viability of iBCIs aimed at helping millions of people suffering from a wider range of neurological diseases and disorders.

References

[1] C. Pandarinath *et al.*, "High performance communication by people with paralysis using an intracortical brain-computer interface," *Elife*, 6:e18554, 2017.

[2] B. Christie *et al.*, "Comparison of spike sorting and thresholding of voltage waveforms for intracortical brain-machine interface performance ," *J. Neural Eng.*, 12:006019, 2015.