High-Temperature Stability of Refractory-Metal VLSI GaAs MESFET's

Krishna V. Shenoy, Clifton G. Fonstad, Jr., and James M. Mikkelson

***Abstract*— Commercially available, self-aligned VLSI GaAs MESFET's, with tungsten-based refractory-metal Schottky gates, nickel-based refractory-metal ohmic contacts, and aluminum interconnection metallization, have been thermally cycled and shown to be stable after 3 h at temperatures up to 500°C. Both partially processed and fully processed wafers were found to be stable with no significant change occurring in either Schottky gate or ohmic contact properties. An increase in the channel resistance component of the series resistance is believed to be responsible for I_{DS} and g_m degradation above 500°C. The fact that commercially available, gold-free VLSI GaAs MESFET's are able to withstand such thermal cycles has very important consequences for monolithic optoelectronic integrated circuit (OEIC) fabrication because it means that it may now be feasible to grow photonic device heterostructures epitaxially on MESFET VLSI wafers; process them into lasers, modulators, and/or detectors; and interconnect them with the electronics to produce VLSI-density OEIC's.**

I. Introduction

Commercially available VLSI GaAs metal semiconductor field effect transistors (MESFET's) are potentially very useful as the starting point in the realization of high density, high performance optoelectronic integrated circuits (OEIC's) [1]. In recent years GaAs integrated circuits have attained VLSI levels of integration and the technology has evolved with the replacement of gold-based contacts and earlier Schottky gate metals by refractory metal gates and nickel-based contacts which promise much better high temperature stability [2]. Direct epitaxy of photonic devices on fully processed MESFET circuitry with dielectric windows may now be a viable approach to fabricating monolithic OEIC's if these new circuits are thermally stable at elevated temperatures [3]–[5]. In this letter, we examine the performance of commercial refractory-metal VLSI GaAs MESFET's after high-temperature anneals which correspond to the thermal cycles encountered during the molecular beam epitaxial (MBE) growth of an in-plane surface-emitting laser heterostructure.

II. Experimental Results and Discussions

Vitesse Semiconductor Corporation HGaAs2 technology, a self-aligned VLSI GaAs MESFET process with tungsten-based refractory-metal Schottky gates, nickel-based refractory-metal ohmic contacts, and aluminum interconnection metallization, was selected for this study [6]. 50 μm × 1.2 μm gate enhancement mode MESFET's (EFET's), 10 μm × 1.2 μm gate depletion mode MESFET's (DFET's), and transmission line model (TLM) structures with 100 μm × 250 μm contact windows spaced at both 5 μm and 10 μm were selected from standard production process control monitor test bars located in the kerfs. Partially processed wafers (with neither aluminum interconnection nor passivation dielectric deposited) as well as fully processed wafers were tested.

Eight electrical tests were performed both before and after thermal anneal cycles. MESFET threshold voltage (V_T), drain-source saturation current (I_{DS}^{sat}), maximum transconductance (g_m), and series resistance (R_s) were extracted for both the EFET's and the DFET's. Forward biased I–V Schottky diode ideality and barrier heights were extracted from the DFET's. Ohmic contact resistances (R_C) from ohmic metal to n^+ ion-implanted source/drains (S/D), and S/D sheet resistances (R_{SH}) were extracted from the TLM structures.

The furnace anneals were conducted in a quartz tube sealed with end-caps in an ambient of atmospheric pressure purified hydrogen (in the case of the partially processed wafers) or nitrogen (in the case of the fully processed wafers). The wafers were ramped from room temperature to the maximum temperature in 0.5 h, maintained at the maximum temperature for 3.0 h, and then ramped back to room temperature in 1.0 h. These times correspond to a 3.0 μm MBE laser growth sequence. The maximum temperature was varied between 400°C (highest previously reported thermally stable MESFET temperature) and 600°C (typical AlGaAs MBE growth temperature).

Two chips diced from a partially processed wafer and two chips from a fully processed wafer were annealed at each temperature. Figs. 1–4 illustrate the thermal stability of MESFET's on a fully processed GaAs wafer. The average of the measured values is plotted. The "Pre-Anneal" point represents the measured value before the thermal cycle and is averaged over all chips. EFET and DFET parameter trends are in agreement; the partially processed wafer trends are similar to the fully processed wafer trends but are less pronounced.

Fig. 1 shows the contact resistivity as measured from the fully processed TLM test structures after 3 h anneals at temperatures between 400°C and 600°C. The pre-anneal contact resistivity is represented as the point at 30°C. A significant increase is seen for anneal temperatures above 550°C. Similar results have recently been reported for graded InGaAs contact

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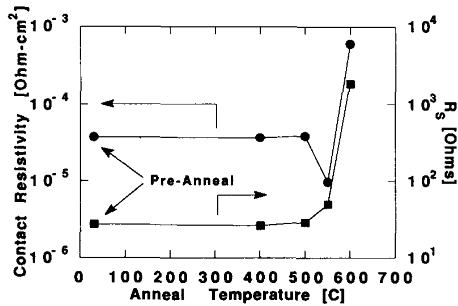

Fig. 1. The contact resistivity (•) as measured from fully processed TLM test structures (100 μm × 250 μm contact windows with 5 μm and 10 μm spaces) after 3 h anneals at temperatures between 400°C and 600°C. A significant increase is seen for anneal temperatures above 550°C. Also the series resistance, R_S (■), of fully processed 50 μm × 1.2 μm gate enhancement-mode MESFET's after 3 h anneals at temperatures between 400°C and 600°C. A significant increase is seen for anneal temperatures above 500°C.

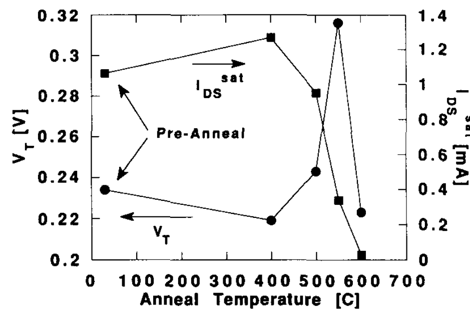

Fig. 2. The threshold voltage, V_T (•), and drain-source saturation current, I_{DS}^{sat} (■) (V_{GS} = 0.5 V, V_{DS} = 1.0 V), of fully processed 50 μm × 1.2 μm gate enhancement-mode MESFET's after 3 h anneals at temperatures between 400°C and 600°C. A moderate V_T increase and a significant I_{DS}^{sat} decrease is seen for anneal temperatures above 500°C.

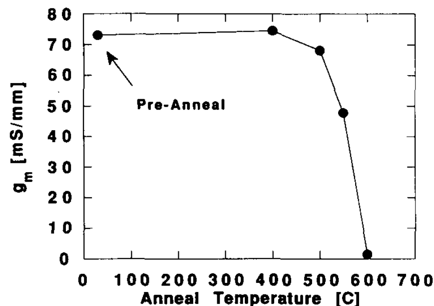

Fig. 3. The maximum transconductance, g_m (V_{DS} = 0.15 V), of fully processed 50 μm × 1.2 μm gate enhancement-mode MESFET's after 3 h anneals at temperatures between 400°C and 600°C. A significant decrease is seen for anneal temperatures above 500°C.

structures with multilayered TiW/Si metallization and a top Au cap [7].

Fig. 1 also shows the series resistance, R_S, of fully processed 50 μm × 1.2 μm gate enhancement-mode MESFET's after 3 h anneals at temperatures between 400°C and 600°C. A significant increase is seen for anneal temperatures above 500°C. R_S is the sum of the channel resistance, source implant

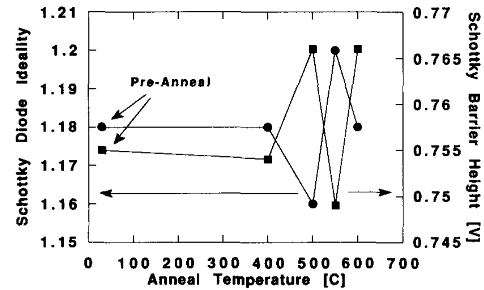

Fig. 4. The Schottky diode ideality (•) and Schottky barrier height (■) of fully processed 10 μm × 1.2 μm gate depletion-mode MESFET's after 3 h anneals at temperatures between 400°C and 600°C. Moderate shifts are seen for anneal temperatures above 400°C.

sheet resistance, and ohmic contact resistance. The source implant sheet resistance shows no significant shifts. The ohmic contact resistance is approximately 1 Ω with less than a 2 Ω increase for the 600°C anneal, which is roughly 0.1% of R_S. Therefore the R_S increase can be primarily attributed to an increase in the channel resistance component. Decreased I_{DS}^{sat} and g_m are expected because R_S acts as a voltage divider and suppresses the Schottky gate voltage.

Fig. 2 shows the threshold voltage, V_T, and drain-source saturation current, I_{DS}^{sat} (V_{GS} = 0.5 V, V_{DS} = 1.0 V), of fully processed 50 μm × 1.2 μm gate enhancement-mode MESFET's after 3 h anneals at temperatures between 400°C and 600°C. A moderate V_T increase (a typical one sigma process variation is 0.02 V) and a significant I_{DS}^{sat} decrease is seen for anneal temperatures above 500°C. Calculated values of I_{DS}^{sat}, using measured values of R_S, are in excellent agreement with experimental values.

Fig. 3 shows the maximum transconductance, g_m (V_{DS} = 0.15 V), of fully processed 50 μm × 1.2 μm gate enhancement-mode MESFET's after 3 h anneals at temperatures between 400°C and 600°C. A significant decrease is seen for anneal temperatures above 500°C. Calculated values of g_m, using measured values of R_S, are in excellent agreement with experimental values.

Fig. 4 shows the Schottky diode ideality and Schottky barrier height of fully processed 10 μm × 1.2 μm gate depletion-mode MESFET's after 3 h anneals at temperatures between 400°C and 600°C. Moderate shifts are seen for anneal temperatures above 400°C.

III. Conclusions

Commercially available, self-aligned VLSI GaAs MESFET's, with tungsten-based refractory-metal Schottky gates, nickel-based refractory-metal ohmic contacts, and aluminum interconnection metallization, have been thermally cycled and shown to be stable after 3 h at temperatures up to 500°C. Both partially processed and fully processed wafers were shown to be stable with no significant change in Schottky gate or ohmic contact properties. An increase in the channel resistance component of the gate-source series resistance is believed to be responsible for I_{DS} and g_m degradation above 500°C. Clearly, a detailed investigation of the critical 500°C to

550°C temperature range is warranted and work is currently in progress.

Most GaAs-based lasers are grown at temperatures in excess of 600°C, but there have been a number of recent reports of excellent lasers grown at 500°C and below [1], [3], [8]–[10]. The fact that commercially available, gold-free VLSI GaAs MESFET's are able to withstand such thermal cycles means that it may now be feasible to grow photonic device heterostructures epitaxially on MESFET VLSI wafers; process them into lasers, modulators, and/or detectors; and interconnect them with the electronics to produce VLSI-density OEIC's.

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