A New Method for Design of Robust Digital Circuits

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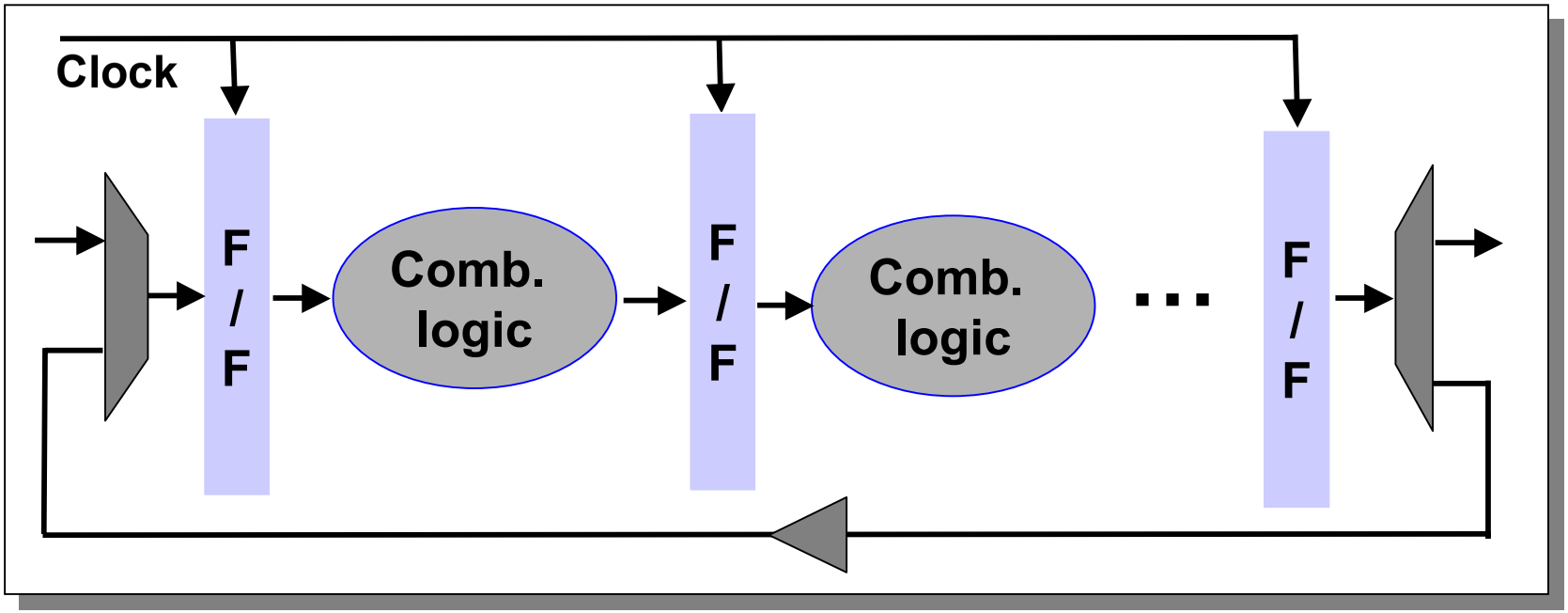
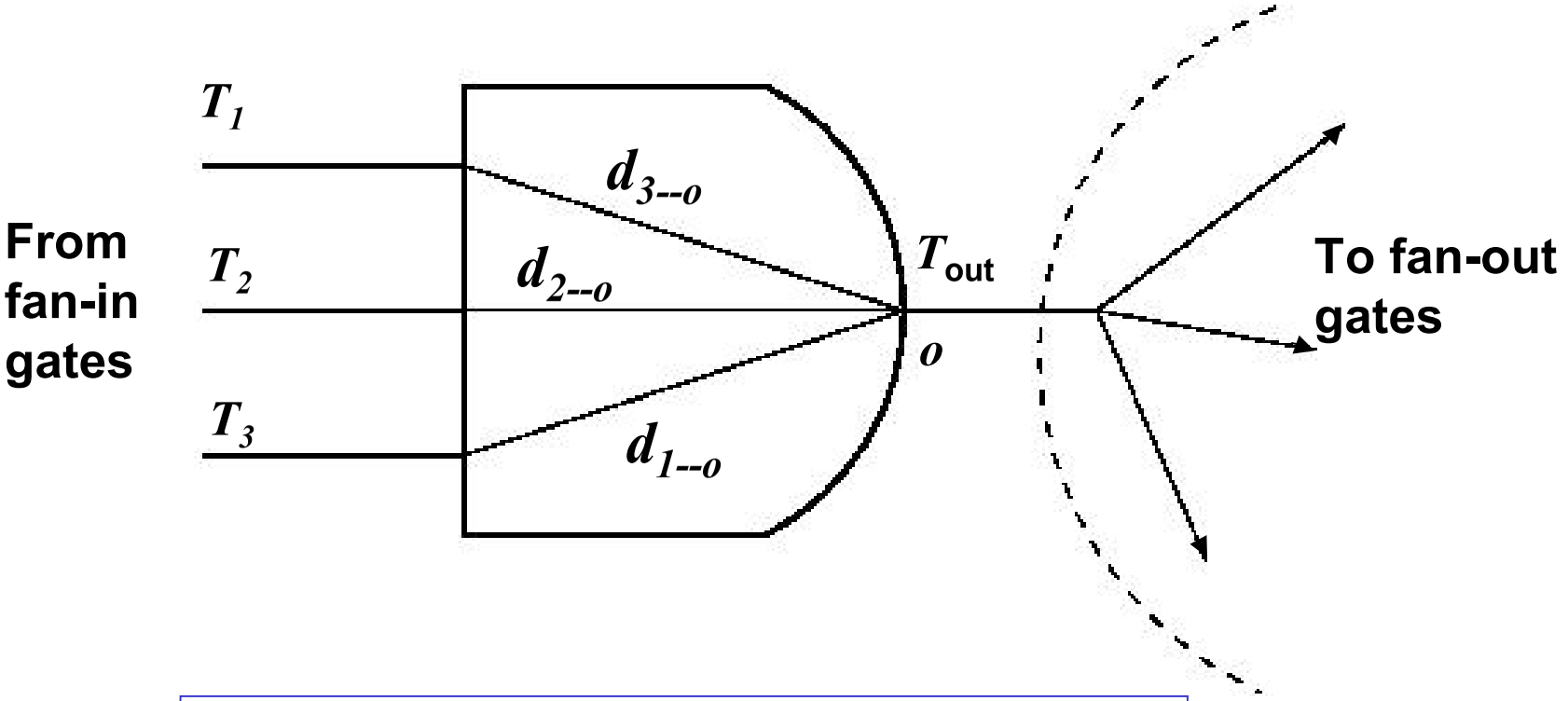
Digital circuit design constraints



- Every logic block has to meet the clock cycle
- Area/power constraint
- Signal integrity constraints, min/max size constraints etc.

Delay propagation in a typical gate



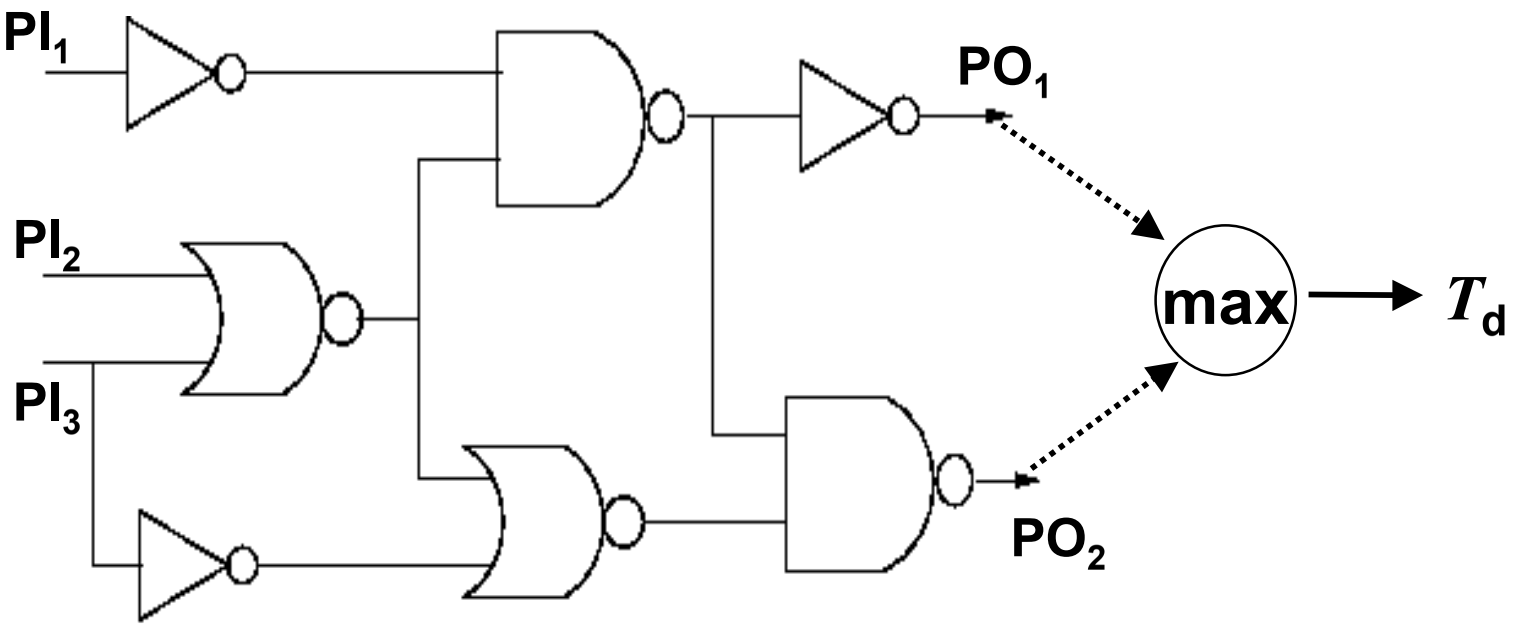
$d_{i—o}$ = delay from input i to output o

$$T_{\text{out}} = \max_{i=1,2,3} (T_i + d_{i-o})$$

Sizing for delay minimization

- Goal – Minimize the circuit delay T_d,

  under area, slope, and other constraints



Deterministic circuit sizing problem

$$d_{i-o} = \mu_i(w, C_L, V_{dd}, V_{th}, \ldots)$$

w = vector of device sizes & μ = mean delay function

minimize : $T_d(w)$

subject to : $\sum w_i \leq A$

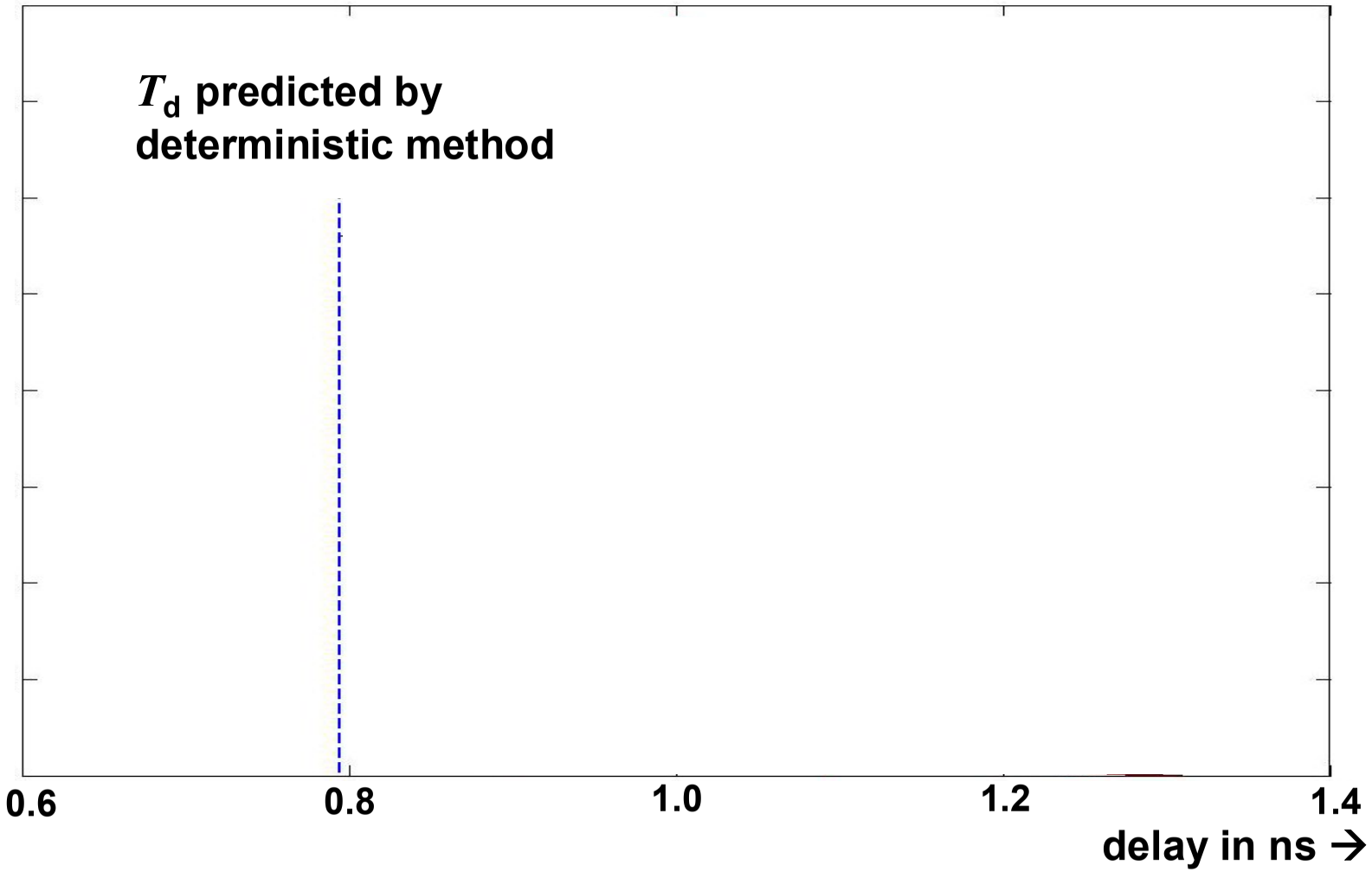
$W_{min} \leq w_i \leq W_{max}$

slew constraints

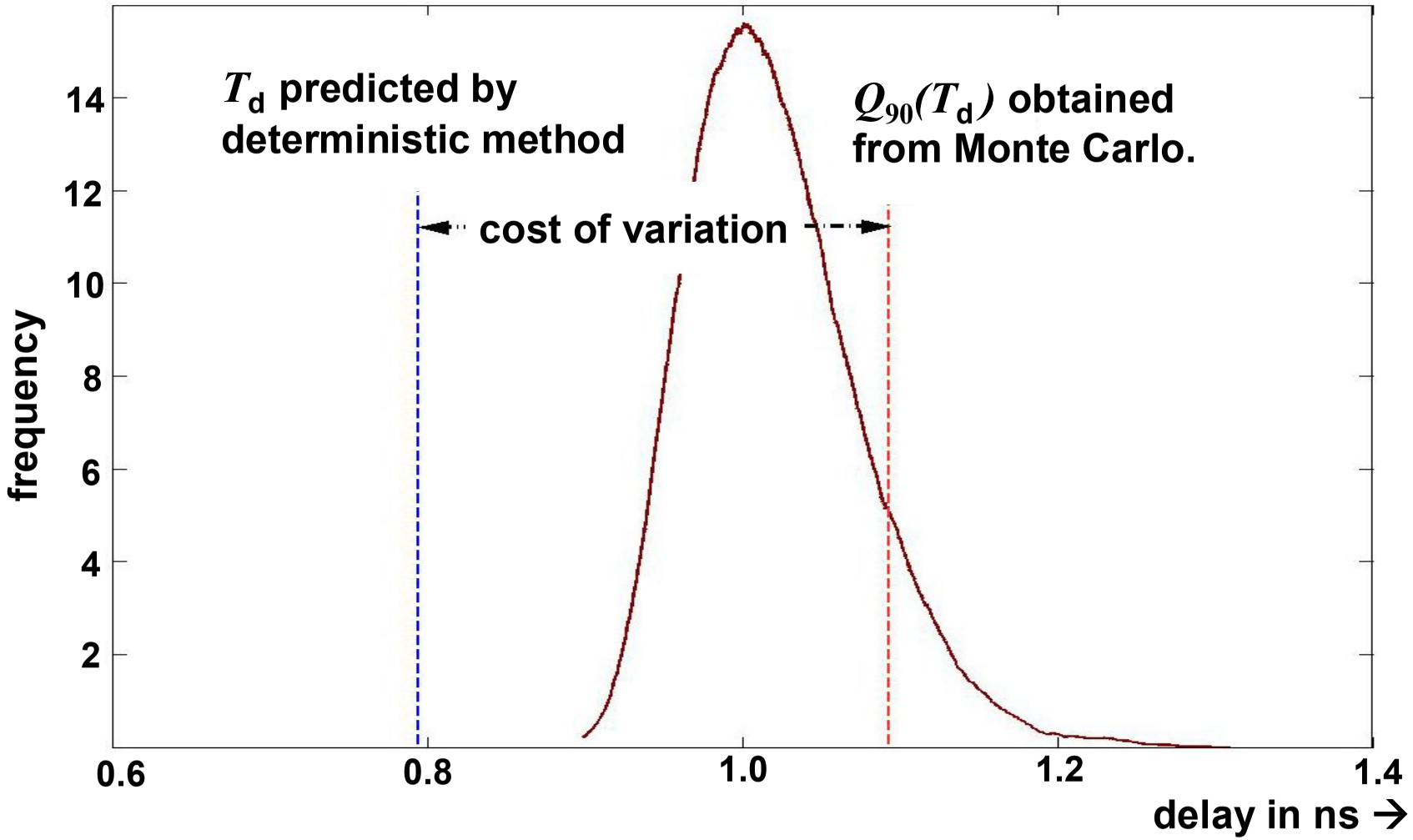
$\vdots$

Design example: 32-bit adder

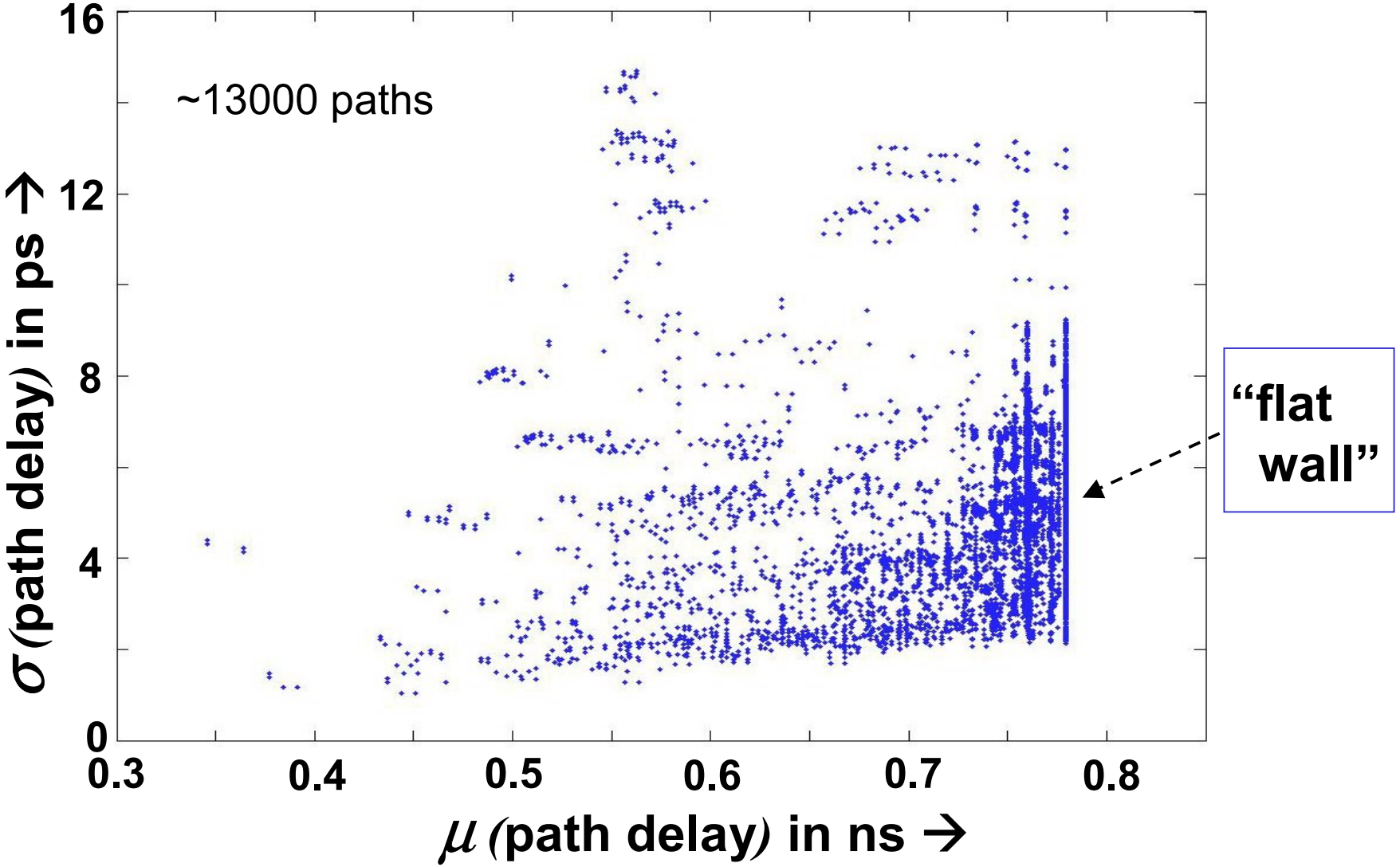
Nominal delay for deterministic adder sizing



Delay PDF for deterministic 32-bit adder sizing



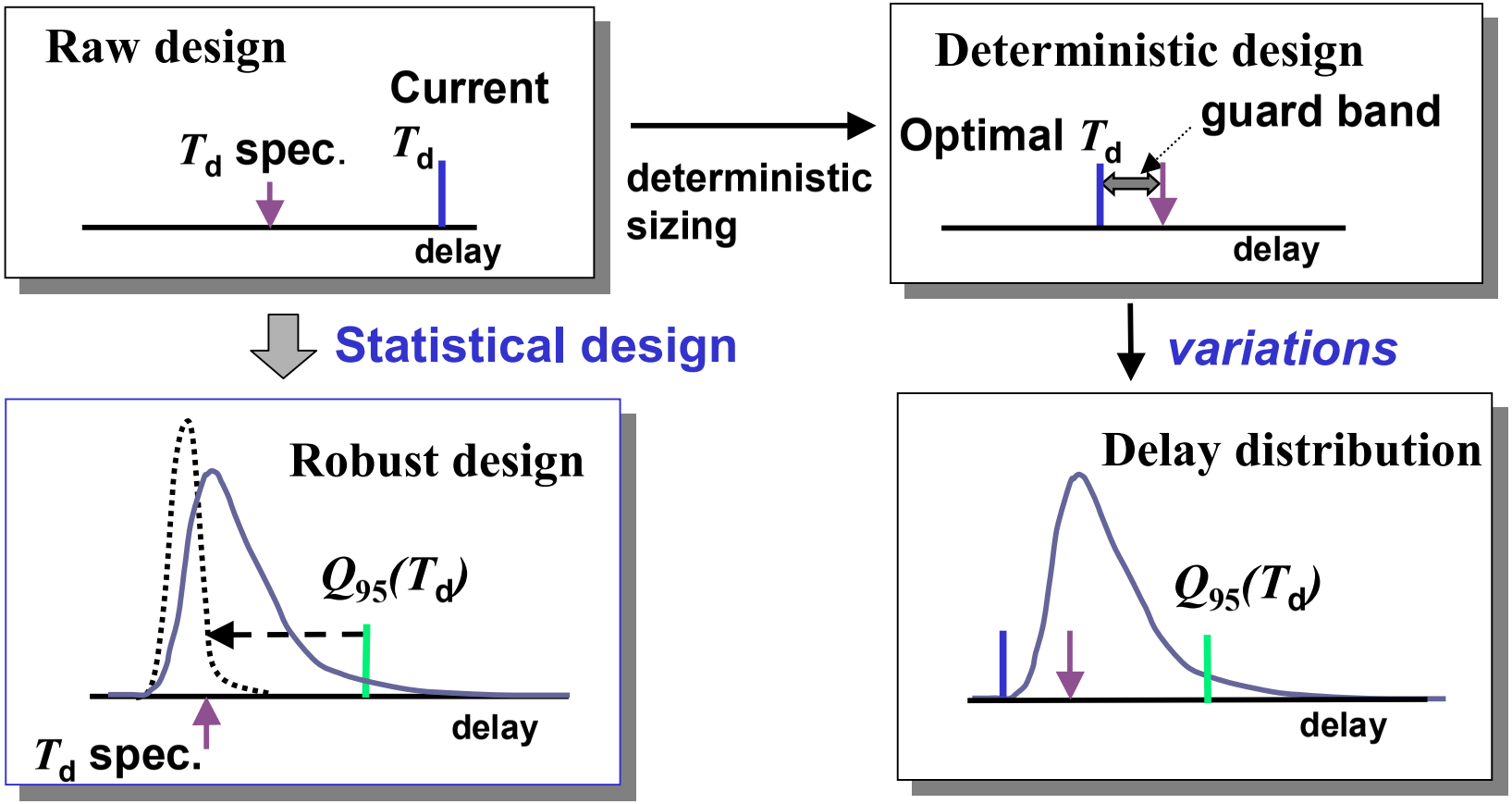
Path delay μ – σ scatter plot for a 32-bit adder



Outline

- Circuit sizing
- Sizing for robust design
  - Augment gate delay with σ margins
  - Use “soft maximum” at converging nodes
- Results
- Conclusions

Objective


Raw design
Current
T_d spec.
T_d
delay
deterministic
sizing
Deterministic design
Optimal T_d
guard band
delay
Statistical design
variations
Robust design
$Q_{95}(T_d)$
delay
T_d spec.
Delay distribution
$Q_{95}(T_d)$
delay

Exact statistical delay minimization problem

- R.V. $d_{i-o} \sim F_i(w, C_{\mathrm{L}}, V_{\mathrm{dd}}, V_{\mathrm{th}}, \ldots)$
- **Propagate symbolic PDFs through netlist**
  → Network Q_{95} constraints (How?)

minimize : $Q_{95}(T_{\mathrm{d}}(w))$

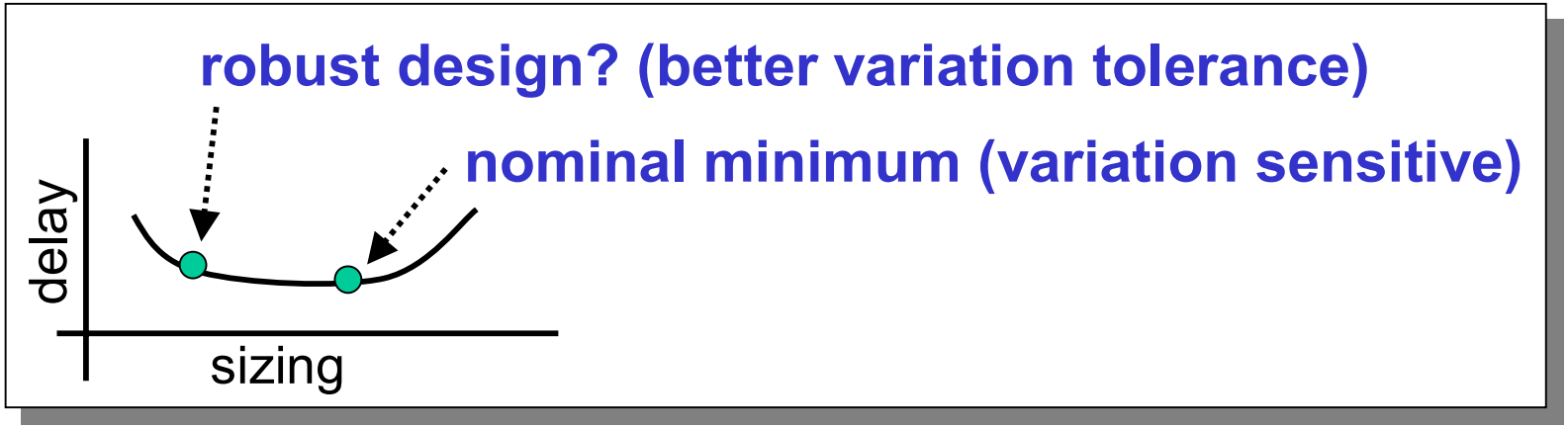
subject to : $\sum w_i \leq A$

⋮

A (very) difficult problem!

Basic intuition

- Sizing problems have a relatively large flat minimum
- The sizer mostly needs to avoid making bad choices



- How to approximately propagate Q_{95} of net timings?

Merits of deterministic circuit sizing

$$d_{i-o} = \mu_i(w, C_L, V_{dd}, V_{th}, \ldots)$$ ***posynomial functions***

w = vector of device sizes & μ = mean delay function

minimize : $T_d(w)$

subject to : $\sum w_i \leq A$

$W_{min} \leq w_i \leq W_{max}$

slope constraints

⋮

Can be formulated as a GGP*

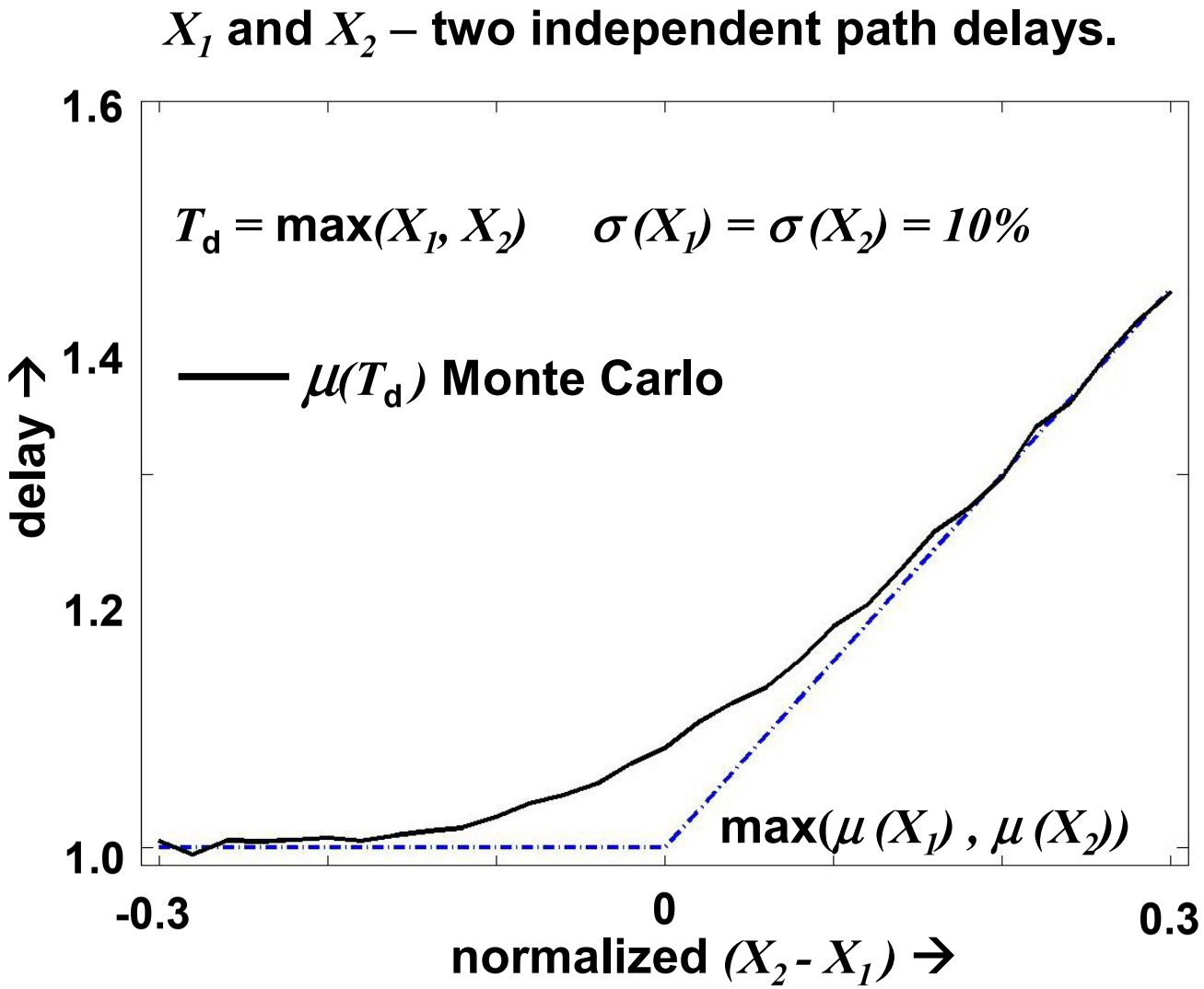
(* S. Boyd *et. al.*, "A tutorial on Geom. Prog.", www.stanford.edu/~boyd/gp_tutorial.html)

Statistical technique (1)

Statistical technique (1)	Deterministic design	Robust design
Augment the mean delay using σ margins	**Gate delay =** $\mu(d_{i-o})$ No variation included	**Gate delay =** $D_{i-o} = \mu(d_{i-o}) + k_j \sigma(d_{i-o})$ k_j = margin coefficient for gate j

- **k_j provides tradeoff between mean and variance at the gate level**

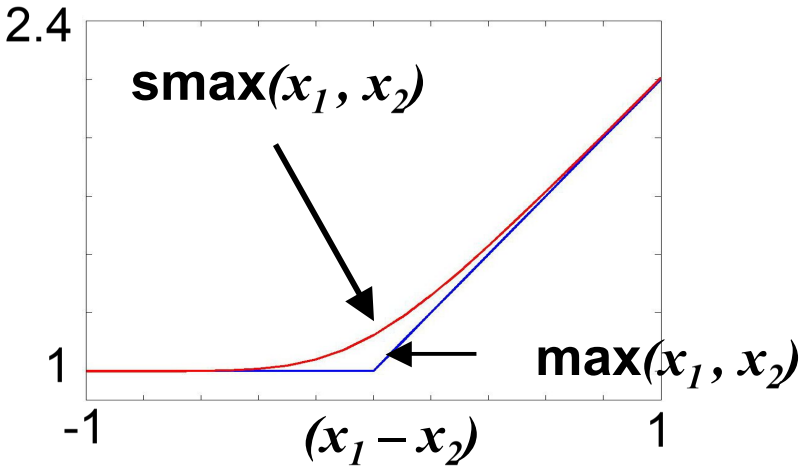
Statistical max function



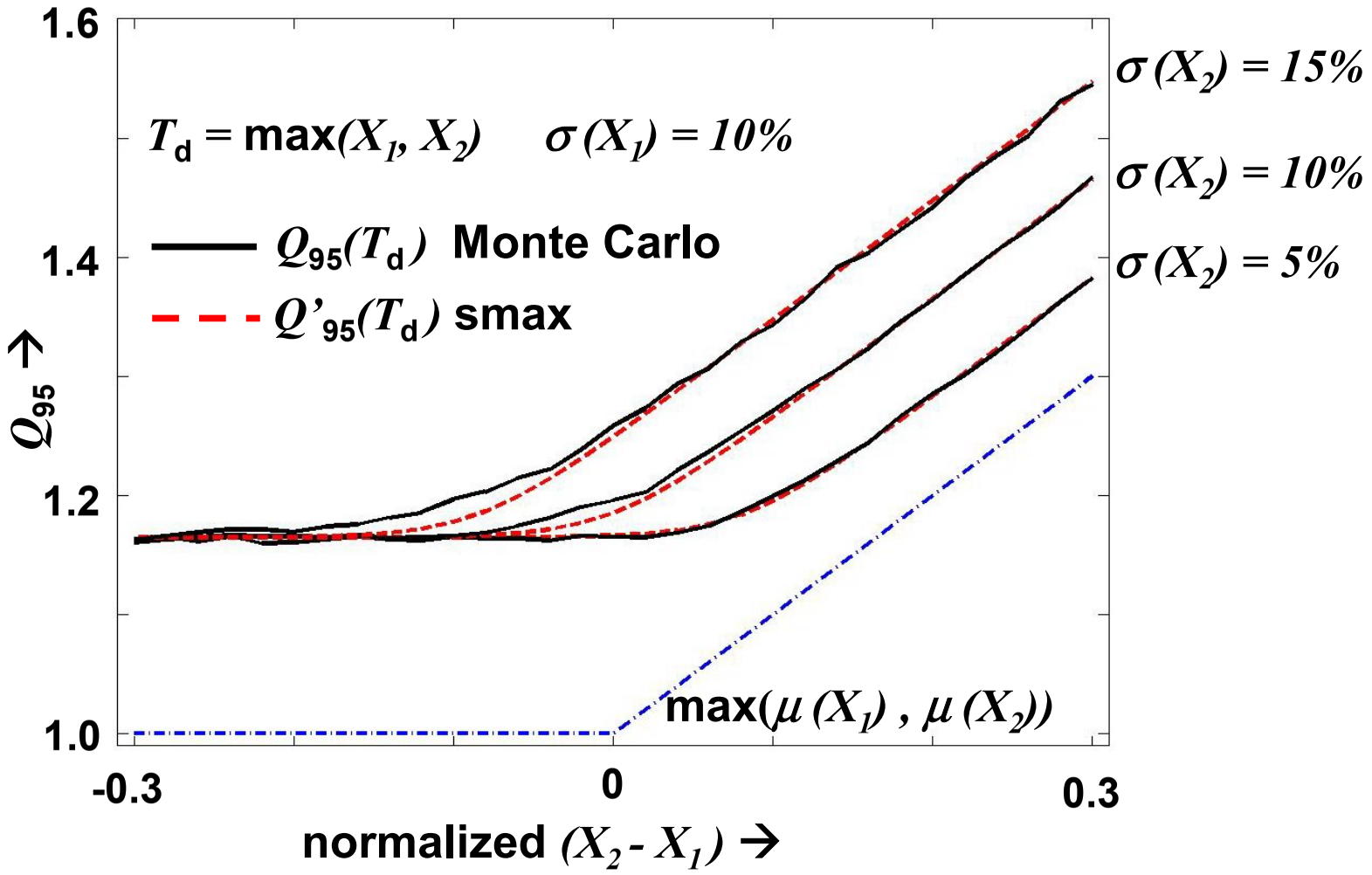
Statistical technique (2)

Statistical technique (2)	Deterministic Design	Robust Design
Use "soft max" to combine path delays at converging nodes	$T_{\text{out}} = \max_{i \in (inputs)} (T_i + d_{i-o})$	$T_{\text{out}} = \underset{i \in (inputs)}{\text{smax}}(T_i + D_{i-o})$ **p = penalty for closeness of converging paths**

$$\text{smax} = \left(\sum | x_i |^p \right)^{1/p}$$



Effect of the two techniques



Algorithm

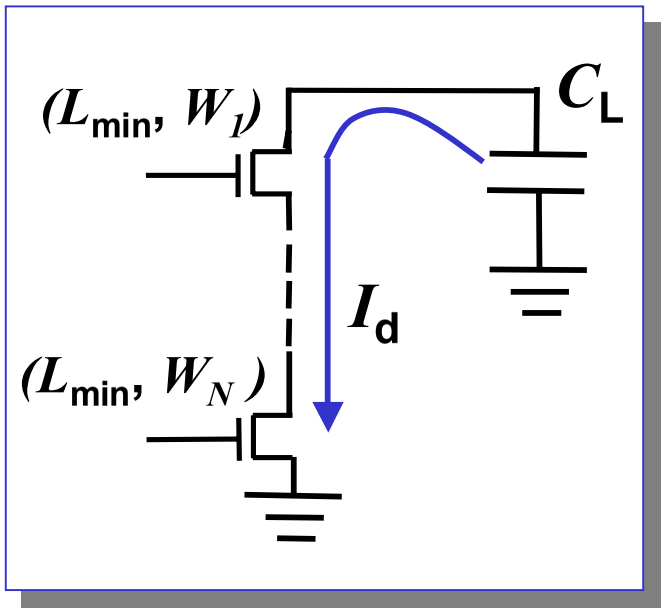
- Modify the deterministic method to include the two statistical techniques
- Get multiple optimized designs at various points in the $k - p$ space
- Perform SSTA and choose the best design

- Typical values: $k \in [0.5\ ,\ 2.5]$ and $p \in [30\ ,\ 50]$
- For simplicity k and p *are* uniform for all gates
- We observed that $Q_{95}(T_d)$ is a weak function of k and p

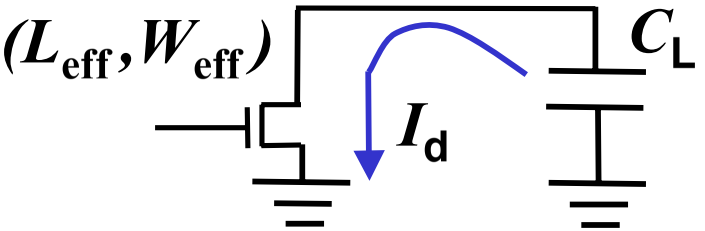
  $\therefore$ Granularity of $k - p$ space is $(0.5,\ 5)$

Gate delay model

- Chain of N transistors $\Rightarrow$ Equivalent transistor
- Velocity saturated devices, can't combine as resistors!



$\Rightarrow$



$$W_{\text{eff}} = \min(W_1, \ldots, W_N)$$

$$L_{\text{eff}} = L_{\min} W_{\text{eff}} \sum_{i=1}^{N} \frac{1}{W_i}$$

Statistical delay model

- Using Pelgrom's model for variation of I_d we can write:

$$\frac{\sigma(I_d)}{I_d} \propto \frac{1}{\sqrt{W_{\text{eff}} L_{\text{eff}}}}$$ for a chain of N transistors

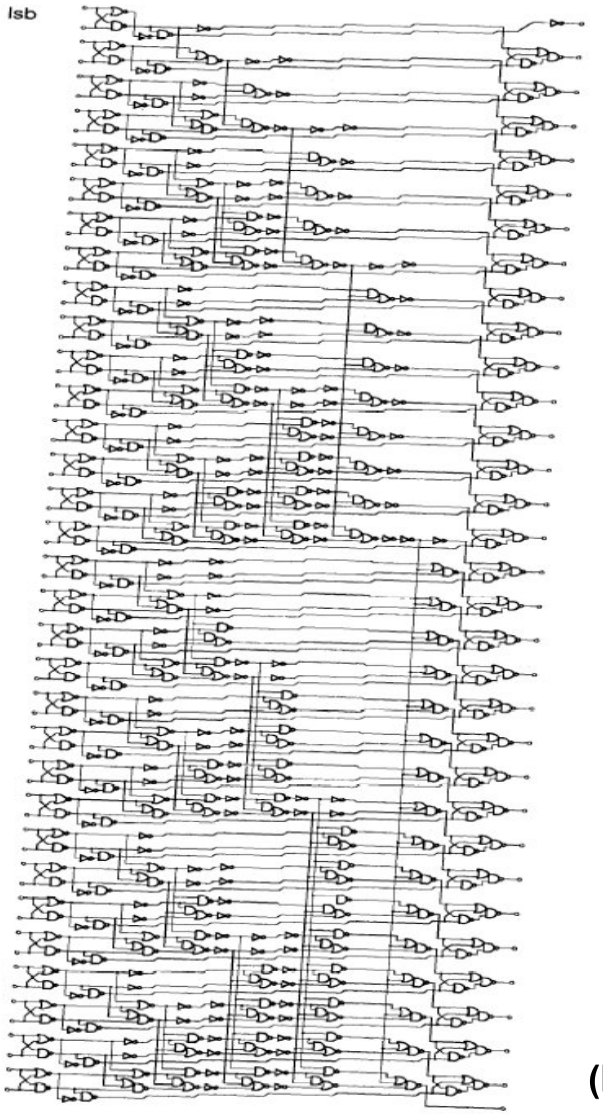
- Variation in the delay of the transistor chain (τ_d) is:

$$\sigma(\tau_d) = \frac{\partial \tau_d}{\partial I_d} \sigma(I_d)$$ to first order

Outline

- Motivation
- Sizing for robust design
  - Augment gate delay with σ margins
  - Use “soft maximum” at converging nodes
- **Results**
- Conclusions

Design example: Ladner-Fisher 32-bit adder

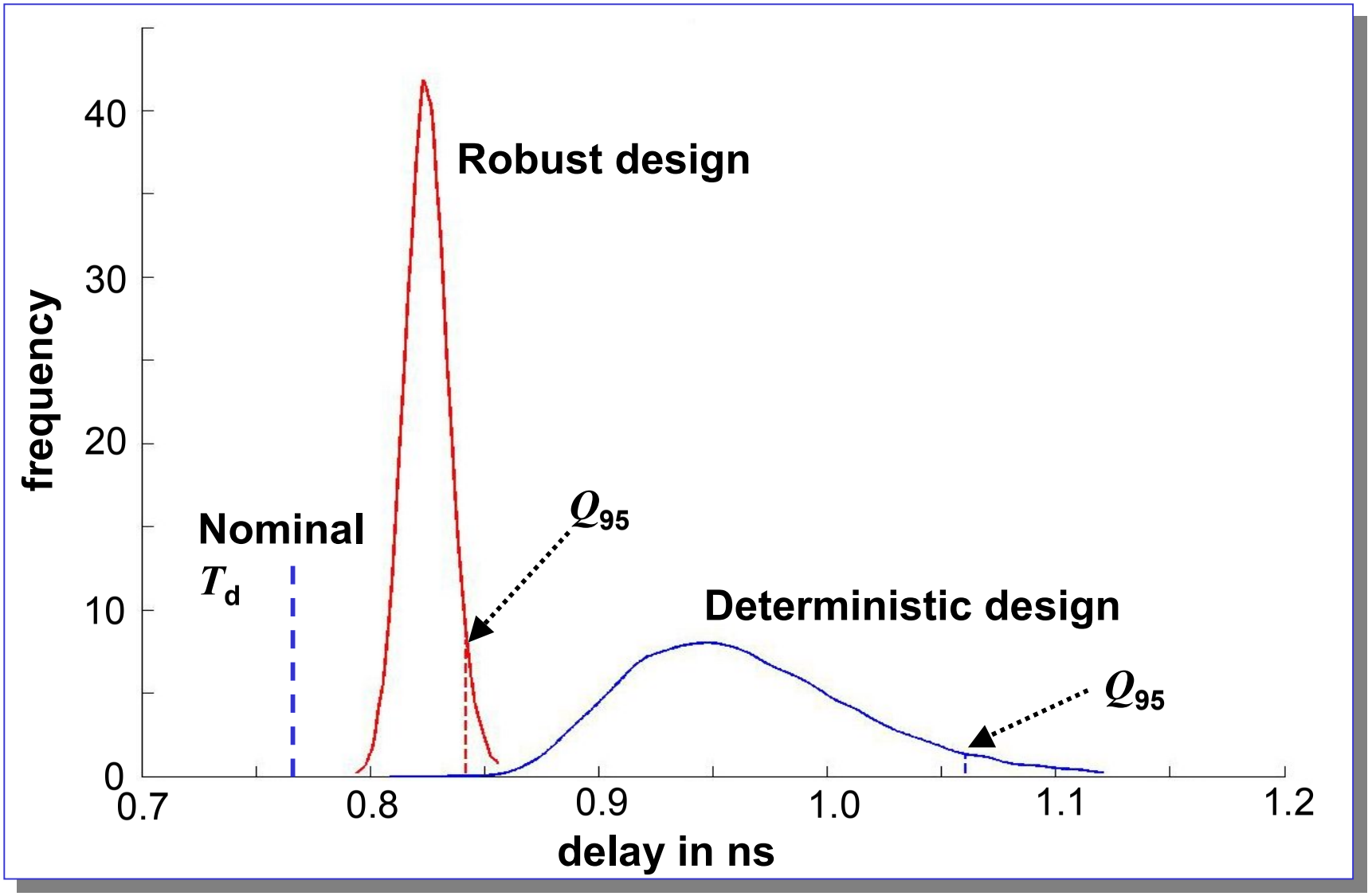


- **451 gates, 1714 devices. 0.18μm CMOS**
- **Same constraints for both methods**
- **Std. Dev. of 15% used for W = 1μ.**
- **Results in a highly sparse GP**
- **~45,000 variables, ~10,000 constraints**
- **Run time per optimization iteration:**

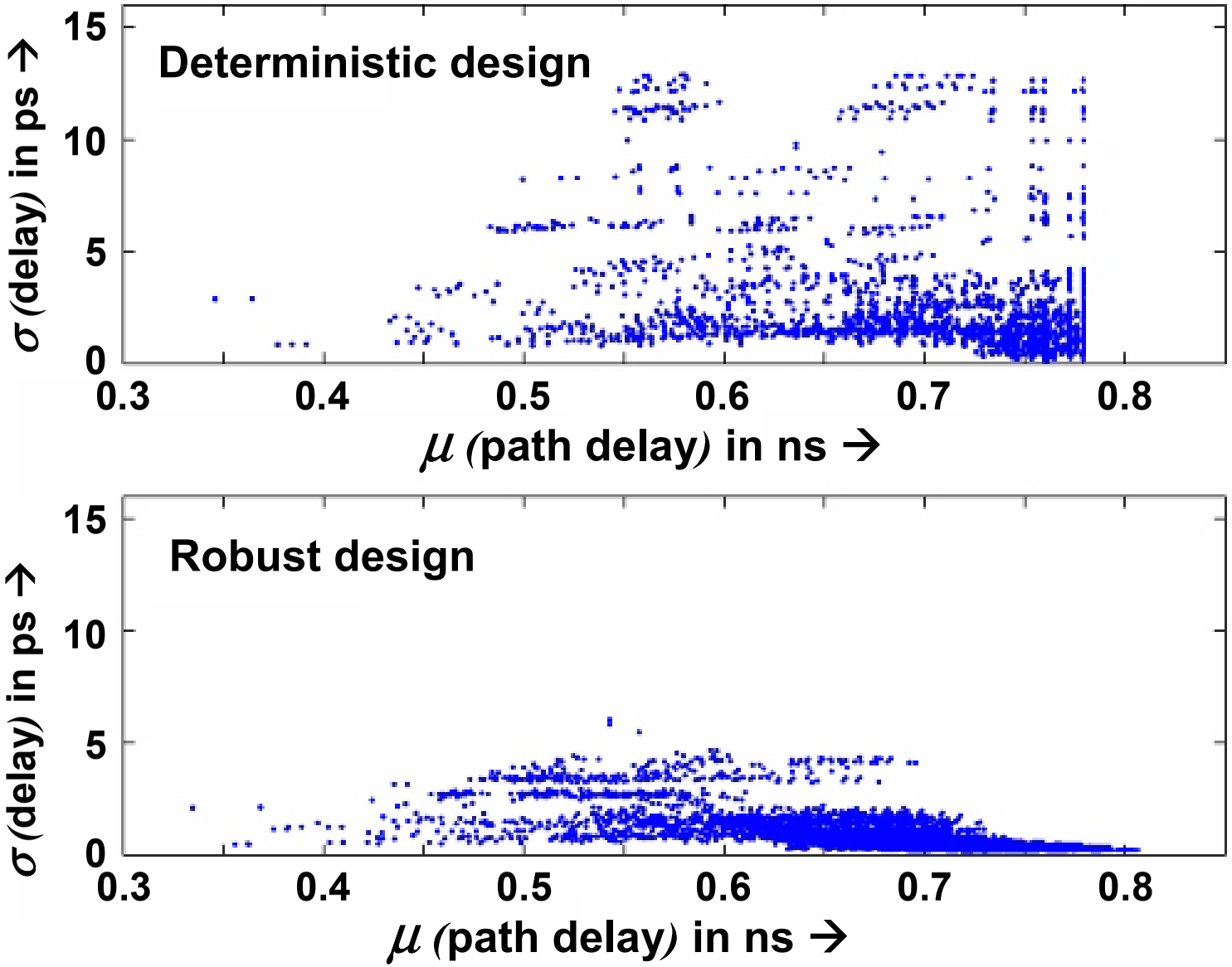
  5 mins (2 GHz Pentium IV™, 1GB RAM)
- **Semi-custom design**

(Knowles. S., Proc. 15th IEEE Symp. on Comp. Arithmetic, 2001)

Delay PDF for robust sizing



Comparison of μ – σ scatter plots of path delays



Conclusions

- **Without major change in the existing design methods, better, robust designs can be obtained**
- **Delay models and constraints can be GP compatible**
  - GPs are scalable and can be efficiently solved for a global optimum
- **Accurate propagation of PDFs might not be necessary**
  - Exploit the flat minima
  - Simple techniques yield poor predictions, but good designs!