Optimization of Phase-Locked Loop Circuits via Geometric Programming

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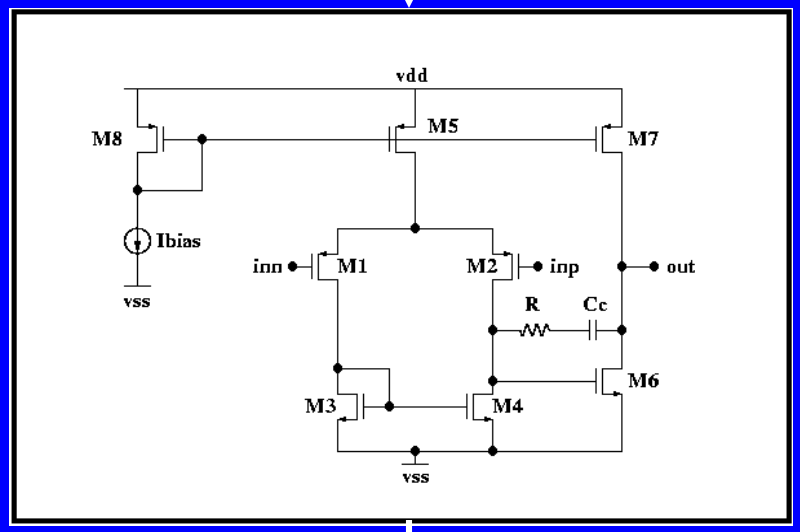
Outline

- Motivation
- Geometric programming (GP)
- GP compatible transistor models
- Clock generation PLL topology
- PLL design in GP form
- Silicon results

Simulation-based methods

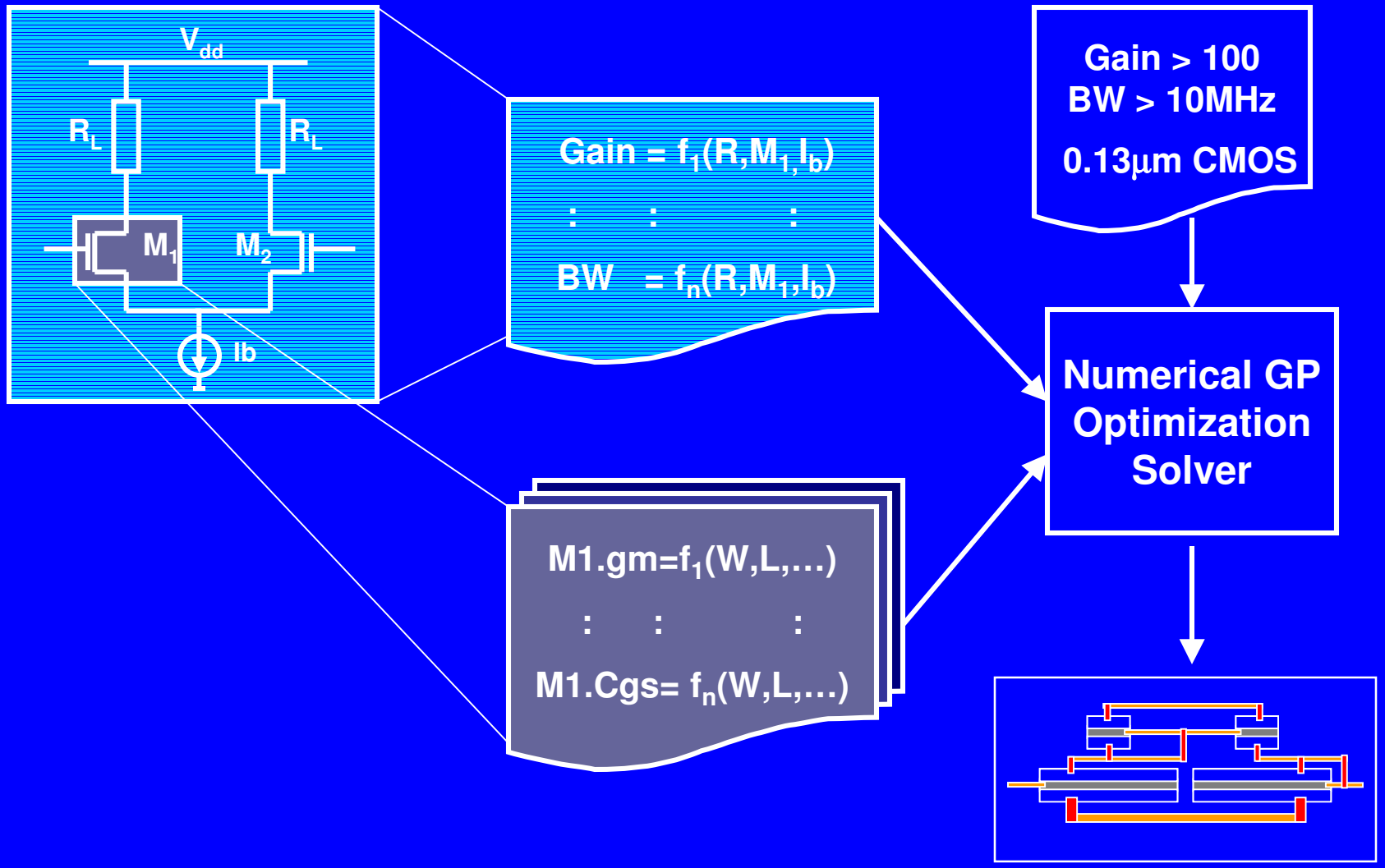
W1 = 1
W2 = 2
: :
L8 = 1



Power = 1
Gain = 500

- General purpose
- Long design cycles
- Needs circuit expert
- Needs optim. expert

Geometric programming-based method



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Geometric programming

- A *monomial* function *g(x)* has the form

$$g(x) = c x_1^{\alpha_1} x_2^{\alpha_2} \cdots x_n^{\alpha_n} \qquad (c > 0)$$

- A *posynomial* function *f(x)* is a sum of monomials

For example, $f(x) = 2 x_1 x_2^{-0.7} + .5 x_1^2 x_3^5$

- Geometric program (GP) is

$$\begin{aligned} \text{minimize} \quad & f_0(x) \\ \text{subject to} \quad & f_i(x) \le 1 \quad i = 1, \ldots, m \\ & g_i(x) = 1 \quad i = 1, \ldots, p \\ & x \ge 0 \end{aligned}$$

GPs can be easily transformed into convex problem

Solving GP's

New *interior point* methods for GP

- are extremely fast
- find globally optimal solution or provide proof of infeasibility
- are independent of starting point

For PLL synthesis: 40k optimization variables and 150k constraints takes ~90 minutes on 2GHz PC

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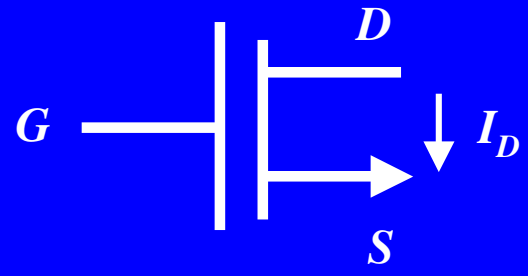
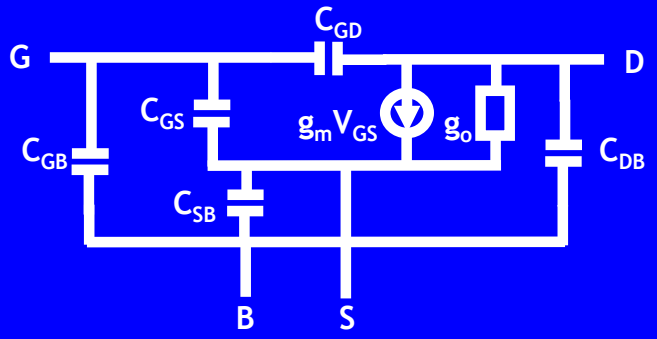
GP electrical models





$$I_{DS} = k\frac{W}{L}(V_{GS} - V_T)^2 \qquad g_m = 2k\frac{W}{L}(V_{GS} - V_T)$$

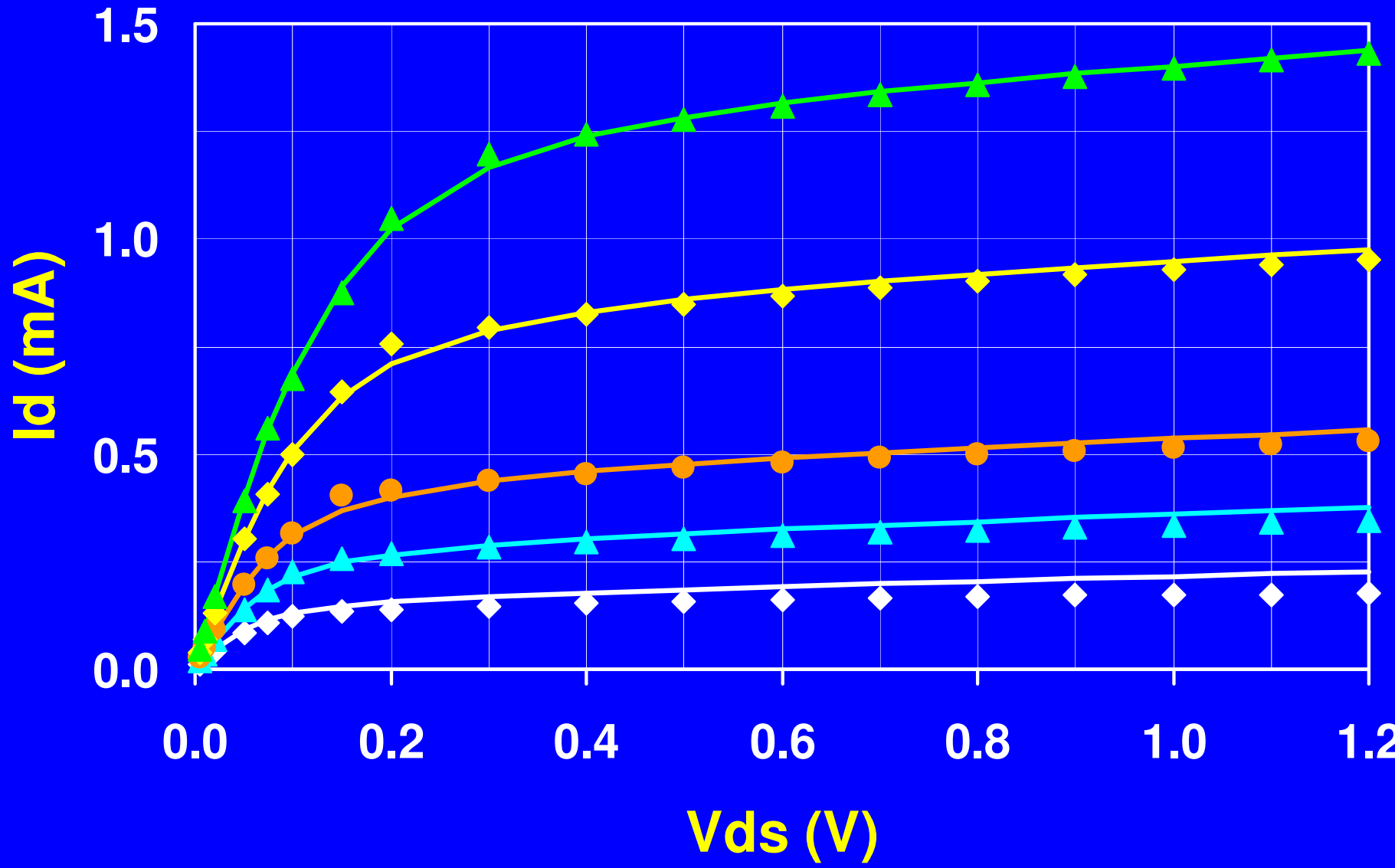
$$I_{DS} = kW^1L^{-1}V_{OV}^2 \qquad g_m = c_2W^1L^{-1}V_{OV}^1$$

$$V_{DS} \geq V_{GS} - V_T \qquad C_{gs} = \frac{2}{3}C_{OX}WL + C_{OX}WL_D$$

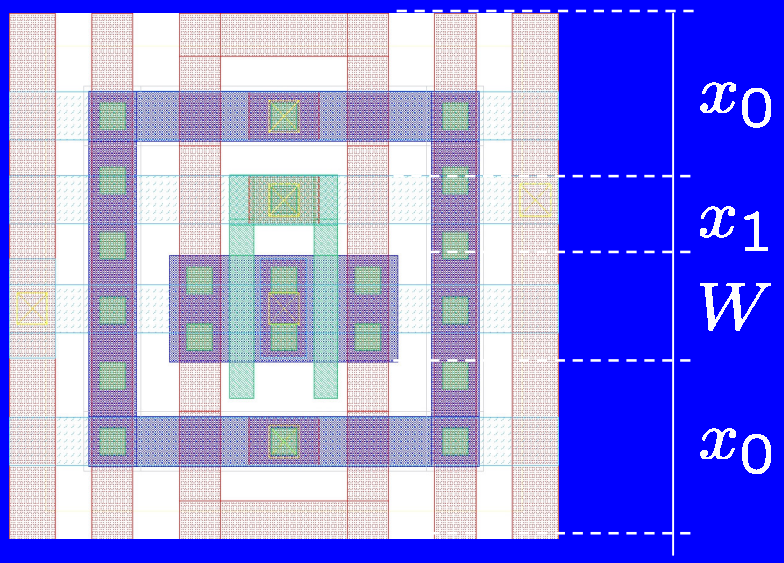
- **Complex GP models can be developed including short-channel effects, finite output impedance, etc…, e.g.,**

$$g_m = \sum c_i I_{DS}^{\alpha_{1,i}} L^{\alpha_{2,i}} W^{\alpha_{3,i}} V_{DS}^{\alpha_{4,i}} V_{SB}^{\alpha_{5,i}}$$

GP models – Id vs. Vds, 0.18μm



GP physical models



Posynomial expressions for

Width and height, e.g.,

$$Height = 2x_0 + x_1 + W$$

AD, AS, PD & PS, e.g.,

$$AD = N_f\,(W + 2W_D)\,(L_D + L_{DIF} + H_{DIF})$$

Placement and Routing

- Symmetry Constraints
- Mirroring Nets
- Net Matching
- Alignment
- Capacitance Constraints
- Shielding
- EM/IR drop considerations
- Dummy poly for matching and STI

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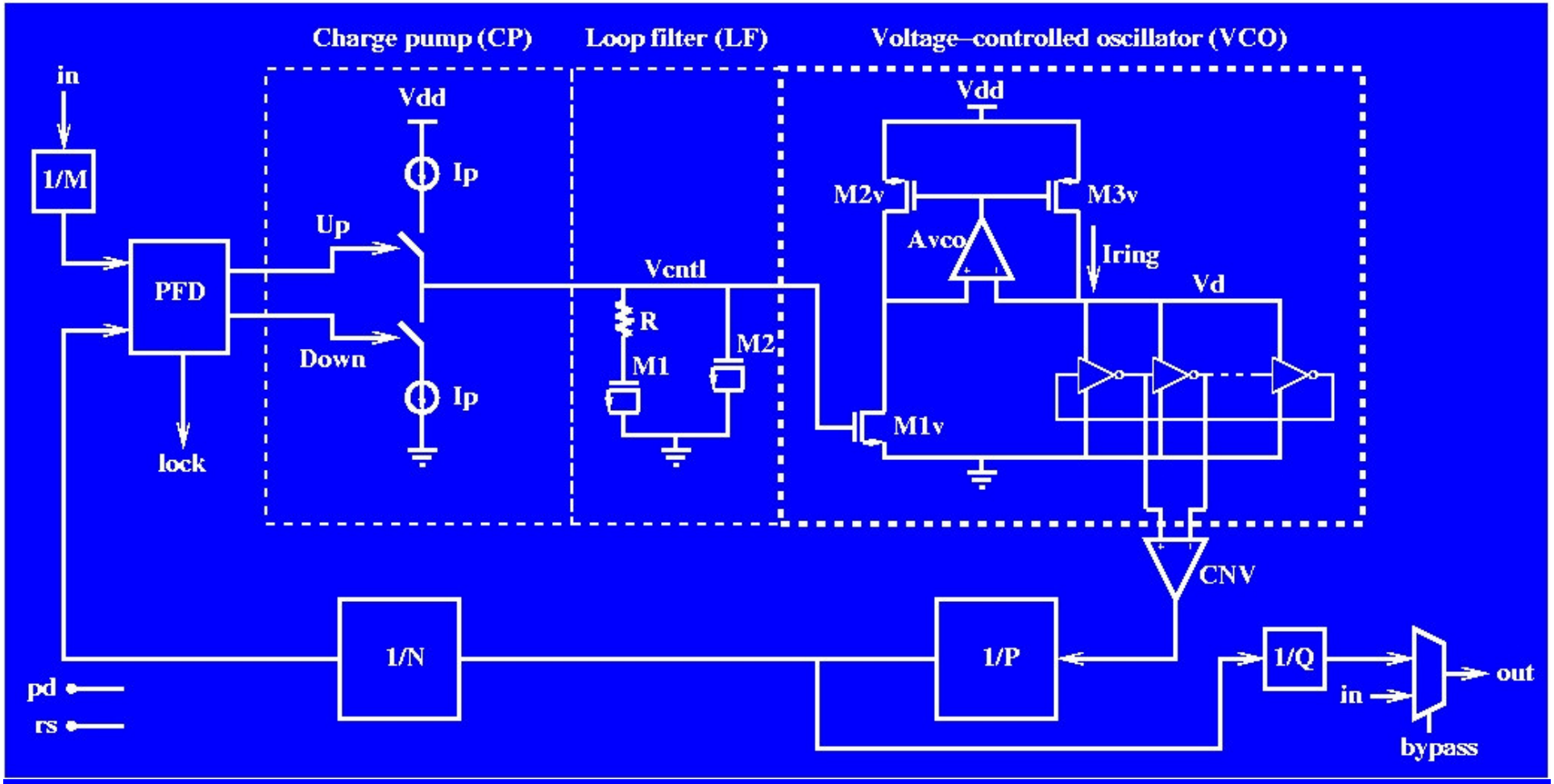
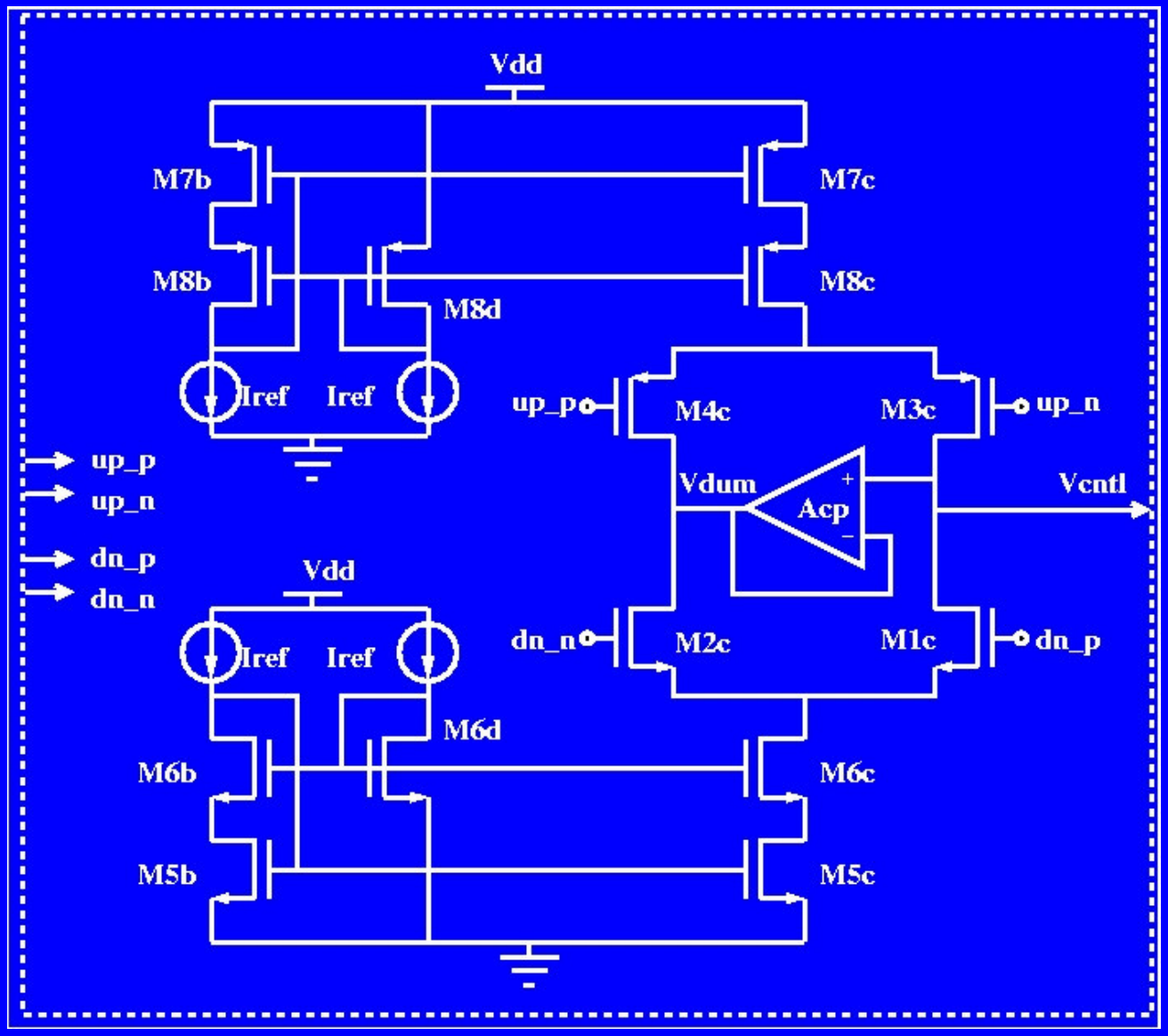
PLL topology



- Charge pump PLL with low–power programmable dividers (12 bit, >2GHz)
- Variables include device dimensions (W,L) and # of ring oscillator stages (S)

Charge pump topology

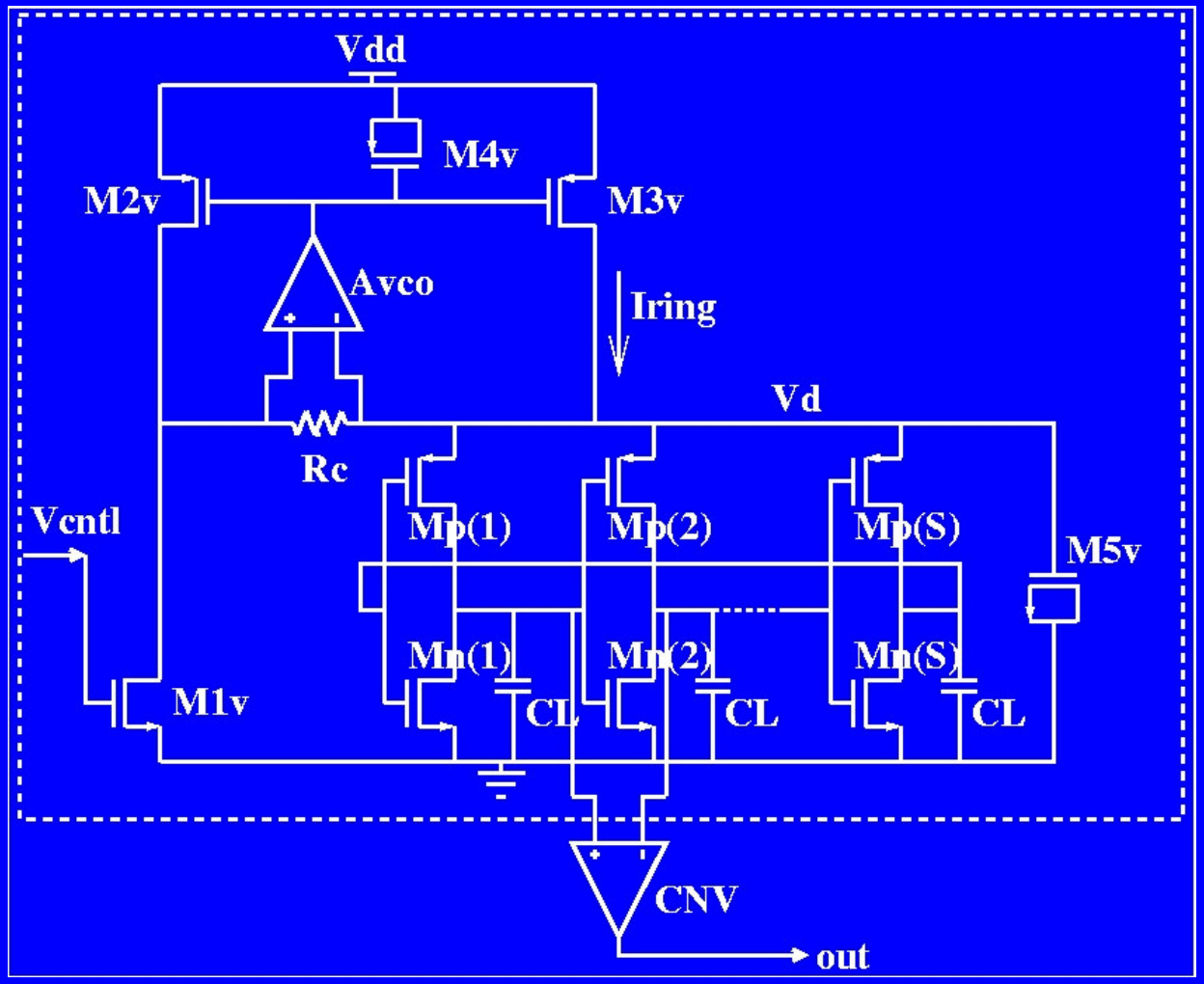


Example current mirror equalities (monomial):

$$L_{\mathrm{M5c}} = L_{\mathrm{M5b}}$$

$$V_{\mathrm{gov,M5c}} = V_{\mathrm{gov,M5b}}$$

VCO topology



Example saturation margin inequalities (posynomial):

$$V_{\mathrm{d}} \geq V_{\mathrm{gov,M1v}}$$

$$V_{\mathrm{d}} \leq V_{\mathrm{dd}} - V_{\mathrm{gov,M3v}}$$

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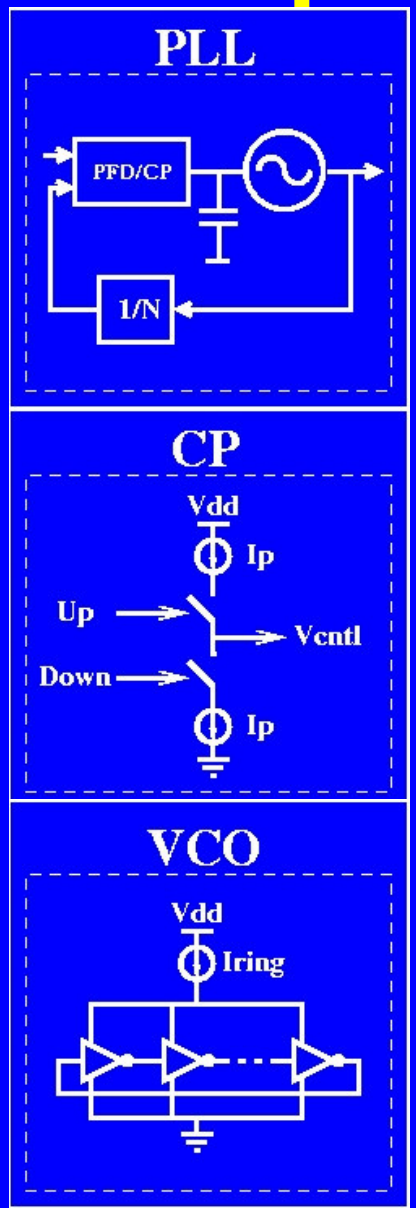
Second-order PLL system-level equations, in monomial form

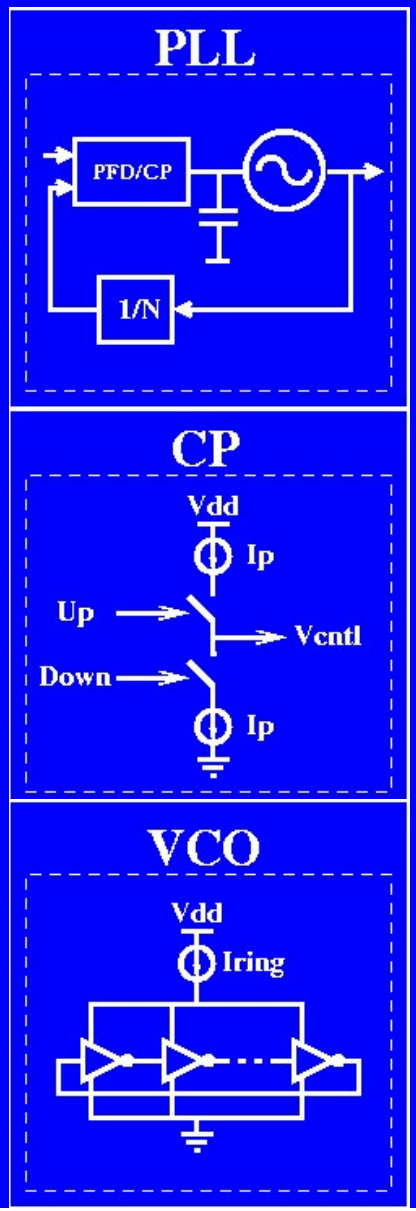


$$\omega_n = \sqrt{\frac{K_{cp} K_{vco}}{2\pi N P C_1}}, \zeta = \frac{\omega_n R C_1}{2}$$

$$K_{cp} = I_{ref} \left(\frac{W_{M5c} L_{M5b}}{W_{M5b} L_{M5c}} \right)$$

$$K_{vco} = g_{m,M1v} \left(\frac{W_{M3v}}{W_{M2v}} \right) \left(\frac{\partial \omega_{vco}}{\partial I_{ring}} \right)$$

Power consumption (posynomial)

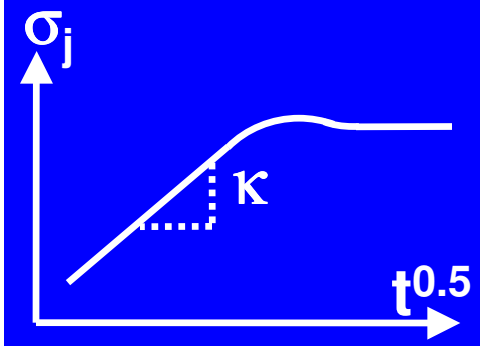


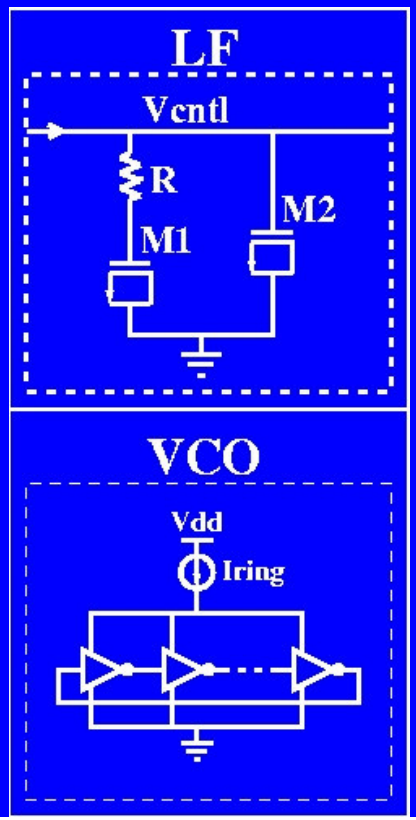
$$Power = Power_{CP} + Power_{VCO} + Power_{digital} < Power_{spec}$$

$$Power_{CP} = V_{dd}\left(4I_{ref} + I_p\right) + Power_{Acp}$$

$$Power_{VCO} = V_{dd}\left(I_{d,M2v} + I_{ring}\right) + Power_{Avco}$$

Accumulated jitter, T_{aj} (posynomial)





$$T_{aj}^2 = \sigma_{j,pk}^2 < \left(T_{aj,spec}\right)^2$$

$$\sigma_{j,pk}^2 = \left(\kappa_{LF}^2 + \kappa_{VCO}^2\right)\frac{1}{2\zeta\omega_n}$$

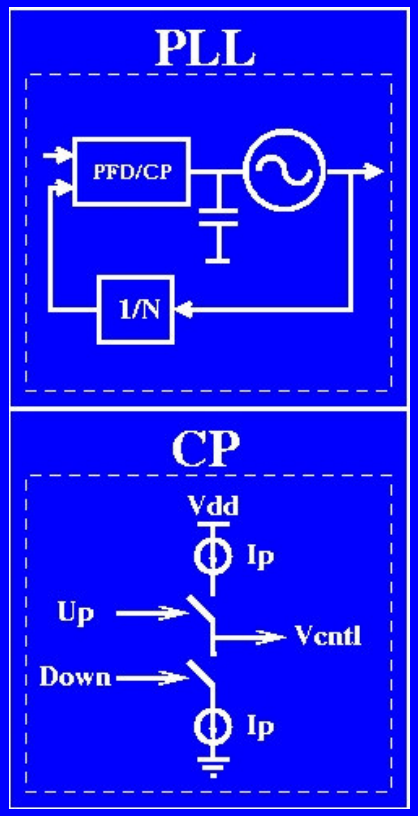
From McNeil (JSSC 1997):

$$\kappa_{LF}^2 = 4kTR\left(\frac{K_{vco}^2}{2\omega_{vco}^2}\right)$$

Using Hajimiri's phase noise model (JSSC 1998):

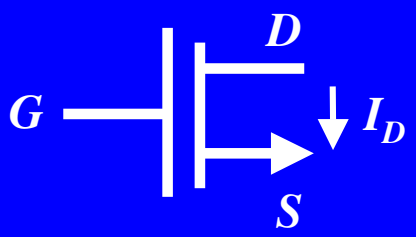
$$\kappa_{VCO}^2 = \left(\frac{\Gamma_{rms}}{C_L V_{d\omega vco}}\right)^2 \left(\frac{4kT\gamma}{2}\right)\left(g_{m,Mn} + g_{m,Mp}\right) S + \left(\frac{\partial\omega_{vco}}{\partial I_{ring}}\right)^2 \left(\frac{1}{2\omega_{vco}^2}\right) 4kT\gamma \left[g_{m,M3v} + \left(\frac{W_{M3v}}{W_{M2v}}\right)^2 \left(g_{m,M1v} + g_{m,M2v}\right)\right]$$

Static phase error, T_{err} (posynomial)



$$T_{\text{err}}^2 = \sigma_{\text{I}_\text{p}}^2 \frac{t_{\text{r,PFD}}^2}{I_\text{p}^2} < (T_{\text{err}})^2$$

$$\sigma_{\text{I}_\text{p}}^2 = \frac{I_\text{p}}{I_{\text{ref}}} \left(\sigma_{\text{I}_{\text{d,M5b}}}^2 + \sigma_{\text{I}_{\text{d,M7b}}}^2 \right)$$



Using Pelgrom's mismatch model (JSSC 1989):

$$\sigma_{\text{I}_{\text{d,M5b}}}^2 = \left(\frac{\sigma_\beta I_{\text{d,M5b}}}{\sqrt{W_{\text{M5b}} L_{\text{M5b}}}} \right)^2 + \left(\frac{\sigma_{\text{V}_\text{t}} g_{\text{m,M5b}}}{\sqrt{W_{\text{M5b}} L_{\text{M5b}}}} \right)^2$$

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GP vs. Silicon – 0.18um PLL arrays

#	Fref [MHz]	Fvco [MHz]	T_{pj} [ps]	Φ_e [ps]	Power [mW]		T_{aj} [ps]	
					GP	Meas	GP	Meas
1	50	1200-1900	2.2	93	11.0	10.8	5.7	6.2
2	33	600-1600	2.1	62	8.8	7.3	7.5	8.0
3	10	1500	4.2	54	7.9	6.0	15.3	14.4
4	20	400	2.7	28	3.2	2.8	14.3	12.0
5	25	250	3.1	16	3.0	3.0	9.7	9.6
6	3-6	81-135	5.9	48	2.7	2.5	27.9	24.2

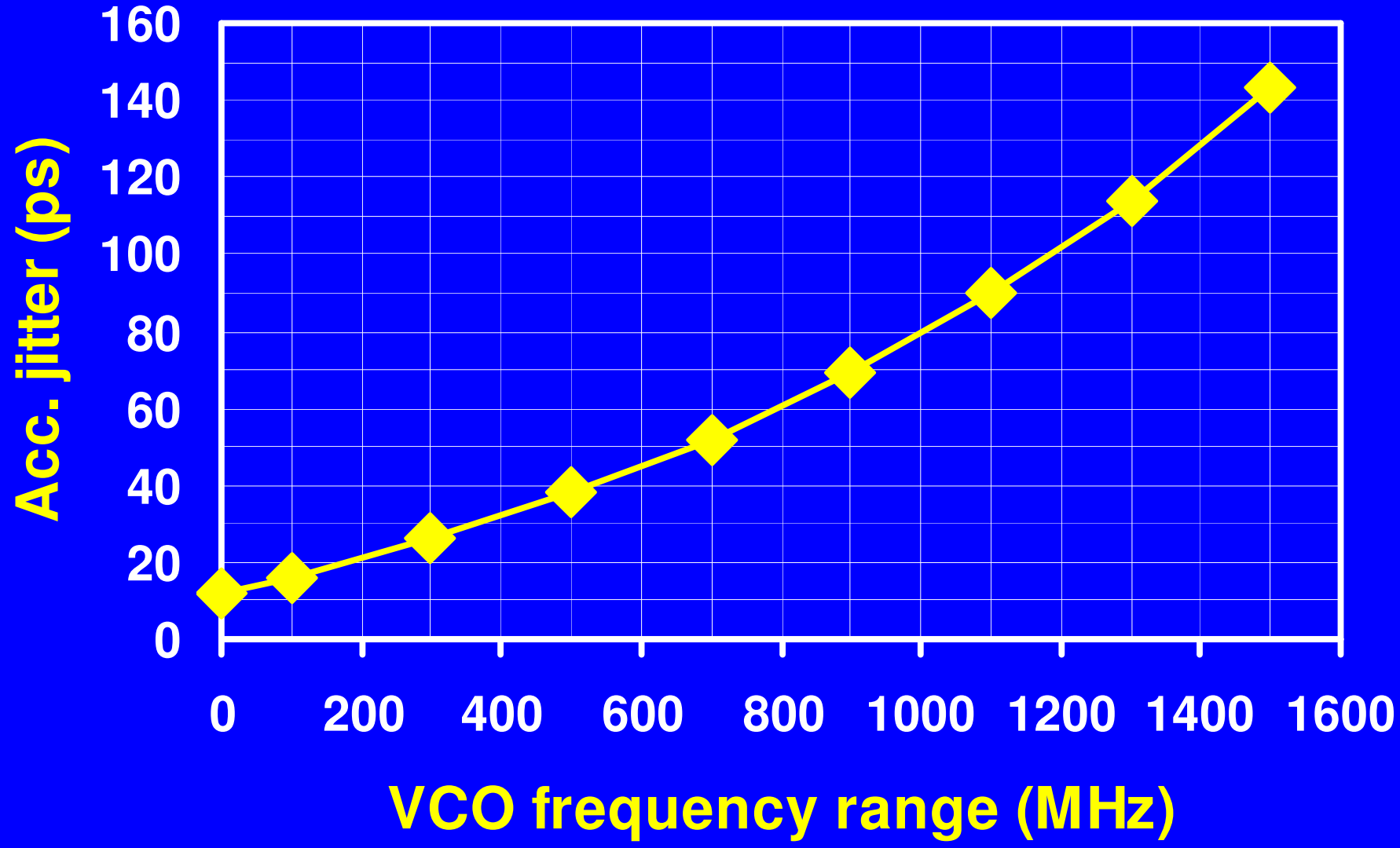
- **Good agreement between GP and silicon meas.**

GP vs. Silicon – 0.13um PLL arrays

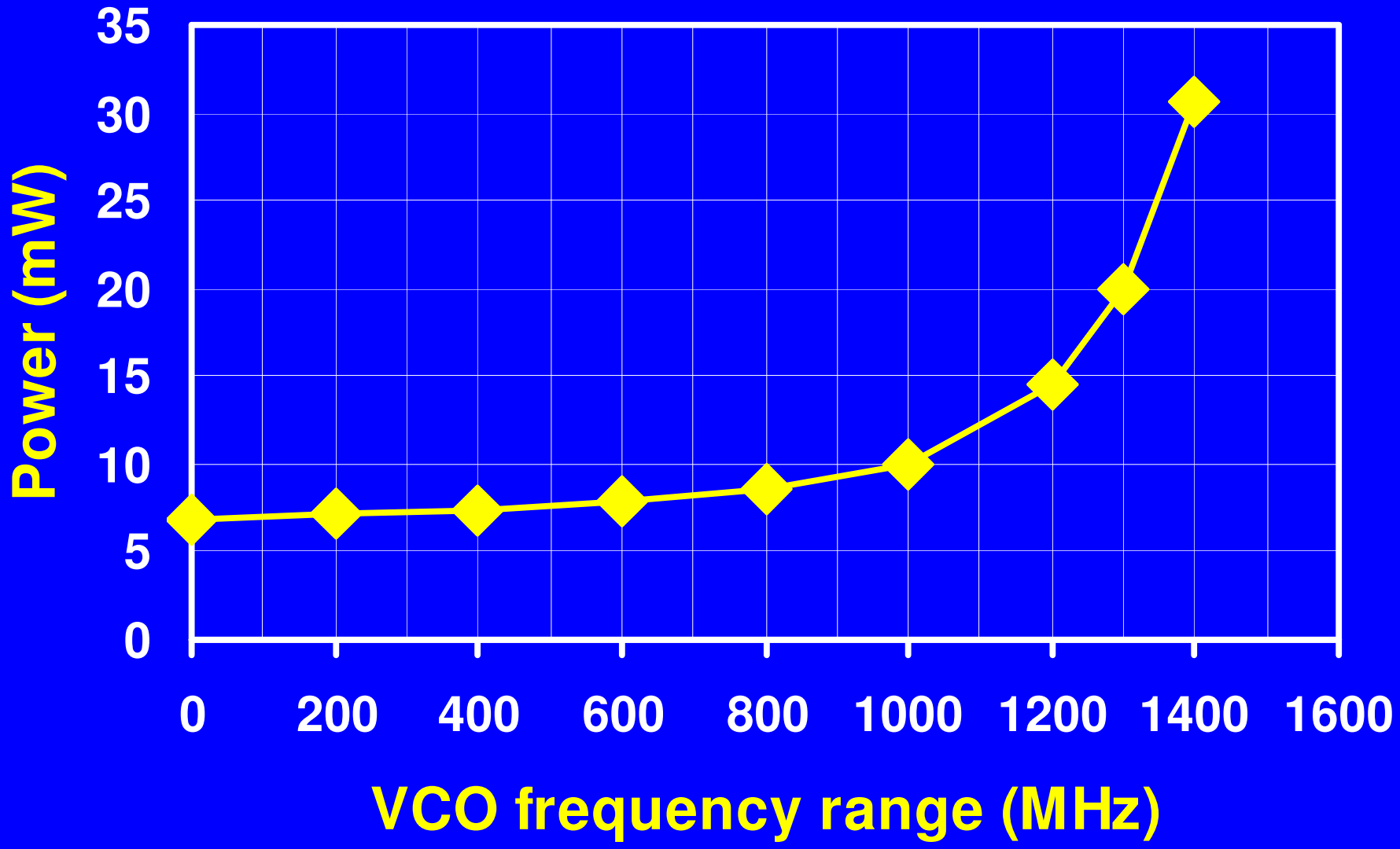
#	Fref [MHz]	Fvco [MHz]	T_{pj} [ps]	Φ_e [ps]	Power [mW]		T_{aj} [ps]	
					GP	Meas	GP	Meas
1	50-155	800-1600	5.4	40	18.3	--	8.9	7.7
2	25-50	500-1000	3.2	47	13.2	--	13.9	13.1
3	20	1000-1400	4.3	53	17.8	12.6	5.8	5.4
4	24	192-384	4.1	43	11.7	11.1	6.7	6.9
5	90-105	900-1050	4.6	30	10.1	6.1	4.7	6.7
6	0.5	512	12.7	22	13.3	8.53	44.9	43.5

- **Good agreement between GP and silicon meas.**

Acc. jitter vs. ΔF_{vco} trade-off analysis



Power vs. ΔF_{vco} trade-off analysis



Automated design does not translate into performance degradation

PLL #	Fref [MHz]	Fvco [MHz]	Taj,noise [ps]	Tpj,noise [ps]-[%Tvco/%Vdd]	
1	5	50	195	40.1	**0.020**
2	80	160	56.5	16.0	**0.026**
3	9.7	1244	65.5	3.8	**0.047**
4	20	1000-1400	125	7.9	**0.079**
5	20	1000-2000	147	8.1	**0.081**

Simulated 0.13µm, worst case PVT (FF, -40C or 125C) with 10% step on Vdd

Comparison to Literature

- **0.10 %Tvco/%Vdd** for 2.5V, 800-1400MHz PLL
  (M. Mansuri, ISSCC 2003)
- **0.08 %Tvco/%Vdd** for 2.0V, 800-1330MHz PLL with voltage regulator
  (V. Van Kaenel, JSSC 1998)

Room temperature with 10% step on Vdd

Conclusions

- First demonstration of fully-automated PLL design, from specification to GDSII
- PLL design problem cast in GP form reduces design time from weeks to hours
- Measured 0.18 μm and 0.13 μm CMOS PLL arrays agree with GP predictions (e.g. 1.9 GHz, 11 mW PLL with 5.8 ps long-term jitter)
- Robust, systematic, and efficient PLL design