## CS 107 Lecture 11: Assembly Part II Friday, February 11, 2022

Computer Systems Winter 2022 Stanford University Computer Science Department

Reading: Course Reader: x86-64 Assembly Language, Textbook: Chapter 3.1-3.4

Lecturer: Chris Gregg

```
// Type your code here, or load an example.
     void while_loop()
 2
 3
         int i=100;
 4
         int total;
 5
 6
         while (i >=0) {
             total += i;
 7
             i--;
 8
 9
10
```

1	1010	.LX0:	.text	//
1	while	e_loop	):	
2	mov	/ eax,	100	
3	jmp	<b>.</b> L2		
4	.L3:			
5	sub	o eax,	1	
6	.L2:			
7	tes	st eax	, eax	
8	jns	<b>.</b> L3		
9	rep	o ret		





- Reading: Course Reader: x86-64 Assembly Language, Textbook: Chapter 3.5-3.6
- Logistics •
  - Midterm Comments
- Programs from class: /afs/ir/class/cs107/samples/lect11 •
- More x86 Assembly Language •
  - Review of what we know so far
  - The lea instruction
  - pushing and popping from the stack
  - Unary operations, Binary operations, Shift operations ullet
  - Special multiplication and division
  - Control
    - Condition codes
    - **Conditional branches**

### Today's Topics



### What did we cover last Monday?

- Registers:
  - 16 regular integer registers, %rax, %rbx, ...
  - naming is historical, and a register has four nested parts: ullet



Operand forms: lots of ways we can refer to immediate values, register ulletvalues, or memory: Operan

Address	Value	Register	Value
0x100	0xFF	%rax	0x100
$0 \times 104$	0xAB	%rcx	0x1
0x108	0x13	%rdx	0x3
0x10C	0x11		

- %rax
- $0 \times 104$
- \$0x10
- (%rax
- 4(%ra
- 9(%ra
- 260 (%
- 0xFC(
- (%rax

%ax %al

return value

nd	Value	Comment
	0x100	Register
	0xAB	Absolute address
) 8	0x108	Immediate
<b>(</b> )	$0 \times FF$	Address 0x100
ax)	0xAB	Address 0x104
ax,%rdx)	0x11	Address 0x10C
srcx,%rdx)	0x13	Address 0x108
,%rcx,4)	$0 \times FF$	Address 0x100
x,%rdx,4)	0x11	Address 0x10C





## What did we cover last Monday? (continued)

• Data movement instructions:

	Instr	ruction		Effect
	MOV		S, D	$D \leftarrow S$
	m	ovb		
	m	OVW		
	m	ovl		
	m	ovq		
	mov	absq	<i>I</i> , <i>R</i>	$R \leftarrow I$
Examples:	1	movl	\$0x4050,%e	ax
	2	movw	%cx,%dx	
	3	movb	(%rdi,%rcx	:),%al
	4	movb	\$-17,(%rsp	)
	5	movq	%rax,-12(%	(rbp)

- Description
- Move
- Move byte
- Move word
- Move double word
- Move quad word
- Move absolute quad word
- Immediate-Register, 4 bytes
- Register-Register, 2 bytes
- Memory-Register, 1 byte
- Immediate-Memory, 1 byte
- Register-Memory, 8 bytes



### What did we cover last Monday? (continued)

movl	\$0x4050, %eax
movq	%rsp, %rax
movw	%ax, %dx
movl	\$1,%ecx
movb	(%rdi, %rcx), %al
movb	\$0x61, (%rsp)
movb	\$0x61,(%rdi, %rcx)
movq	%rax, 12(%rsp)



# ./mov\_examples\_main Before function call: hello After function call: hallo



### The lea instruction

- that reads from memory to a register, but it does not reference memory at all.
- location:

Instru	ction	Effect		
leaq	S,D	D ← &	S	
Exam	nples: if %rax holds	value	) )	< and
leaq	6(%rax), %rdx		:	%rdx
leaq	(%rax,%rcx), %rdx	• •	:	%rdx
leaq	(%rax,%rcx,4), %r	dx	:	%rdx
leaq	7(%rax,%rax,8), %	rdx	:	%rdx
leaq	0xA(,%rcx,4), %rd	X	:	%rdx
leaq	9(%rax,%rcx,2), %	rdx	:	%rdx

 The lea instruction is related to the mov instruction. It has the form of an instruction It's first operand appears to be a memory reference, but instead of reading from the designated location, the instruction copies the effective address to the destination. • You can think of it as the "&" operator in C — it retrieves the address of a memory

Description

Load effective address

```
%rcx holds value y:
```

```
now holds x + 6
now holds x + y
now holds x + 4^*y
now holds 7 + 9x
now holds 10 + 4y
now holds 9 + x + 2y
```



### The lea instruction

```
#include<stdlib.h>
#include<stdio.h>
int main() {
    int a = 42;
    int *aptr = &a;
    printf("a: %d, aptr: %p", a, aptr);
```

Notice that the value 42 is moved into memory via a mov instruction, while the address of that value is moved into %rdx using the lea instruction. In both cases, 12(%rsp) is the location in memory that is referred to, but mov moves data to that address, and lea moves the address into the register.

### Take a look at the following C code (left) and assembly generated by gcc (right):

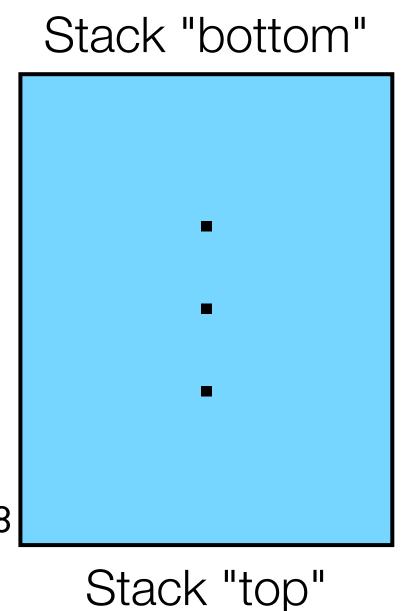
.LC0:		
	.string	"a: %d, aptr: %
main:		
	subq	\$24, %rsp
	movl	\$42, 12(%rsp)
	leaq	12(%rsp), %rdx
	movl	\$42, %esi
	movl	\$.LCO, %edi
	movl	\$0, %eax
	call	printf
	movl	\$0, %eax
	addq	\$24, %rsp
	ret	

Note: we often use the lea instruction for calculations that aren't memory addresses! This is because we get a nifty linear equation from lea, and it really doesn't matter if it isn't an address.



- As we have seen from stack-based memory allocation in C, the stack is an important part of our program, and assembly language has two built-in operations to use the stack.
- Just like the stack ADT, they have a first-in, first-out discipline. • By convention, we draw stacks upside down, and the stack "grows" downward. ullet







 The push and pop operations write a modify the stack pointer, %rsp:

Instruc	t	Effect
pushq	S	$R[\$rsp] \leftarrow R[\$rsp]-8;$
		$M[R[\%rsp]] \leftarrow S$
popq	D	D ← M[R[%rsp]];
		R[%rsp] → [%rsp]+8



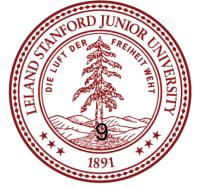
### The push and pop operations write and read from the stack, and they also

Description

Push quad word

Push quad word

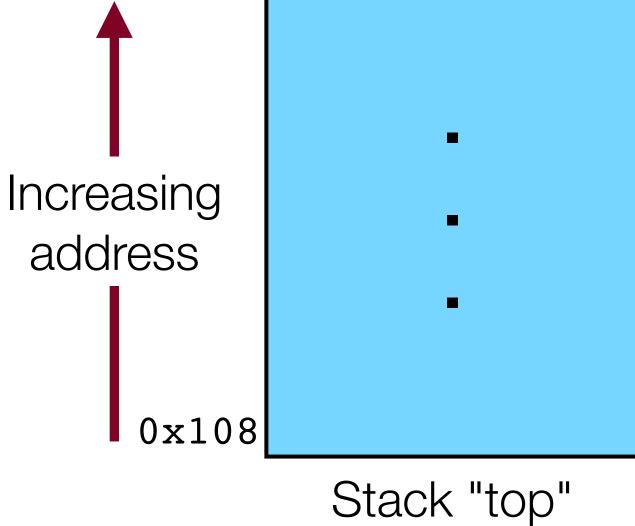
Stack "bottom" • • Stack "top"



• Example:

Initially		
%rax	0x123	
%rdx	0	
%rsp	0x108	

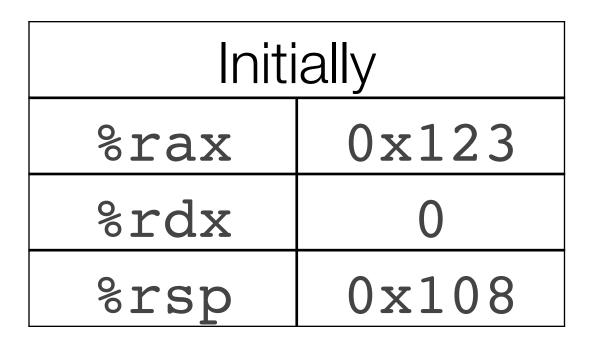


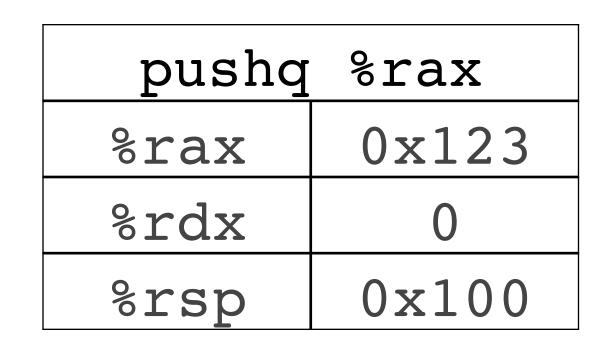


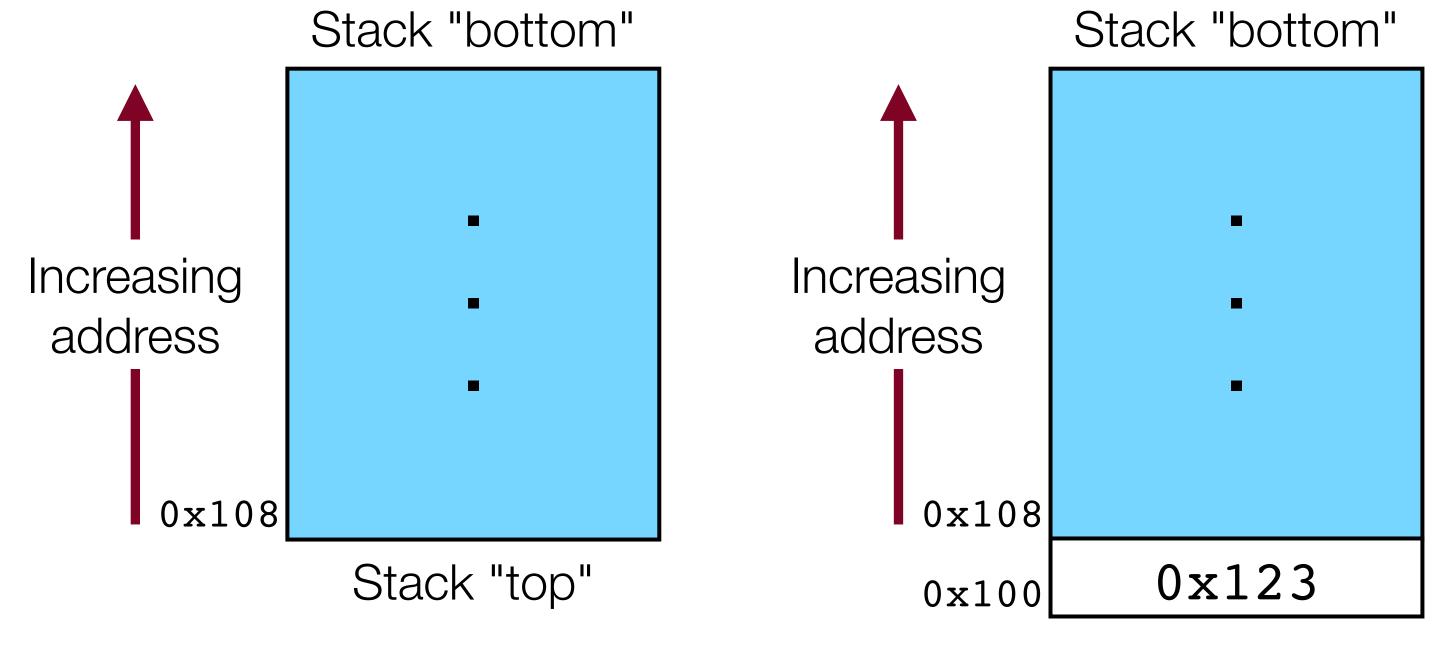
LELAND



• Example:



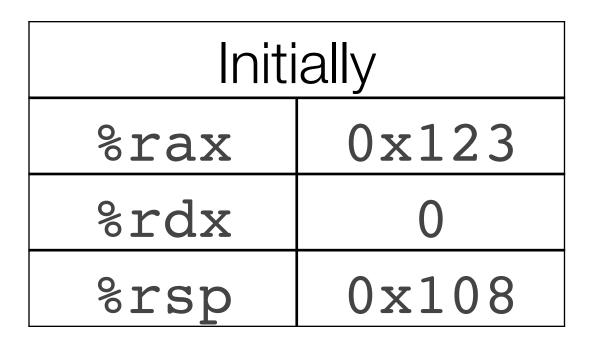


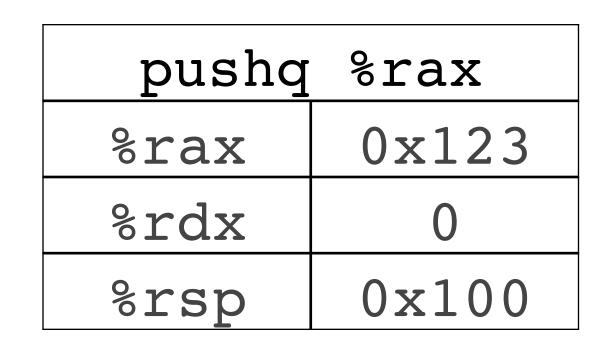


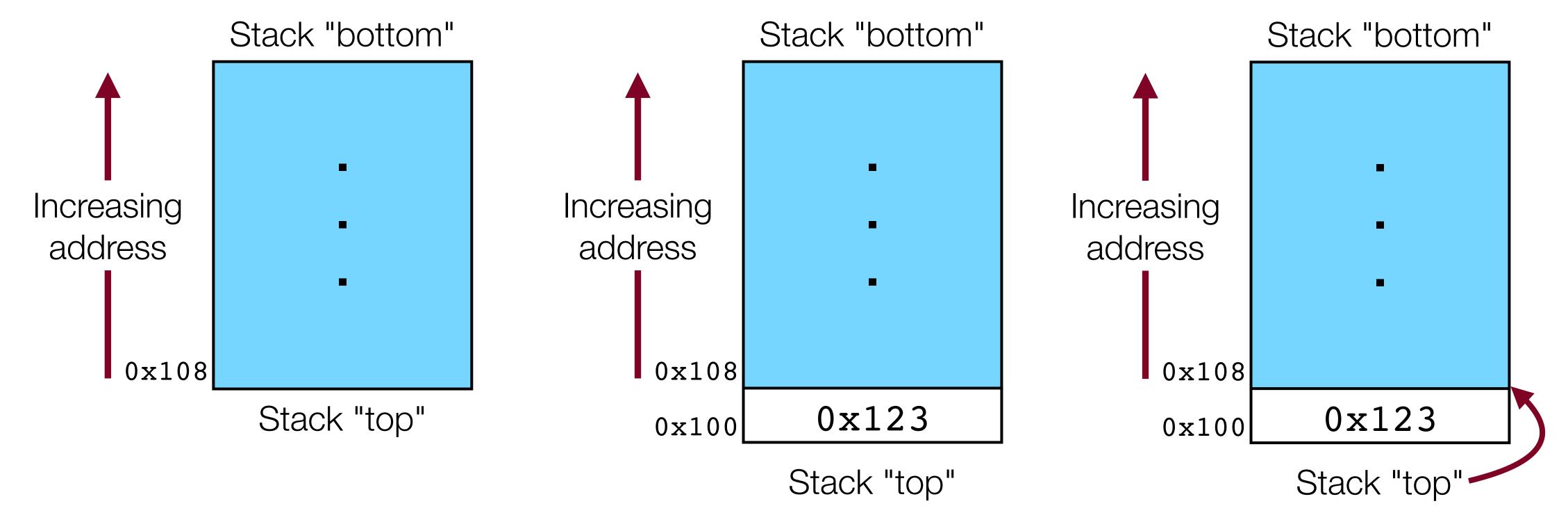
Stack "top"



• Example:







popq	%rdx
%rax	0x123
%rdx	0x123
%rsp	0x108



- As you can tell, pushing a quad word onto the stack involves first decrementing the stack pointer by 8, and then writing the value at the new top-of-stack address.
- Therefore, the behavior of the instruction pushq %rbp is equivalent to the pair of instructions:

subq \$8, %rsp movq \$rbp,(%rsp) (Store %rbp on the stack)

• The behavior of the instruction popg %rax is equivalent to the pair of instructions:

movq (%rsp), %rax addq \$8,%rsp

(subg is a subtraction, and this decrements the stack pointer)

(Read %rax from the stack) (Increment the stack pointer)









### The following instructions act on a single operand (register or memory):

Instruction	Effect
inc D	$D \leftarrow D + 1$
dec D	<i>D</i> ← D − 1
neg D	$D \leftarrow -D$
not D	$D \leftarrow \neg D$

inc D is reminiscent of C's ++ operator, and neg D is reminiscent of C's -- operator.

Examples: incq 16(%rax) decq %rdx not %rcx

### Unary Instructions

Description Increment Decrement Negate Complement





## Binary Instructions

Instruction	Effect	Description
add S, D	$D \leftarrow D + S$	Add
sub S, D	$D \leftarrow D - S$	Subtract
imul S, D	$D \leftarrow D * S$	Multiply
xor S, D	$D \leftarrow D \wedge S$	Exclusive-or
or S, D	$D \leftarrow D \mid S$	Or
and S, D	$D \leftarrow D \& S$	And

Reading the syntax is a bit tricky — e.g., subq %rax, %rdx decrements %rdx by %rax, and can be read as "Subtract %rax from %rdx"

Examples: addg %rcx,(%rax) xorq \$16,(%rax,%rdx,8) subq %rdx,8(%rax)

The following instructions act on two operands (register or memory, but not both):



### Shift Instructions

## immediate value or the byte %cl (and only that register!)

Instruction	Effect	Description
sal k, D	$D \leftarrow D << k$	Left shift
shl k, D	$D \leftarrow D << k$	Left shift (same as sal)
sar k, D	$D \leftarrow D >>_A k$	Arithmetic right shift
shr k, D	$D \leftarrow D >>_L k$	Logical right shift

Technically, you could shift up to 255 with *%c1*, but the data width operation determines how many bits are shifted, and the high order bits are ignored. For example, if %cl has a value of 0xFF, then shlb shifts by 7 (ignoring the upper bits), shlw shifts by 15, shll would shift by 31, and shlq would shift by 63.

Examples: shll \$3,(%rax) shr %cl,(%rax,%rdx,8) sar \$4,8(%rax)

The following instructions perform shifts. The first operand can be either an



### Special Multiplication Instructions

Recall that multiplying two 64-bit numbers can produce a 128-bit result. The x86-64 instruction set supports 128-bit numbers with the "oct" (16-byte) size.

Instruction	Effect	Description
imulq S	$R[\$rdx]:R[\$rax] \leftarrow S \times R[\$rax]$	Signed full multiply
mulq S	$R[\$rdx]{:}R[\$rax] \leftarrow S \times R[\$rax]$	Unsigned full multiply

The imulg instruction has two forms. One, shown on slide 15, takes two operands and leaves the result in a single 64-bit register, truncating if necessary (and acts the same on signed and unsigned numbers). Example: imulg %rbx, %rcx

The second form (shown above) multiplies the source by rax, and puts the product into the 128-bit %rdx (upper 64 bits) and %rax (lower 64 bits).

Example: mul %rdx This multiples %rdx by %rax and puts the result into the combined %rdx:%rax registers.





### Multiplication Example

```
#include <stdio.h>
#include <stdlib.h>
#include <inttypes.h>
typedef unsigned ___int128 uint128_t;
void store uprod(uint128 t *dest,
                 uint64 t x, uint64 t y)
    *dest = x * (uint128 t) y;
int main()
    uint64 t x = 200000000000; // 2 trillion
    uint64_t y = 300000000000; // 3 trillion
    uint128 t z;
    store_uprod(&z,x,y);
    print uint128(z); // see lect12 code
                // for function definition
    return 0;
```

mov	%rsi,%rax
mul	%rdx
mov	%rax,(%rdi)
mov	%rdx,0x8(%rdi)
retq	

Note: %rdi is 1st argument %rsi is 2nd argument %rdx is 3rd argument





## Special Division Operations

Slide 11 did not list a division instruction or modulus instruction. There are single-operand divide instructions (shown below):

Instruction	Effect	Description
cqto	R[%rdx]:R[%rax] — SignExtend(R[%rax])	Convert to oct word
idivq S	$R[\rdx] \leftarrow R[\rdx]:R[\rax] \mod S;$	Signed divide
	R[%rax] — R[%rdx]:R[%rax] ÷ S	
divq S	$R[$ rdx] $\leftarrow R[$ rdx]: $R[$ rax] mod S;	Unsigned divide
	$R[\$rax] \leftarrow R[\$rdx]:R[\$rax] \div S$	

The dividend for the idivg and divg instructions is the 128-bit quantity in registers %rdx (high-order 64-bits) and %rax (low-order 64-bits). The divisor is the operand source. The quotient from the division is stored in %rax, and the remainder is stored in %rdx.

For most division, the dividend is just in %rax, and %rdx is either all zeros (for unsigned, or the sign bit of %rax (for signed arithmetic). The ctgo instruction can be used to accomplish this.





### Division Example

mov
mov
cqto
idiv
mov
mov
retq



### gcc is clever enough to see that only one division is needed!

%rdx,%r8 %rdi,%rax	<pre># copy qp # Move x to lower 8 bytes of dividend</pre>
	# Sign-extend to upper 8 bytes of divid
%rsi	# Divide by y
%rax,(%r8)	# Store quotient at qp
%rdx,(%rcx)	# Store remainder at rp

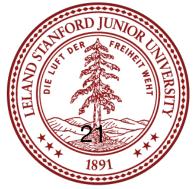
Note: %rdi is 1st argument %rsi is 2nd argument %rdx is 3rd argument %rcx is 4th argument





### 3 minute break





- So far, we have only been discussing "straight-line" code, where one instruction happens directly after the previous instruction.
- However, it is often necessary to perform one instruction or another tools to do this.
- branch)
- We will start by discussing "condition codes" that are set when we do arithmetic (and other operations), and then we will talk about jump instructions to change control flow.

### Control

instruction based on the logic in our programs, and assembly code gives us

• We can alter the flow of code using a "jump" instruction, which indicates that the next instruction will be somewhere else in the program (this is called a



### Condition Codes

- Besides the registers we have already discussed, the CPU has a separate set of single-bit *condition code* registers describing attributes of recent operations.
- We can use these registers (by testing them) to perform branches in the code.
- These are the most useful condition code registers:
  - **CF**: Carry flag. The most recent operation generated a carry out of the most significant bit. Used to detect overflow for unsigned operations.
  - **ZF**: Zero flag. The most recent operation yielded zero.
  - SF: Sign flag. The most operation yielded a negative value.
  - OF: Overflow flag. The most recent operation caused a two's-complement overflow either negative or positive.



### Condition Codes: Examples

- **CF**: Carry flag. The most recent operation generated a carry out of the most significant b/t. Used to detect overflow for unsigned operations.
- **ZF**: Zero flag. The most recent operation yielded zero.
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### The **ZF** flag.

### Which flag above would be set?



## Condition Codes: Examples

- **CF**: Carry flag. The most recent operation generated a carry out of the most significant b/t. Used to detect overflow for unsigned operations.
- **ZF**: Zero flag. The most recent operation yielded zero.
- **SF**: Sign flag. The most operation yielded a negative value.
- **OF**: Overflow flag. The most recent operation caused a two's-complement overflow either negative or positive.

int 
$$a = 5;$$
  
int  $b = -5;$   
int  $t = a + b;$ 

int t = a + b;

int a

The **ZF** flag.

The SF flag.

- Which flag above would be set?
- Which flag above would be set?



### Condition Codes

- shr, etc.)
- For logical operations (e.g., xor), the carry and overflow flags are set to 0.
- For shift operations, the carry flag is set to the last bit shifted out, while the overflow flag is set to zero.
- (see <u>here</u> about a potential reason why).

 The leag instruction does not set any condition codes (because it is intended) for address computations), but the other arithmetic instructions we talked about do set them (inc, dec, neg, not, add, sub, imul, xor, or, and, shl, sar,

• inc and dec set the overflow and zero flags, but leave the carry flag unchanged







## without altering any other registers, the cmp and test instructions:

Instruction		Based on	Descriptior
CMP	S <sub>1</sub> , S <sub>2</sub>	S <sub>2</sub> - S <sub>1</sub>	Compare
cmpb			Compare b
cmpw			Compare v
cmpl			Compare o
cmpq			Compare o
TEST	S <sub>1</sub> , S <sub>2</sub>	S <sub>2</sub> & S <sub>1</sub>	Test
testb			Test byte
testw			Test word
testl			Test double
testq			Test quad v

### cmp and test

There are two types of instructions we can use that set the condition codes

•

- byte
- word
- double word
- quad word

e word word

- By setting the condition codes, we can set up for a jump or other logic, based on some condition (e.g., whether a register has reached a certain value.
- Be careful! The operands for • **cmp** are listed in reverse order! (cmp is based on the sub instruction)
  - Often, we use testq %rax, %rax to see whether %rax is negative, zerg or positive.



## Accessing the Condition Codes

- There are three common ways to use the condition codes:
  1. We can set a single byte to 0 or 1 depending on some combination of the condition codes.
  - 2. We can conditionally jump to some other part of the program.
  - 3. We can conditionally transfer data.



## Accessing the Condition Codes

• There are three common ways to use the condition codes: condition codes.

2. We can conditionally jump to some other part of the program. **3.** We can conditionally transfer data.

Instruction	Synonym	Set Condition
sete D	setz	Equal / zero
setne D	setnz	Not equal / not zero
sets D		Negative
setns D		Nonnegative
setg D	setnle	Greater (signed >)
setge D	setnl	Greater or equal (sig
setl D	setnge	Less (signed <)
setle D	setng	Less or equal (signed
seta D	setnbe	Above (unsigned >)
setae D	setnb	Above or equal (unsi
setb D	setnae	Below (unsigned <)
setbe D	setna	Below or equal (unsig

1. We can set a single byte to 0 or 1 depending on some combination of the

Example: a < b

```
int comp(data t a, data t b)
               ain%rdi, bin %rsi
               comp:
               cmpq %rsi, %rdi # Compare a:b
signed >=)
               setl %al
                              # Set low-order byte of
                                # %eax to 0 or 1
ied <=)
               movzbl %al, %eax # Clear rest of %eax
signed >=)
                                # (and rest of %rax)
               ret
signed <=)
```



## Accessing the Condition Codes

- There are three common ways to use the condition codes: condition codes.
- 2. We can conditionally jump to some other part of the program. 3. We can conditionally transfer data.

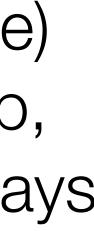
l	Instruction	Synonym	Set Condition
	jmp Label		Direct jump
	jmp *Operand		Indirect jump
	je <i>Label</i>	jz	Equal / zero (ZF=1)
	jne <i>Label</i>	jnz	Not equal / not zero (ZF=0)
	js <i>Label</i>		Negative (SF=1)
	jns <i>Label</i>		Nonnegative (SF=0)
	jg Label	jnle	Greater (signed >) (SF=0 and S
	jge <i>Label</i>	jnl	Greater or equal (signed >=) (S
	jl <i>Label</i>	jnge	Less (signed <) (SF != OF)
	jle <i>Label</i>	jng	Less or equal (signed <=) (ZF= <sup>-</sup>
	ja <i>Label</i>	jnbe	Above (unsigned >) (CF = 0 and
	jae <i>Label</i>	jnb	Above or equal (unsigned >=) (
	jb Label	jnae	Below (unsigned <) (CF = 1)
	jbe Label	jna	Below or equal (unsigned <=) (0

1. We can set a single byte to 0 or 1 depending on some combination of the

- SF=OF) SF=OF)
- 1 or SF!=OF)
- d ZF = 0
- (CF = 0)
- (CF = 1 or ZF = 1)

- Jump instructions jump to labels in assembly code, and those labels are changed to addresses (most often relative)
- jmp is an *unconditional* jump, meaning that the jump is always taken.
- Unconditional jumps can be direct or indirect
- Conditional jumps must be • direct.





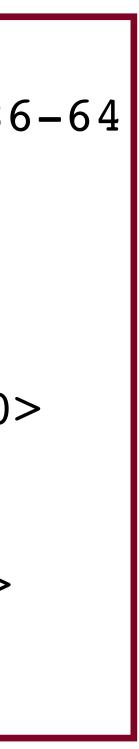


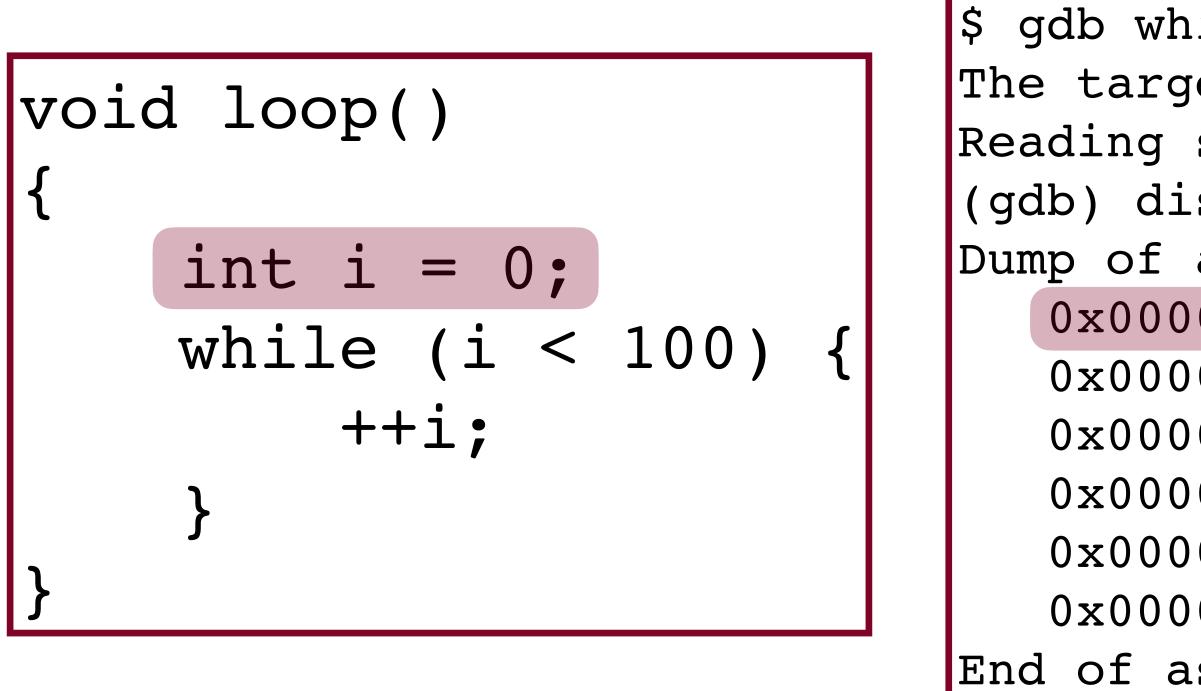
	<pre>\$ gdb while_loop.o</pre>
void loop() {	The target architecture is assumed to be i386:x86 Reading symbols from while_loop.odone. (gdb) disas loop
<pre>int i = 0; while (i &lt; 100) { ++i; } }</pre>	<pre>Dump of assembler code for function loop:</pre>
	End of assembler dump.

Compile to an object file:

gcc -c -Og while loop.c







Compile to an object file:

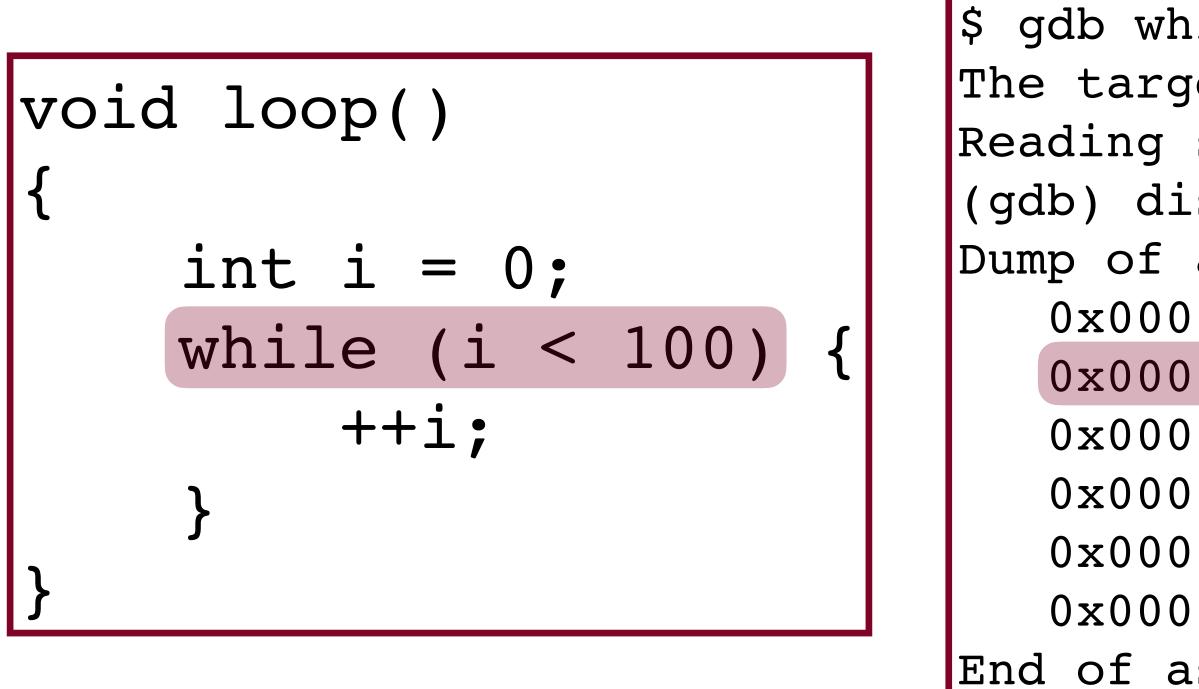
gcc -c -Og while loop.c

nile_loop.o get architectur	ro ic ac	sumod +	$a$ $ba$ $i386 \cdot v86$
symbols from w	vuite_to	op.o	done.
lsas loop			
assembler code	e for fu	nction	loop:
000000000000000000000000000000000000000	<+0>:	mov	\$0x0,%eax
000000000000000000000000000000000000000	<+5>:	jmp	0xa <loop+10></loop+10>
0000000000000007	<+7>:	add	\$0x1,%eax
0000000000000000000	<+10>:	cmp	\$0x63,%eax
b000000000000d	<+13>:	jle	0x7 <loop+7></loop+7>
1000000000000000	<+15>:	repz re	etq
assembler dump.			

### Set %eax to 0







Compile to an object file:

gcc -c -Og while loop.c

nile_loop.o		
get architecture is	assumed	to be i386:x86
symbols from while	_loop.o	.done.
isas loop		
assembler code for	function	loop:
0000000000000 <+0>	: mov	\$0x0,%eax
00000000000000005 <+5>	: jmp	0xa <loop+10></loop+10>
0000000000007 <+7>	: add	\$0x1,%eax
)0000000000000a <+10	>: cmp	\$0x63,%eax
)000000000000d <+13	>: jle	0x7 <loop+7></loop+7>
)000000000000f <+15	>: repz r	retq
assembler dump.		





	<pre>\$ gdb while_loop.o</pre>			
vora roop()	The target architecture is assumed to be i386:x86 Reading symbols from while_loop.odone. (gdb) disas loop			
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}	0x000000000000000 <+13>: jle 0x7 <loop+7> 0x000000000000000 &lt;+15&gt;: repz retq End of assembler dump.</loop+7>			

Compile to an object file:

gcc -c -Og while loop.c

compare % eax to 0x63 (99d) by subtracting % eax - 0x63, setting the Sign Flag (SF) because the result is negative.





	<pre>\$ gdb while_loop.o</pre>				
void loop() {	The target architecture is assumed to be i386:x86 Reading symbols from while_loop.odone. (gdb) disas loop				
<pre>int i = 0; while (i &lt; 100) { ++i; }</pre>	<pre>Dump of assembler code for function loop:</pre>				
} }	<pre>0x00000000000000 &lt;+13&gt;: jle 0x7 <loop+7> 0x000000000000000 &lt;+15&gt;: repz retq End of assembler dump.</loop+7></pre>				

Compile to an object file:

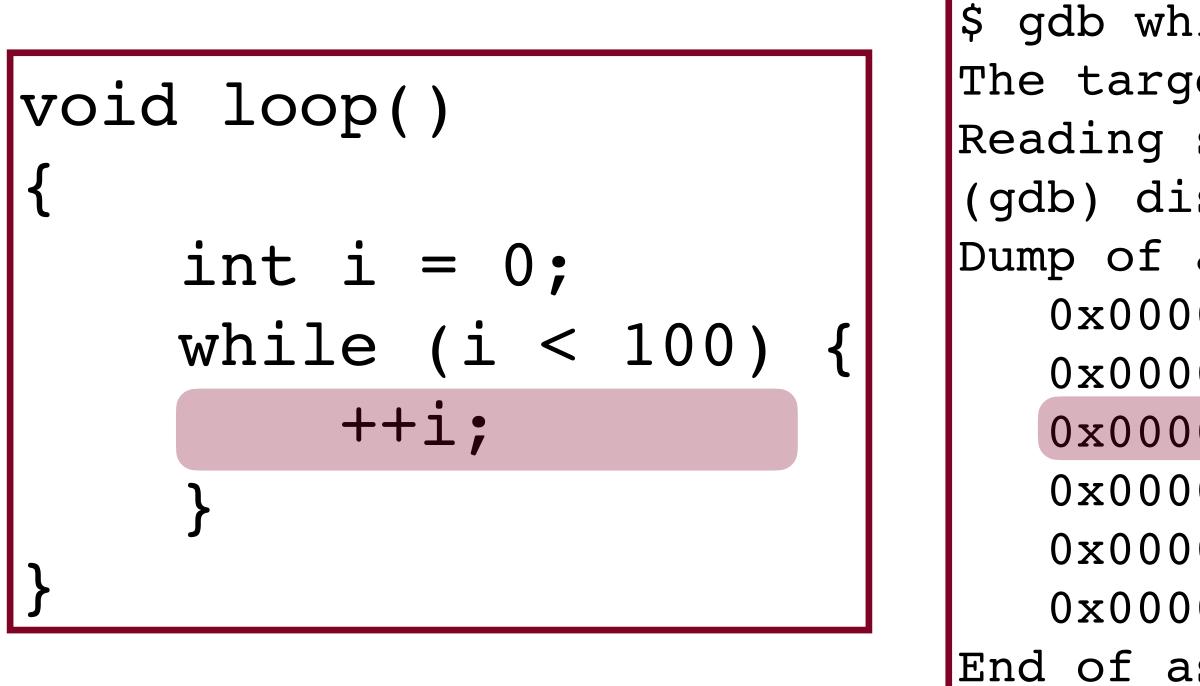
gcc -c -Og while loop.c

jle is "jump less than or equal." The Sign Flag indicates that the result was negative (less than), so we jump to  $0 \times 7$ .

### %rax: 0







Compile to an object file:

gcc -c -Og while loop.c

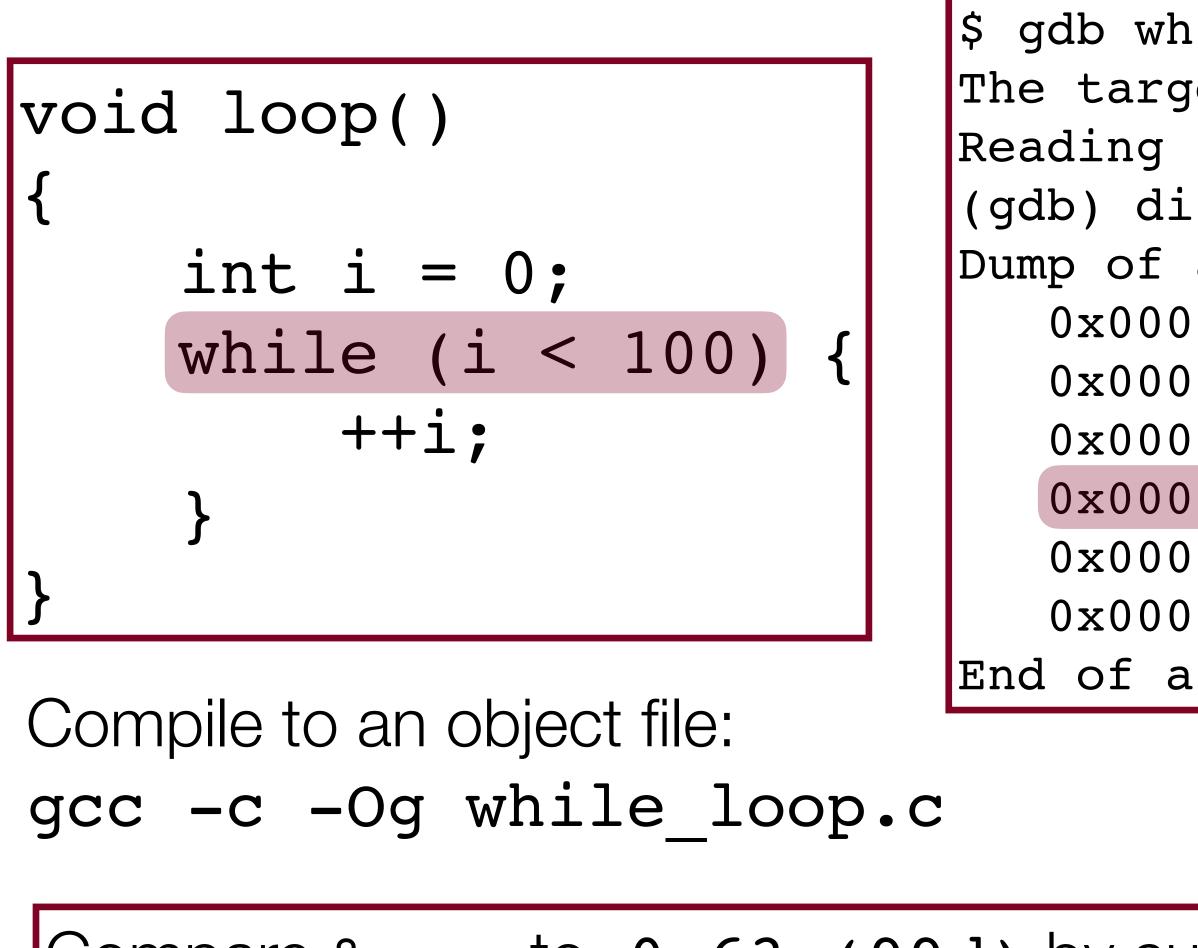


nile_loop.o	_	_				
get architectur	re is as	sumed t	o be i386:x86			
symbols from while loop.odone.						
isas loop						
assembler code	e for fu	nction	loop:			
000000000000000000000000000000000000000	<+0>:	mov	\$0x0,%eax			
000000000000000000000000000000000000000	<+5>:	jmp	0xa <loop+10></loop+10>			
0000000000000007	<+7>:	add	\$0x1,%eax			
000000000000000000a	<+10>:	cmp	\$0x63,%eax			
0000000000000d	<+13>:	jle	0x7 <loop+7></loop+7>			
100000000000000	<+15>:	repz re	etq			
assembler dump.						

Add 1 to %eax







nile_loop.o		
get architecture i	s assumed t	to be i386:x86
symbols from while	e_loop.o	.done.
lsas loop		
assembler code for	r function	loop:
000000000000000000 <+0	>: mov	\$0x0,%eax
000000000000000000000000000000000000000	>: jmp	0xa <loop+10></loop+10>
0000000000007 <+7	>: add	\$0x1,%eax
)0000000000000a <+1	0>: cmp	\$0x63,%eax
)000000000000d <+1	3>: jle	0x7 <loop+7></loop+7>
)000000000000f <+1	5>: repz r	etq
assembler dump.		

Compare %eax to 0x63 (99d) by subtracting %eax - 0x63. When %rax is 0, what flags change based on the the comparison? (We care about **Zero** Flag, Sign Flag, Carry Flag, and Overflow Flag): 0 - 99, so SF and CF





	<pre>\$ gdb while_loop.o</pre>
void loop() {	The target architecture is assumed to be i386:x86 Reading symbols from while_loop.odone. (gdb) disas loop
<pre>int i = 0; while (i &lt; 100) {     ++i; }</pre>	<pre>Dump of assembler code for function loop:</pre>
} Compoile to op object file:	0x000000000000000000f <+15>: repz retq End of assembler dump.

Compile to an object file:

gcc -c -Og while loop.c



### %rax: 1

Eventually, this will become positive (when Seax is 100), and the loop will end.





	<pre>\$ gdb while_loop.o</pre>
	<pre>The target architecture is assumed to be i386:x86 Reading symbols from while_loop.odone. (gdb) disas loop Dump of assembler code for function loop:</pre>
Compute to operation tiles	0x00000000000000000000 <+15>: repz retq End of assembler dump.

Compile to an object file:

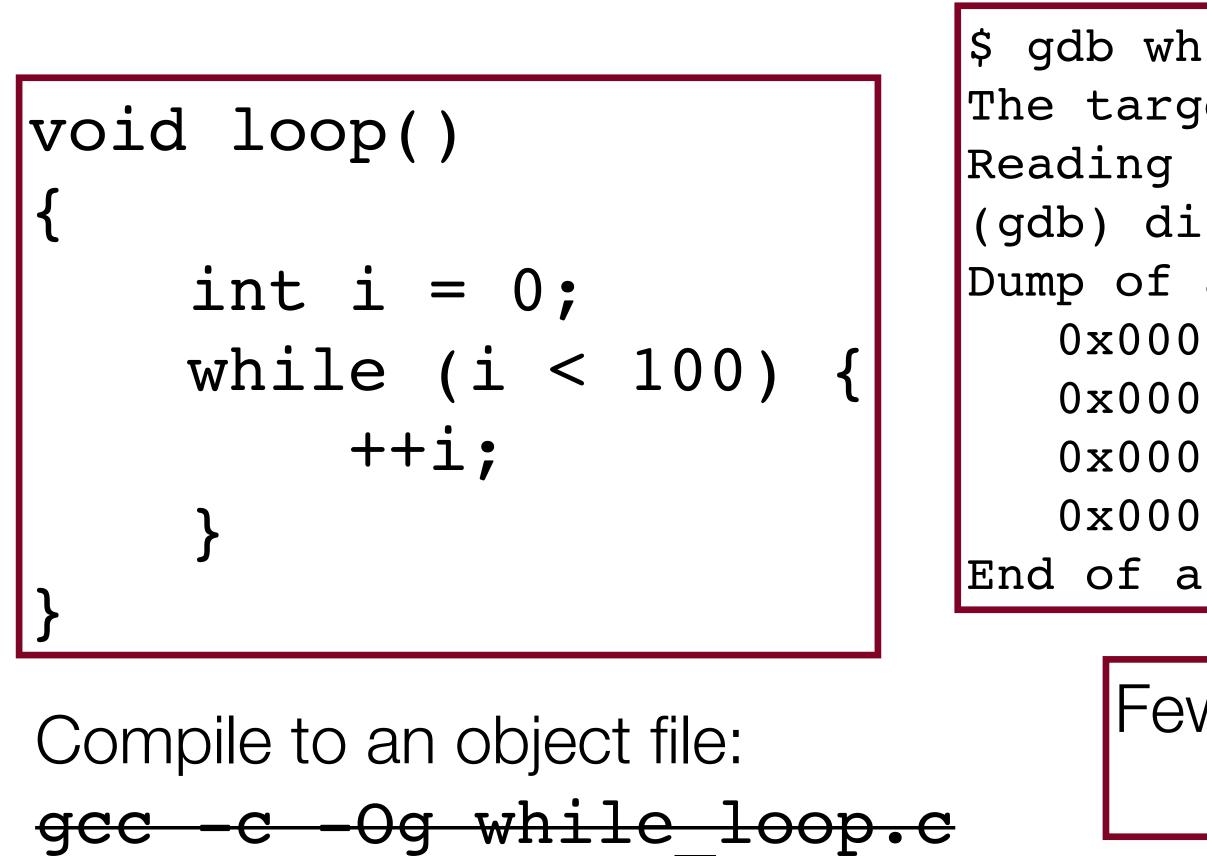
gcc -c -Og while loop.c



### Could the compiler have done better with this loop?







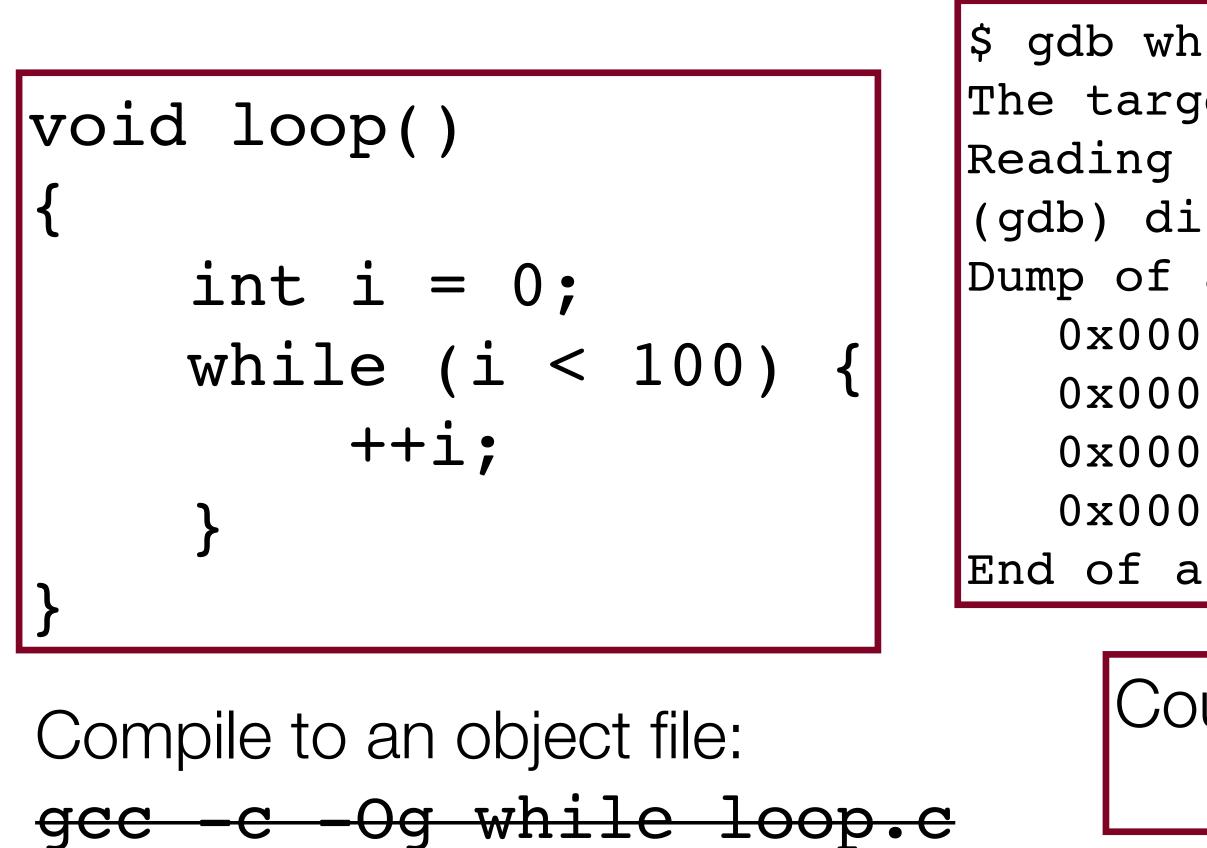
gcc - c - 01 while loop.c

nile_loop.o	
get architecture is assumed	to be i386:x86
symbols from while loop.o.	done.
isas loop	
assembler code for functio	n loop:
)000000000000 <+0>: mov	\$0x64,%eax
0000000000005 <+5>: sub	\$0x1,%eax
)0000000000008 <+8>: jne	0x5 <loop+5></loop+5>
00000000000000a <+10>: repz	retq
assembler dump.	

Fewer lines, less jumping!







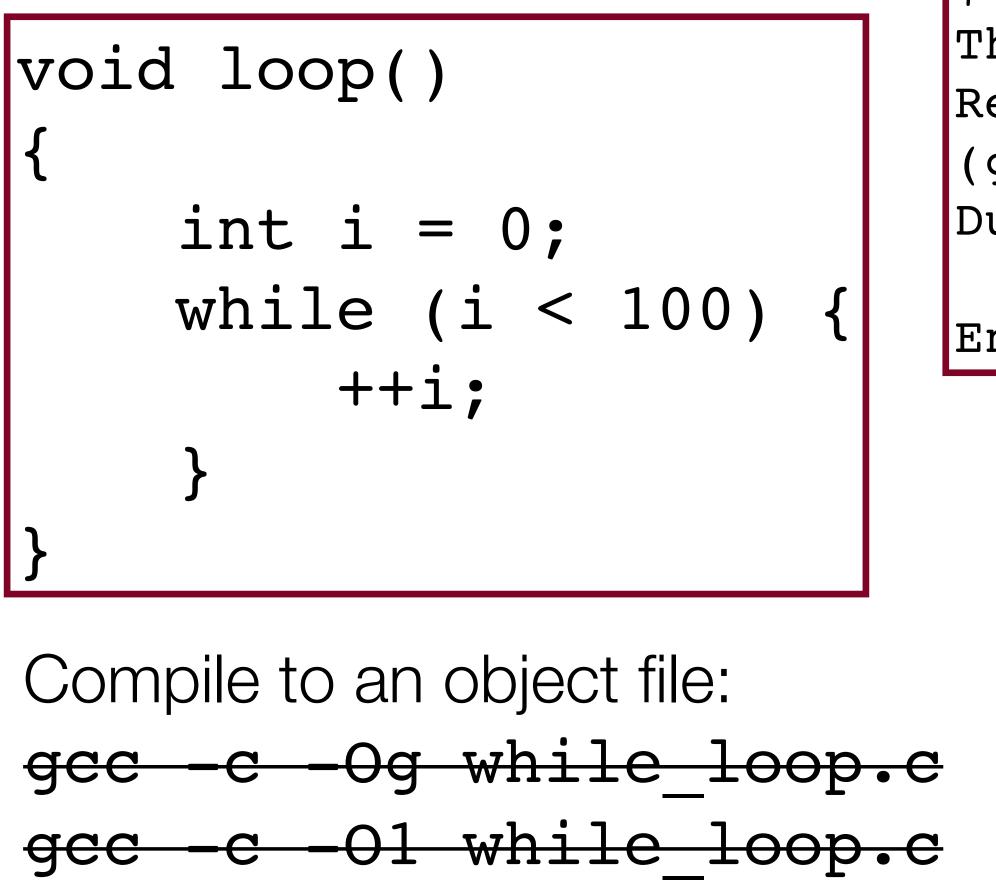
gcc -c -01 while loop.c

nile_loop.o	
get architecture is a	assumed to be i386:x86
symbols from while_1	Loop.odone.
lsas loop	
assembler code for f	Eunction loop:
)0000000000000 <+0>:	mov \$0x64,%eax
00000000000000005 <+5>:	sub \$0x1,%eax
)000000000008 <+8>:	jne 0x5 <loop+5></loop+5>
)0000000000000a <+10>:	: repz retq
assembler dump.	

Could we do better?







gcc -c -O2 while loop.c

\$ gdb while loop.o The target architecture is assumed to be i386:x86-64 Reading symbols from while loop.o...done. (gdb) disas loop Dump of assembler code for function loop: 0x00000000000000 <+0>: repz retq End of assembler dump.



Sure! As the optimization level goes up, gcc gets smarter! The compiler realized that this loop is not doing anything, so it completely optimized it out!







- machine code.
- It is instructive in this case to look at the machine code for some jump instructions, just to see how the underlying machine is referencing where to jump.
- Remember, %rip is the instruction pointer, which has an address of the current instruction.
  - Well...kind of. On older x86 machines, when an instruction was executing, the first thing that happened was that <code>%rip</code> is changed to point to the next instruction. The instruction set has retained this behavior.
  - Jump instructions are often encoded to jump relative to \$rip. Let's see what that means in practice...

• As we have mentioned before, assembly language is still one step higher than



• Let's look at our while loop again:

```
void loop()
    int i = 0;
    while (i < 100)
        ++i;
```

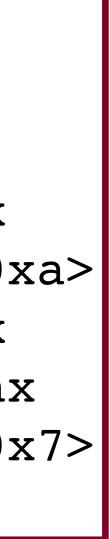
Compile to an object file: gcc -c -Og while loop.c

D	i	S	a	S
0	0	0	0	0
			0	•
			5	•
			7	•
			a	•
			d	•
			f	•

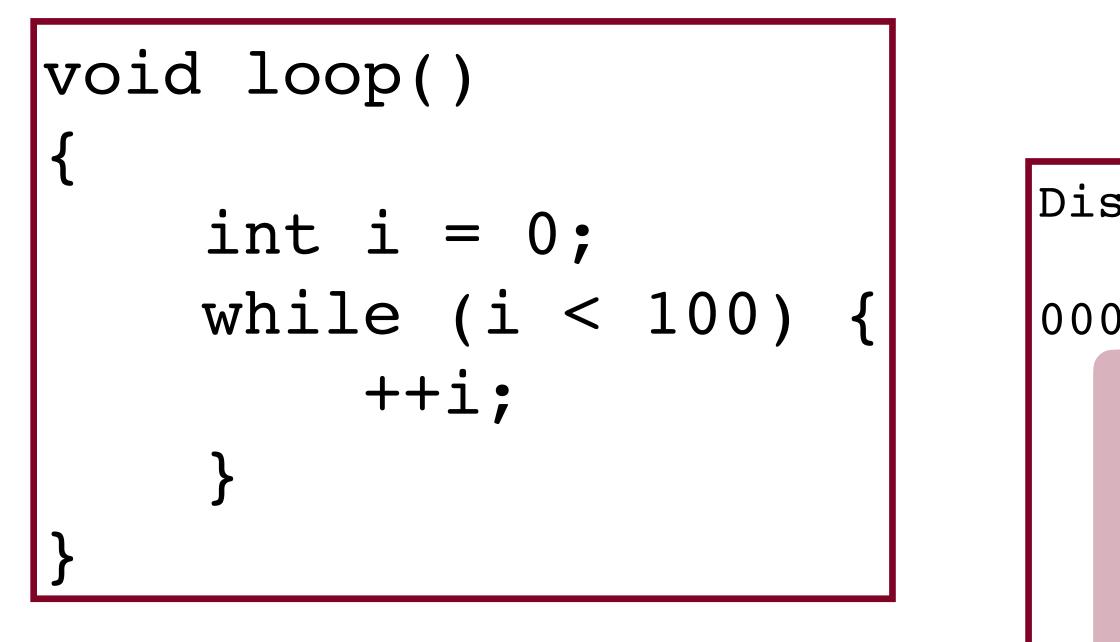
### Run the objdump program: objdump -d while loop.o

```
sembly of section .text:
 )00000000000 <loop>:
  b8 00 00 00 00
                                  $0x0,%eax
                           MOV
  eb 03
                                  a <loop+0xa>
                           jmp
  83 c0 01
                                  $0x1,%eax
                           add
  83 f8 63
                                  $0x63,%eax
                           cmp
  7e f8
                                  7 < loop+0x7>
                           jle
f: f3 c3
                           repz retq
```





• Take the following function:

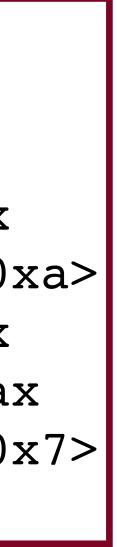


Compile to an object file: gcc -c -Og while loop.c Run the objdump program: objdump -d while loop.o

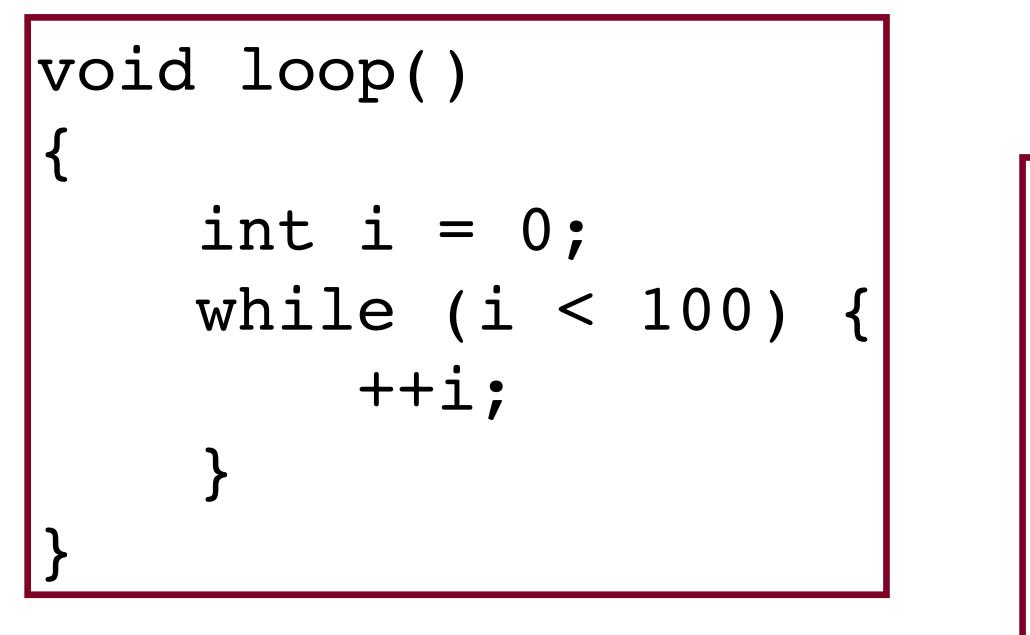
```
Disassembly of section .text:
00000000000000000000 <loop>:
   0: b8 00 00 00 00
                                       $0x0,%eax
                               mov
   5: eb 03
                                       a <loop+0xa>
                               jmp
   7: 83 c0 01
                                       $0x1,%eax
                               add
   a: 83 f8 63
                                       $0x63,%eax
                               cmp
   d: 7e f8
                                       7 < 100p + 0x7 >
                               jle
   f: f3 c3
                               repz retq
```

0-based addresses for each instruction (will be replaced with real addresses when a full program is created)

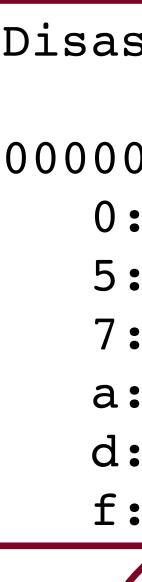




• Take the following function:



Compile to an object file: gcc -c -Og while loop.c

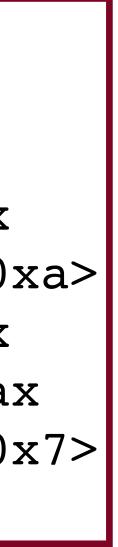


Run the objdump program: objdump -d while loop.o

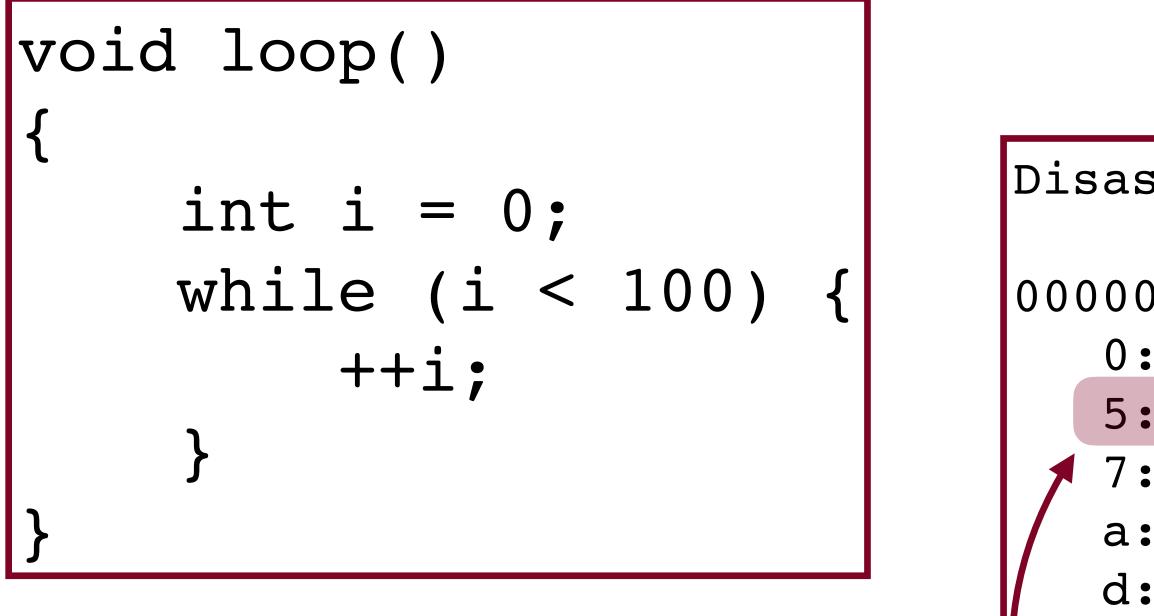
```
Disassembly of section .text:
00000000000000000000 <loop>:
   0: b8 00 00 00 00
                                       $0x0,%eax
                               mov
   5: eb 03
                                       a <loop+0xa>
                               jmp
   7: 83 c0 01
                                       $0x1,%eax
                               add
   a: 83 f8 63
                                       $0x63,%eax
                               cmp
                                       7 < 100p + 0x7 >
   d: 7e f8
                               jle
   f: f3 c3
                               repz retq
```

Machine code for the instructions. Instructions are "variable length" the mov instruction is 5 bytes, the tmp is 3 bytes, etc.





• Take the following function:



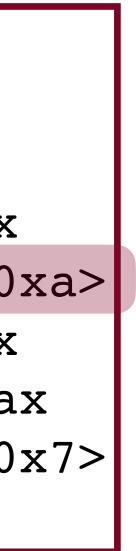
Compile to an object file: gcc -c -Og while\_loop.c

0: 5: 7: a: d: f: Run the objdump program: objdump -d while loop.o

```
Disassembly of section .text:
```

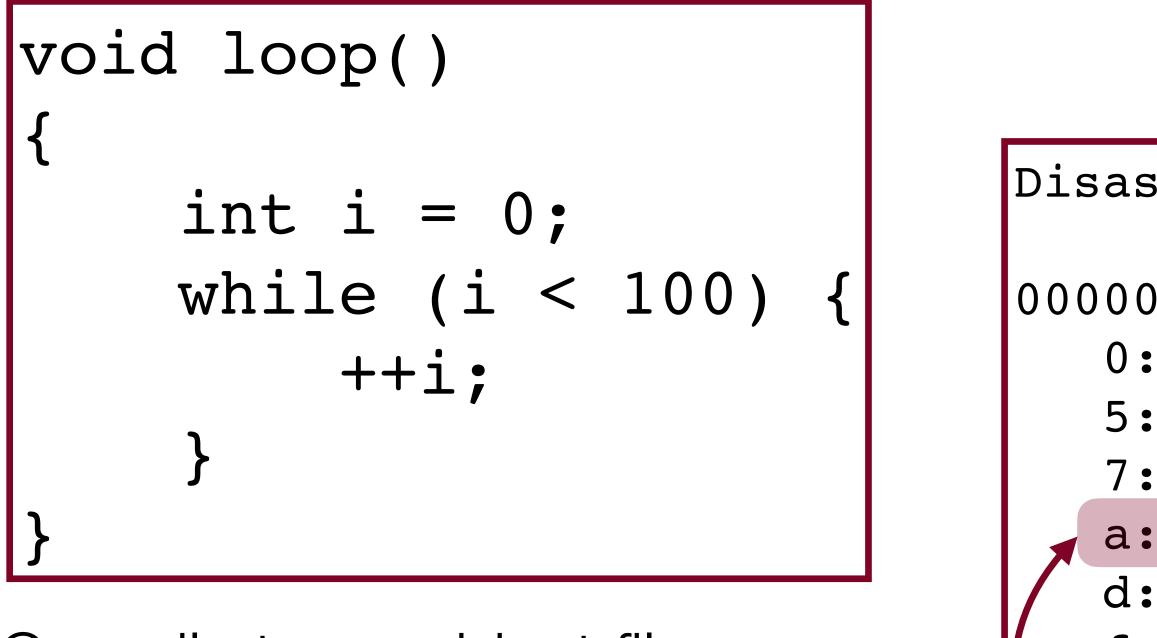
0	0000	000	00000	<loop>:</loop>		
•	b8	00	00 00	00	mov	\$0x0,%eax
•	eb	03			jmp	a <loop+0:< td=""></loop+0:<>
•	83	c0	01		add	\$0x1,%eax
•	83	f8	63		cmp	\$0x63,%ea
•	7e	f8			jle	7 <loop+0:< td=""></loop+0:<>
•	f3	<b>c</b> 3			repz	retq

The jmp instruction. "eb" means that this is a jmp, and 03 is the number of instructions to jump, relative to %rip. When the instruction is executing, %rip is set to the next instruction (7 in this case). So...7 + is 0xa, so this instruction jumps to 0xa.





• Take the following function:

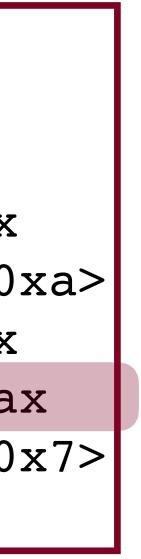


Compile to an object file: gcc -c -Og while\_loop.c Run the objdump program: objdump -d while\_loop.o

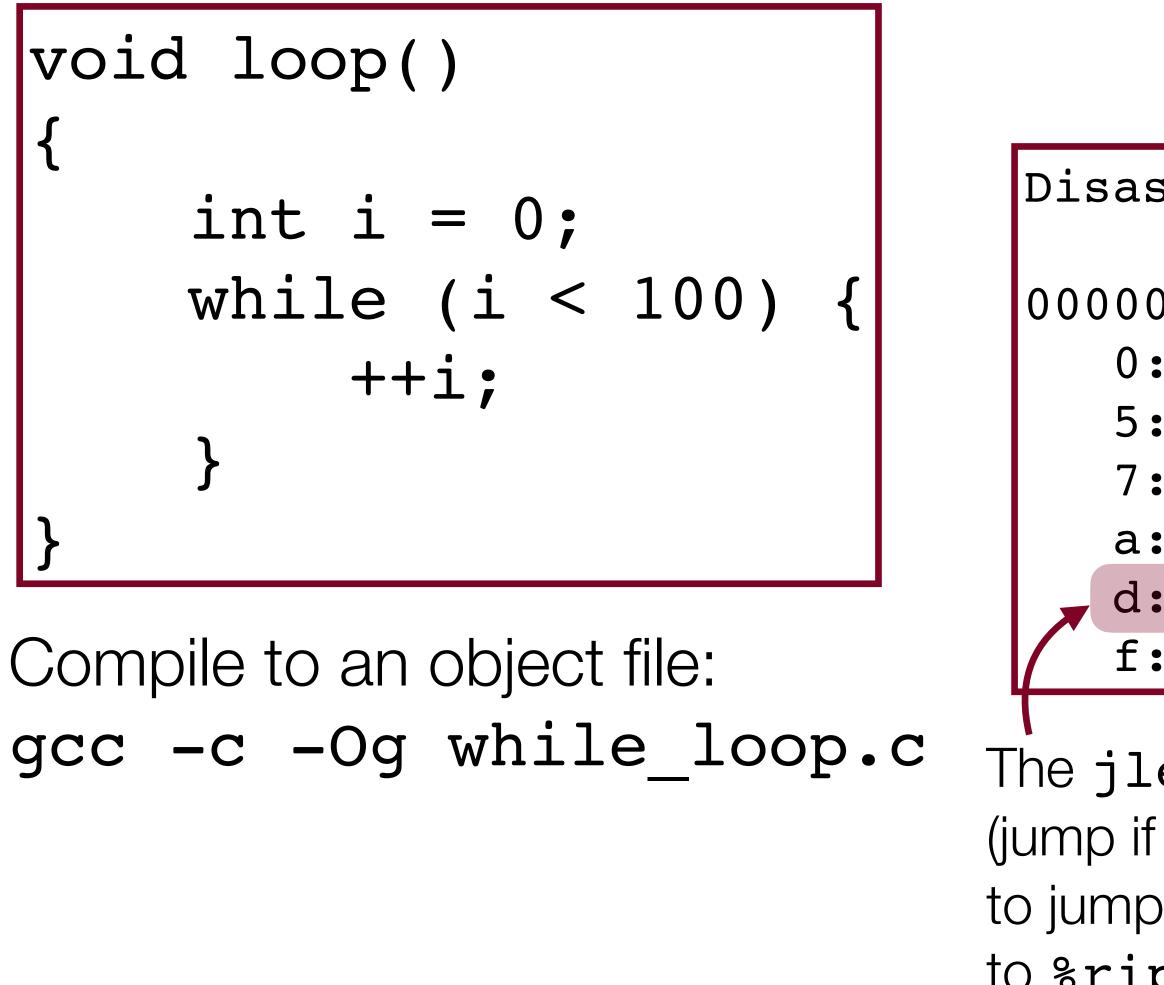
sass	semb	oly	of	se	ction	1.	text:				
000	000	000	000	0	<loop< td=""><td>)&gt;:</td><td></td><td></td><td></td><td></td><td></td></loop<>	)>:					
0:	b8	00	00	00	00			mov	\$(	)x0,	%eax
5:	eb	03						jmp	a	<10	op+0
7:	83	<b>c</b> 0	01					add	\$(	)x1,	%eax
a:	83	f8	63					cmp	\$(	)x63	,%ea
d:	7e	f8						jle	7	<10	op+0
f:	f3	<b>c</b> 3						repz	reto	1	

The **cmp** instruction. Notice that the 0x63 is embedded into the machine code, because it is an immediate value.





• Take the following function:

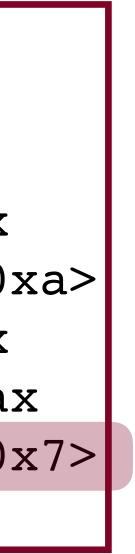


Run the objdump program: objdump -d while loop.o

```
Disassembly of section .text:
00000000000000000000 <loop>:
                                      $0x0,%eax
   0: b8 00 00 00 00
                               MOV
   5: eb 03
                                       a <loop+0xa>
                               jmp
   7: 83 c0 01
                                      $0x1,%eax
                               add
   a: 83 f8 63
                                      $0x63,%eax
                               cmp
   d: 7e f8
                                       7 < 100p + 0x7 >
                               jle
   f: f3 c3
                               repz retq
```

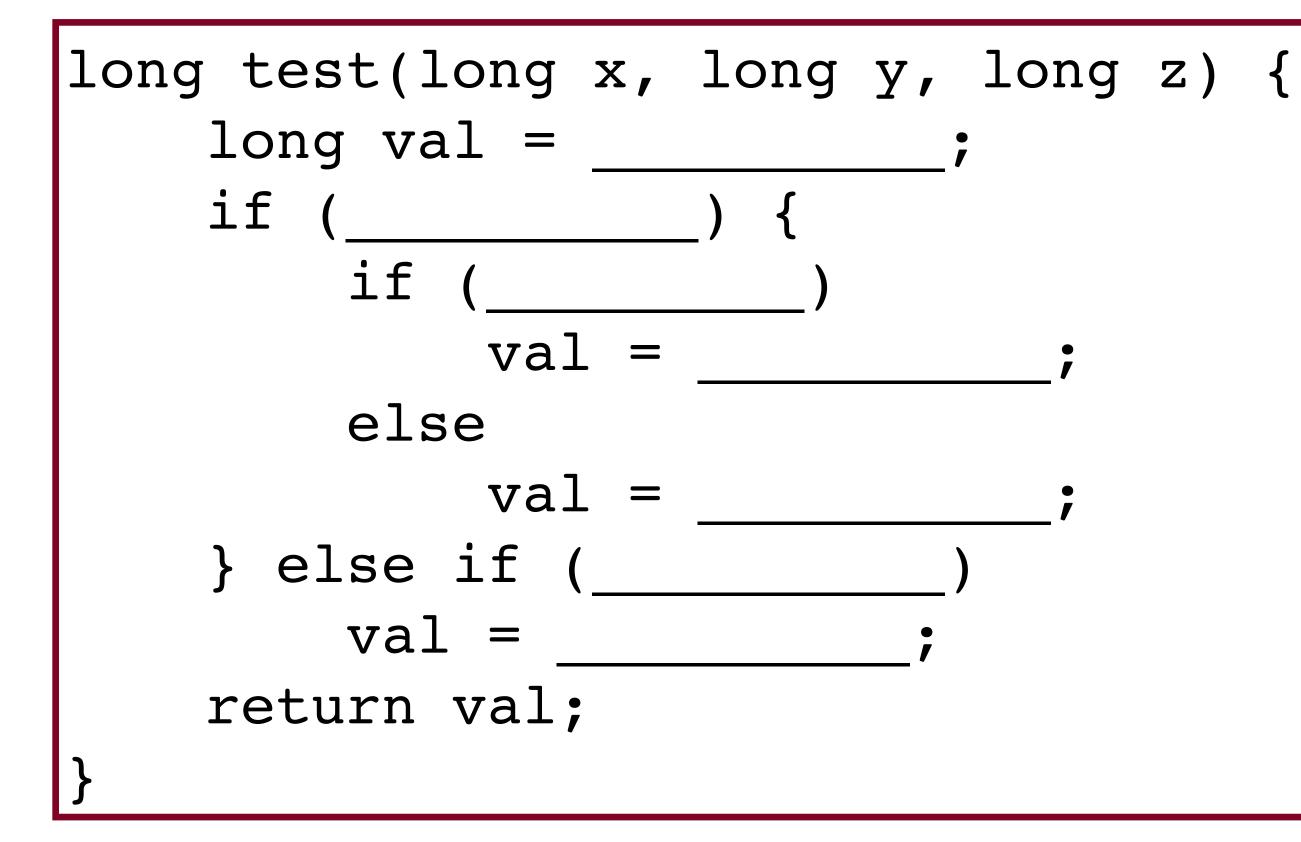
The jle instruction. "7e" means that this is a jle (jump if less than), and f8 is the number of instructions to jump (in two's complement! So, it means -8), relative to rip, which is at 0xf when the instruction is running. So, 0xf - 8 is 0xa, so this instruction jumps to 0x7.





### Practice: Reverse-engineer Assembly to C

• Take the following function:



```
# x in %rdi, y in %rsi, z in %rdx
test:
    leaq (%rdi,%rsi), %rax
    addq %rdx, %rax
    cmpq $-3, %rdi
    jge .L2
    cmpq %rdx, %rsi
    jge .L3
    movq %rdi, %rax
    imulq %rsi, %rax
    ret
.L3:
    movq %rsi, %rax
    imulq %rdx, %rax
    ret
.L2:
    cmpq $2, %rdi
    jle .L4
    movq %rdi, %rax
    imulq %rdx, %rax
.L4:
    rep; ret
```



### Practice: Reverse-engineer Assembly to C

• Take the following function:

```
long test(long x, long y, long z) {
    long val = x + y + z;
    if (x < -3) {
        if (y < z)
            val = x * y;
        else
            val = y * z;
    } else if (x > 2)
        val = x * z;
    return val;
```

```
# x in %rdi, y in %rsi, z in %rdx
test:
    leaq (%rdi, %rsi), %rax
    addq %rdx, %rax
    cmpq $-3, %rdi
    jge .L2
    cmpq %rdx, %rsi
    jge .L3
    movq %rdi, %rax
    imulq %rsi, %rax
    ret
.L3:
    movq %rsi, %rax
    imulq %rdx, %rax
    ret
.L2:
    cmpq $2, %rdi
    jle .L4
    movq %rdi, %rax
    imulq %rdx, %rax
.L4:
    rep; ret
```



### Conditional Moves

analogous to the jump instructions:

Instruction	Synonym	Move Condition
cmove S,R	cmovz	Equal / zero (ZF=1)
cmovne S,R	cmovnz	Not equal / not zero (ZF=0)
cmovs S,R		Negative (SF=1)
cmovns S,R		Nonnegative (SF=0)
cmovg S,R	cmovnle	Greater (signed >) (SF=0 ar
cmovge S,R	cmovnl	Greater or equal (signed >=
cmovl S,R	cmovnge	Less (signed <) (SF != OF)
cmovle S,R	cmovng	Less or equal (signed $\leq$ =) (2
cmova S,R	cmovnbe	Above (unsigned >) (CF = 0
cmovae S,R	cmovnb	Above or equal (unsigned >
cmovb S,R	cmovnae	Below (unsigned <) (CF = 1
cmovbe S,R	cmovna	Below or equal (unsigned <

 The x86 processor provides a set of "conditional move" instructions that move memory based on the result of the condition codes, and that are completely

- Ind SF=OF) =) (SF=OF)
- (ZF=1 or SF!=OF) 0 and ZF = 0) >=) (CF = 0)<=) (CF = 1 or ZF = 1)
- With these instructions, we can sometimes eliminate branches, which are particularly inefficient on modern computer hardware.



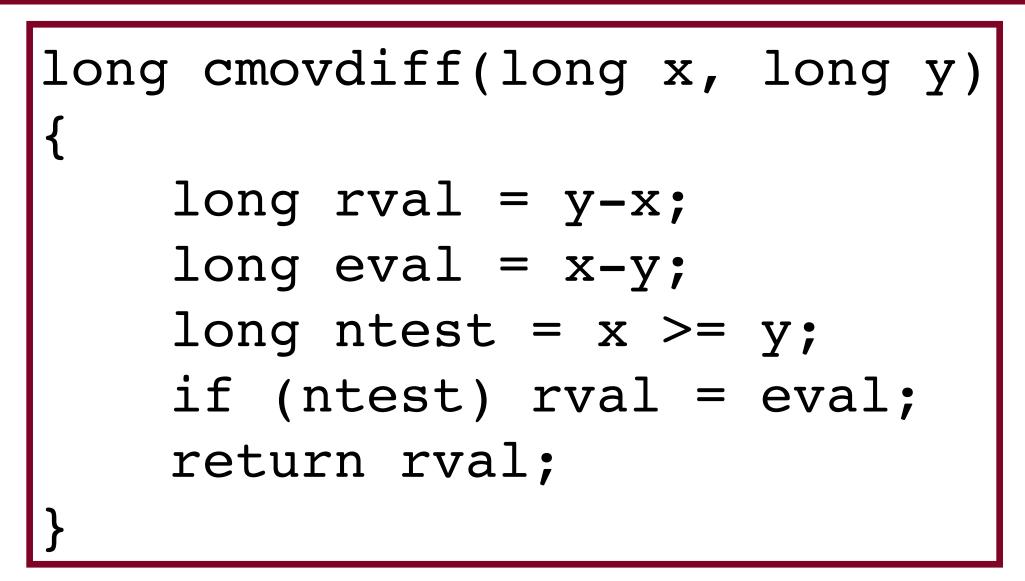


### Jumps -vs- Conditional Move

# long absdiff(long x, long y) { long result; if (x < y) result = y - x; else result = x - y; return result; }</pre>

# x in %rdi, y in %rsi
absdiff:
 cmpq %rsi, %rdi
 jge .L2
 movq %rsi, %rax
 subq %rdi, %rax
 ret
.L2:
 movq %rdi, %rax
 subq %rsi, %rax
 ret

Which is faster? Let's test!



# x	in %r	di, y	in %rsi
cmov	vdiff:		
	movq	%rsi,	%rax
	subq	%rdi,	%rax
	movq	%rdi,	%rdx
	subq	%rsi,	%rdx
	cmpq	%rsi,	%rdi
	cmovo	ge %rdx	x, %rax
	ret		



### References and Advanced Reading

- References: ullet
  - x86-64.html
  - onepage x86-64.pdf
  - gdbtui: <u>https://beej.us/guide/bggdb/</u> •
  - More gdbtui: <u>https://sourceware.org/gdb/onlinedocs/gdb/TUI.html</u> •
  - Compiler explorer: <u>https://gcc.godbolt.org</u> •
- Advanced Reading:
  - default/files/managed/39/c5/325462-sdm-vol-1-2abcd-3abcd.pdf
  - history of x86 instructions: <u>https://en.wikipedia.org/wiki/</u> • X86 instruction listings
  - x86-64 Wikipedia: https://en.wikipedia.org/wiki/X86-64 ullet

### Stanford guide to x86-64: <u>https://web.stanford.edu/class/cs107/guide/</u>

### CS107 one-page of x86-64: <u>https://web.stanford.edu/class/cs107/resources/</u>

x86-64 Intel Software Developer manual: <u>https://software.intel.com/sites/</u>



