# <u>https://forms.gle/uGUBDvKyT</u> <u>uZHrrbK7</u>

#### Code: mov



### CS 107, Lecture 11 Assembly Continued

Reading: B&O 3.1-3.4

#### mov

The **mov** instruction <u>copies</u> bytes from one place to another; it is similar to the assignment operator (=) in C.

mov src,dst

The **src** and **dst** can each be one of:

- Immediate (constant value, like a number) (only src)
- Register
- Memory Location
   (at most one of src, dst)

Direct address

%rbx

0x6005c0

\$0x104

# **Operand Forms: Immediate**

mov



Copy the value 0x104 into some destination.

# **Operand Forms: Registers**



# **Operand Forms: Absolute Addresses**



# **Operand Forms: Indirect**

MOV

mov

Copy the value at the address stored in register %rbx into some destination. (%rbx), , (%rbx) Copy the value from some source into the memory at the address stored in register %rbx. 41

# **Operand Forms: Base + Displacement**

0x10(%rax),

Copy the value at the address (<u>0x10 plus</u> what is stored in register %rax) into some destination.

## mov

mov

,0x10(%rax)

Copy the value from some source into the memory at the address (<u>0x10</u> <u>plus</u> what is stored in register %rax).42

# **Operand Forms: Indexed**

(%rax,%rdx),

Copy the value at the address which is (the sum of the values in registers %rax and %rdx) into some destination.

#### mov

mov

.,(%rax,%rdx)

Copy the value from some source into the memory at the address which is (the sum of the values in registers %rax and %rdx). 43

# **Operand Forms: Indexed**

Copy the value at the address which is (the sum of **0x10 plus** the values in registers %rax and %rdx) into some destination.

mov

# %rax and %rdx) into some destination. 0x10(%rax,%rdx),

mov

,0x10(%rax,%rdx)

Copy the value from some source into the memory at the address which is (the sum of <u>0x10</u> <u>**blus**</u> the values in registers %rax and %rdx).

# **Practice #2: Operand Forms**

What are the results of the following move instructions (executed separately)? For this problem, assume the value *0x11* is stored at address *0x10C*, *0xAB* is stored at address *0x104*, *0x100* is stored in register %rax and *0x3* is stored in %rdx.

- 1. mov \$0x42,(%rax)
- 2. mov 4(%rax),%rcx
- 3. mov 9(%rax,%rdx),%rcx





0x4(,%rdx,4),

Copy the value at the address which is (4 times the value in register %rdx, <u>plus</u> <u>0x4)</u>, into some destination.

mov

mov

,0x4(,%rdx,4)

Copy the value from some source into the memory at the address which is (4 times the value in register %rdx, **plus 0x4).** 4

Copy the value at the address which is (<u>the</u> <u>value in register %rax</u> plus 2 times the value in register %rdx) into some destination. (%rax,%rdx,2),

mov

mov

,(%rax,%rdx,2)

Copy the value from some source into the memory at the address which is (<u>the value in register %rax</u> plus 2 times the value in register %rdx).

Copy the value at the address which is (<u>0x4 plus</u> the value in register %rax plus 2 times the value in register %rdx) into some destination.

mov

# register %rdx) into some destination. 0x4(%rax,%rdx,2),

mov

,0x4(%rax,%rdx,2)

Copy the value from some source into the memory at the address which is (**0x4 plus** the value in register %rax plus 2 times the value in register %rdx). 49

# **Most General Operand Form**

# $Imm(r_b, r_i, s)$

# is equivalent to...

# $Imm + R[r_b] + R[r_i]*s$

# **Most General Operand Form**



# **Operand Forms**

Туре	Form	Operand Value	Name
Immediate	\$Imm	Imm	Immediate
Register	<i>r</i> !	R[ <i>r</i> <sub>!</sub> ]	Register
Memory	Imm	M[ <i>Imm</i> ]	Absolute
Memory	( <i>r</i> <sub>!</sub> )	$M[R[r_{!}]]$	Indirect
Memory	Imm(r <sub>"</sub> )	$M[Imm + R[r_{"}]]$	Base + displacement
Memory	( <i>r</i> ", <i>r</i> #)	$M[R[r_{"}] + R[r_{\#}]]$	Indexed
Memory	Imm(r <sub>"</sub> , r <sub>#</sub> )	$M[Imm + R[r_{"}] + R[r_{\#}]]$	Indexed
Memory	(, r#, s)	M[R[ <i>r</i> #] . <i>s</i> ]	Scaled indexed
Memory	Imm(, r#, s)	$M[Imm + R[r_{\#}] \cdot s]$	Scaled indexed
Memory	( <i>r</i> ", <i>r</i> #, <i>s</i> )	$M[R[r_{"}] + R[r_{\#}] . s]$	Scaled indexed
Memory	$Imm(r_{, r_{\#}, s)$	$M[Imm + R[r_{"}] + R[r_{\#}] \cdot s]$	Scaled indexed

**Figure 3.3 from the book: "Operand forms.** Operands can denote immediate (constant) values, register values, or values from memory. The scaling factor *s* must be either. 1, 2, 4, or 8."

# **Practice #3: Operand Forms**

What are the results of the following move instructions (executed separately)? For this problem, assume the value *0x1* is stored in register %rcx, the value *0x100* is stored in register %rax, the value *0x3* is stored in register %rdx, and value *0x11* is stored at address *0x10C*.

1. mov \$0x42,0xfc(,%rcx,4)

2. mov (%rax,%rdx,4),%rbx

# Goals of indirect addressing: C

# Why are there so many forms of indirect addressing?

We see these indirect addressing paradigms in C as well!

# **Our First Assembly**

<pre>int sum_array(int arr[], in     int sum = 0;</pre>	nt nelems) {	We're 1/4 <sup>th</sup> of the way to understanding assembly! What looks understandable right now?		
<pre>for (int i = 0; i &lt; nele     sum += arr[i]; } return sum; }</pre>	ems; i++) {	Some notes: • Registers store addresses and values • mov src, dst <i>copies</i> value into dst • sizeof(int) is 4 • Instructions executed sequentially		
00000000004005b6 <sum_array< td=""><td><pre>/&gt;:</pre></td><td></td><td></td></sum_array<>	<pre>/&gt;:</pre>			
4005b6: ba 00 00 00 00	) mov	\$0x0,%edx		
4005bb: b8 00 00 00 00	) mov	\$0x0,%eax		
4005c0: eb 09	jmp	4005cb <sum array+0x15=""></sum>		
4005c2: 48 63 ca	movslq	%edx,%rcx		
4005c5: 03 04 8f	add	(%rdi,%rcx,4),%eax		
1005c8· 83 c7 01	add	\$0x1,%edx		
We'll come back to this	cmp	%esi,%edx	••	
example in future lectures!	jl'	4005c2 <sum_array+0xc></sum_array+0xc>		
	ιτρειτ		55	

# Why are we reading assembly?



#### Main goal: Information retrieval

- We will not be writing assembly! (that's the compiler's job)
- Rather, we want to translate the assembly **back** into our C code.
- Knowing how our C code is converted into machine instructions gives us insight into how to write more efficient, cleaner code.

# **Extended warmup: Information Synthesis**

Spend a few minutes thinking about the main paradigms of the mov instruction.

- What might be the equivalent C-like operation?
- Examples (note %r\_\_\_ registers are 64-bit):
- 1. mov \$0x0,%rdx
- 2. mov %rdx,%rcx
- 3. mov \$0x42,(%rdi)
- 4. mov (%rax,%rcx,8),%rax



# **Extended warmup: Information Synthesis**

Spend a few minutes thinking about the main paradigms of the mov instruction.

- What might be the equivalent C-like operation?
- Examples (note %r\_\_\_ registers are 64-bit):
- 1. mov \$0x0, %rdx \$maybe long x = 0
- 2. mov %rdx,%rcx -> maybe long x = y;
- 3. mov \$0x42,(%rdi) -> maybe \*ptr = 0x42;
- 4. mov (%rax,%rcx,8),%rax -> maybe long x = arr[i];

Indirect addressing is like pointer arithmetic/deref!



# **Lecture Plan**

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• The <b>lea</b> Instruction	24
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**Reference Sheet**: cs107.stanford.edu/resources/x86-64-reference.pdf See more guides on Resources page of course website!

# **Helpful Assembly Resources**

- Course textbook (reminder: see relevant readings for each lecture on the Schedule page, <u>http://cs107.stanford.edu/schedule.html</u>)
- CS107 Assembly Reference Sheet: <u>http://cs107.stanford.edu/resources/x86-64-reference.pdf</u>
- CS107 Guide to x86-64: <u>http://cs107.stanford.edu/guide/x86-64.html</u>

# References and Advanced Reading

- References:
  - Stanford guide to x86-64: <u>https://web.stanford.edu/class/cs107/guide/</u> x86-64.html
  - CS107 one-page of x86-64: <u>https://web.stanford.edu/class/cs107/resources/</u> onepage x86-64.pdf
  - gdbtui: <u>https://beej.us/guide/bggdb/</u>
  - More gdbtui: <u>https://sourceware.org/gdb/onlinedocs/gdb/TUI.html</u>
  - Compiler explorer: <u>https://gcc.godbolt.org</u>
- Advanced Reading:
  - x86-64 Intel Software Developer manual: <u>https://software.intel.com/sites/</u> <u>default/files/managed/39/c5/325462-sdm-vol-1-2abcd-3abcd.pdf</u>
  - history of x86 instructions: <u>https://en.wikipedia.org/wiki/</u> X86 instruction listings
  - x86-64 Wikipedia: <u>https://en.wikipedia.org/wiki/X86-64</u>



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#### mov

The **mov** instruction <u>copies</u> bytes from one place to another; it is similar to the assignment operator (=) in C.

mov src,dst

The **src** and **dst** can each be one of:

- Immediate (constant value, like a number) (only src)
- Register
- Memory Location
   (at most one of src, dst)

# **Memory Location Syntax**

Syntax	Meaning	
0x104	Address 0x104 (no \$)	
(%rax)	What's in %rax	
4(%rax)	What's in %rax, plus 4	
(%rax, %rdx)	Sum of what's in %rax and %rdx	
4(%rax, %rdx)	Sum of values in %rax and %rdx, plus 4	
(, %rcx, 4)	What's in %rcx, times 4 (multiplier can be 1, 2, 4, 8)	
(%rax, %rcx, 2)	What's in %rax, plus 2 times what's in %rcx	
8(%rax, %rcx, 2) 8(%rax, %rcx, 2)		

# **Operand Forms**

Туре	Form	Operand Value	Name
Immediate	\$Imm	Imm	Immediate
Register	<i>r</i> !	R[ <i>r</i> <sub>!</sub> ]	Register
Memory	Imm	M[ <i>Imm</i> ]	Absolute
Memory	$(r_{!})$	$M[R[r_{!}]]$	Indirect
Memory	Imm(r <sub>"</sub> )	$M[Imm + R[r_{"}]]$	Base + displacement
Memory	( <i>r</i> ", <i>r</i> #)	$M[R[r_{"}] + R[r_{\#}]]$	Indexed
Memory	$Imm(r_{"}, r_{\#})$	$M[Imm + R[r_{"}] + R[r_{\#}]]$	Indexed
Memory	(, r#, s)	$M[R[r_{\#}] . s]$	Scaled indexed
Memory	Imm(, r#, s)	$M[Imm + R[r_{\#}] . s]$	Scaled indexed
Memory	( <i>r</i> <sub>"</sub> , <i>r</i> <sub>#</sub> , <i>s</i> )	$M[R[r_{"}] + R[r_{\#}] \cdot s]$	Scaled indexed
Memory	$Imm(r_{"}, r_{\#}, s)$	$M[Imm + R[r_{"}] + R[r_{\#}] \cdot s]$	Scaled indexed

**Figure 3.3 from the book: "Operand forms.** Operands can denote immediate (constant) values, register values, or values from memory. The scaling factor *s* must be either. 1, 2, 4, or 8."

# **Lecture Plan**

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# **Data Sizes**

Data sizes in assembly have slightly different terminology to get used to:

- A byte is 1 byte.
- A word is 2 bytes.
- A **double word** is 4 bytes.
- A quad word is 8 bytes.

Assembly instructions can have suffixes to refer to these sizes:

- b means byte
- w means word
- 1 means double word
- q means quad word

# **Register Sizes**

Bit:	63	31	15	7	0
	%rax	%eax	%ax	%al	
	%rbx	%ebx	%bx	%bl	
	%rcx	%ecx	%cx	%cl	
	%rdx	%edx	%dx	%dl	
	%rsi	%esi	%si	%sil	
	%rdi	%edi	%di	%dil	

# **Register Sizes**

Bit:	63	31	15	7	0
	%rbp	%ebp	%bp	%bpl	
	%rsp	%esp	%sp	%spl	
	%r8	%r8d	%r8w	%r8b	
	%r9	%r9d	%r9w	%r9b	
	%r10	%r10d	%r10w	%r10b	
	%r11	%r11d	%r11w	%r11b	

# **Register Sizes**

Bit:	63	31	15	7 0
	%r12	%r12d	%r12w	%r12b
	%r13	%r13d	%r13w	%r13b
	%r14	%r14d	%r14w	%r14b
	%r15	%r15d	%r15w	%r15b
# **Register Responsibilities**

Some registers take on special responsibilities during program execution.

- %rax stores the return value
- %rdi stores the first parameter to a function
- %rsi stores the second parameter to a function
- %rdx stores the third parameter to a function
- %rip stores the address of the next instruction to execute
- %rsp stores the address of the current top of the stack

**Reference Sheet**: cs107.stanford.edu/resources/x86-64-reference.pdf See more guides on Resources page of course website!

### mov Variants

- mov can take an optional suffix (b,w,l,q) that specifies the size of data to move: movb, movw, movl, movq
- mov only updates the specific register bytes or memory locations indicated.
  - Exception: movl writing to a register will also set high order 4 bytes to 0.

#### **Practice: mov And Data Sizes**

For each of the following mov instructions, determine the appropriate suffix based on the operands (e.g. **movb**, **movw**, **movl** or **movq**).

- 1. mov\_\_\_ %eax, (%rsp)
- 2. mov\_\_\_ (%rax), %dx
- 3. mov\_\_\_\_\$0xff, %bl
- 4. mov\_\_\_ (%rsp,%rdx,4),%dl
- 5. mov\_\_\_ (%rdx), %rax
- 6. mov\_\_\_ %dx, (%rax)

#### **Practice: mov And Data Sizes**

For each of the following mov instructions, determine the appropriate suffix based on the operands (e.g. **movb**, **movw**, **movl** or **movq**).

- 1. movl %eax, (%rsp)
- 2. movw (%rax), %dx
- 3. movb \$0xff, %b1
- 4. movb (%rsp,%rdx,4),%dl
- 5. movq (%rdx), %rax
- 6. movw %dx, (%rax)

#### mov

- The **movabsq** instruction is used to write a 64-bit Immediate (constant) value.
- The regular **movq** instruction can only take 32-bit immediates.
- 64-bit immediate as source, only register as destination.

#### movabsq \$0x0011223344556677, %rax

### movz and movs

- There are two mov instructions that can be used to copy a smaller source to a larger destination: **movz** and **movs**.
- movz fills the remaining bytes with zeros
- movs fills the remaining bytes by sign-extending the most significant bit in the source.
- The source must be from memory or a register, and the destination is a register.

#### movz and movs

#### MOVZ S, R $R \leftarrow ZeroExtend(S)$

Instruction	Description	
movzbw	Move zero-extended byte to word	
movzbl	Move zero-extended byte to double word	
movzwl	Move zero-extended word to double word	
movzbq	Move zero-extended byte to quad word	
movzwq	Move zero-extended word to quad word	

#### movz and movs

#### MOVS S,R $R \leftarrow SignExtend(S)$

Instruction	Description
movsbw	Move sign-extended byte to word
movsbl	Move sign-extended byte to double word
movswl	Move sign-extended word to double word
movsbq	Move sign-extended byte to quad word
movswq	Move sign-extended word to quad word
movslq	Move sign-extended double word to quad word
cltq	Sign-extend %eax to %rax %rax <- SignExtend(%eax)

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#### lea

#### The **lea** instruction <u>copies</u> an "effective address" from one place to another. **lea src,dst**

Unlike **mov**, which copies data <u>at</u> the address src to the destination, **lea** copies the value of src *itself* to the destination.

The syntax for the destinations is the same as **mov**. The difference is how it handles the src.

Operands	mov Interpretation	lea Interpretation
6(%rax), %rdx	Go to the address (6 + what's in %rax), and copy data there into %rdx	Copy 6 + what's in %rax into %rdx.

Operands	mov Interpretation	lea Interpretation
6(%rax), %rdx	Go to the address (6 + what's in %rax), and copy data there into %rdx	Copy 6 + what's in %rax into %rdx.
(%rax, %rcx), %rdx	Go to the address (what's in %rax + what's in %rcx) and copy data there into %rdx	Copy (what's in %rax + what's in %rcx) into %rdx.

Operands	mov Interpretation	lea Interpretation
6(%rax), %rdx	Go to the address (6 + what's in %rax), and copy data there into %rdx	Copy 6 + what's in %rax into %rdx.
(%rax, %rcx), %rdx	Go to the address (what's in %rax + what's in %rcx) and copy data there into %rdx	Copy (what's in %rax + what's in %rcx) into %rdx.
(%rax, %rcx, 4), %rdx	Go to the address (%rax + 4 * %rcx) and copy data there into %rdx.	Copy (%rax + 4 * %rcx) into %rdx.

Operands	mov Interpretation	lea Interpretation
6(%rax), %rdx	Go to the address (6 + what's in %rax), and copy data there into %rdx	Copy 6 + what's in %rax into %rdx.
(%rax, %rcx), %rdx	Go to the address (what's in %rax + what's in %rcx) and copy data there into %rdx	Copy (what's in %rax + what's in %rcx) into %rdx.
(%rax, %rcx, 4), %rdx	Go to the address (%rax + 4 * %rcx) and copy data there into %rdx.	Copy (%rax + 4 * %rcx) into %rdx.
7(%rax, %rax, 8), %rdx	Go to the address (7 + %rax + 8 * %rax) and copy data there into %rdx.	Copy (7 + %rax + 8 * %rax) into %rdx.

Unlike **mov**, which copies data <u>at</u> the address src to the destination, **lea** copies the value of src *itself* to the destination.

#### **Lecture Plan**

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## **Unary Instructions**

#### The following instructions operate on a single operand (register or memory):

Instruction	Effect	Description
inc D	D ← D + 1	Increment
dec D	D ← D - 1	Decrement
neg D	D ← -D	Negate
not D	D ← ~D	Complement

#### **Examples:**

incq 16(%rax)
dec %rdx
not %rcx

### **Binary Instructions**

The following instructions operate on two operands (both can be register or memory, source can also be immediate). Both cannot be memory locations. Read it as, e.g. "Subtract S from D":

Instruction	Effect	Description
add S, D	D ← D + S	Add
sub S, D	D ← D - S	Subtract
imul S, D	D ← D * S	Multiply
xor S, D	D ← D ^ S	Exclusive-or
or S, D	D ← D   S	Or
and S, D	D ← D & S	And

#### **Examples:**

```
addq %rcx,(%rax)
xorq $16,(%rax, %rdx, 8)
subq %rdx,8(%rax)
```

# **Large Multiplication**

- Multiplying 64-bit numbers can produce a 128-bit result. How does x86-64 support this with only 64-bit registers?
- If you specify two operands to **imul**, it multiplies them together and truncates until it fits in a 64-bit register.

imul S, D  $\leftarrow$  D  $\leftarrow$  S

 If you specify one operand, it multiplies that by %rax, and splits the product across 2 registers. It puts the high-order 64 bits in %rdx and the low-order 64 bits in %rax.

Instruction	Effect	Description
imulq S	R[%rdx]:R[%rax] ← S x R[%rax]	Signed full multiply
mulq S	R[%rdx]:R[%rax] ← S x R[%rax]	Unsigned full multiply

# **Division and Remainder**

Instruction	Effect	Description
idivq S	R[%rdx] ← R[%rdx]:R[%rax] mod S; R[%rax] ← R[%rdx]:R[%rax] ÷ S	Signed divide
divq S	R[%rdx] ← R[%rdx]:R[%rax] mod S; R[%rax] ← R[%rdx]:R[%rax] ÷ S	Unsigned divide

- <u>Terminology</u>: dividend / divisor = quotient + remainder
- x86-64 supports dividing up to a 128-bit value by a 64-bit value.
- The high-order 64 bits of the dividend are in **%rdx**, and the low-order 64 bits are in **%rax**. The divisor is the operand to the instruction.
- The quotient is stored in %rax, and the remainder in %rdx.

# **Division and Remainder**

Instruction	Effect	Description
idivq S	R[%rdx] ← R[%rdx]:R[%rax] mod S; R[%rax] ← R[%rdx]:R[%rax] 🕇 S	Signed divide
divq S	R[%rdx] ← R[%rdx]:R[%rax] mod S; R[%rax] ← R[%rdx]:R[%rax] 🕇 S	Unsigned divide
cqto	R[%rdx]:R[%rax] ← SignExtend(R[%rax])	Convert to oct word

- <u>Terminology</u>: dividend / divisor = quotient + remainder
- The high-order 64 bits of the dividend are in **%rdx**, and the low-order 64 bits are in **%rax**. The divisor is the operand to the instruction.
- Most division uses only 64-bit dividends. The cqto instruction sign-extends the 64-bit value in %rax into %rdx to fill both registers with the dividend, as the division instruction expects.

### **Shift Instructions**

The following instructions have two operands: the shift amount **k** and the destination to shift, **D**. **k** can be either an immediate value, or the byte register **%cl** (and only that register!)

Instruction	Effect	Description
sal k, D	D ← D << k	Left shift
shl k, D	D ← D << k	Left shift (same as sal)
sar k, D	$D \leftarrow D >>_A k$	Arithmetic right shift
shr k, D	$D \leftarrow D \gg_L k$	Logical right shift

#### **Examples:**

shll \$3,(%rax)
shrl %cl,(%rax,%rdx,8)
sarl \$4,8(%rax)

# **Shift Amount**

Instruction	Effect	Description
sal k, D	D ← D << k	Left shift
shl k, D	D ← D << k	Left shift (same as sal)
sar k, D	$D \leftarrow D \gg_A k$	Arithmetic right shift
shr k, D	$D \leftarrow D \gg_L k$	Logical right shift

- When using %cl, the width of what you are shifting determines what portion of %cl is used.
- For w bits of data, it looks at the low-order log2(w) bits of %cl to know how much to shift.
  - If %cl = 0xff, then: shlb shifts by 7 because it considers only the low-order log2(8) = 3 bits, which represent 7. shlw shifts by 15 because it considers only the low-order log2(16) = 4 bits, which represent 15.

#### **Lecture Plan**

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# **Assembly Exploration**

- Let's pull these commands together and see how some C code might be translated to assembly.
- Compiler Explorer is a handy website that lets you quickly write C code and see its assembly translation. Let's check it out!
- <u>https://godbolt.org/z/WPzz6G4a9</u>

#### Code Reference: add\_to\_first

```
// Returns the sum of x and the first element in
arr
int add to first(int x, int arr[]) {
    int sum = x;
    sum += arr[0];
    return sum;
add to first:
 movl %edi, %eax
 addl (%rsi), %eax
  ret
```

#### Code Reference: full\_divide

```
// Returns x/y, stores remainder in location stored in
remainder ptr
long full_divide(long x, long y, long *remainder_ptr) {
    long quotient = x / y;
    long remainder = x % y;
    *remainder ptr = remainder;
    return quotient;
full divide:
  movq %rdi, %rax
 movq %rdx, %rcx
  cqto
  idivq %rsi
  movq %rdx, (%rcx)
  ret
```

```
000000000040116e <sum_example1>:
40116e:8d 04 37 lea (%rdi,%rsi,1),%eax
401171:c3 retq
```

Which of the following is most likely to have generated the above assembly?

```
// A)
void sum_example1() {
    int x;
    int y;
    int sum = x + y;
}
// C)
void sum_example1(int x, int y) {
    int sum = x + y;
}
```

```
// B)
int sum_example1(int x, int y) {
    return x + y;
}
```

```
000000000040116e <sum_example1>:
40116e:8d 04 37 lea (%rdi,%rsi,1),%eax
401171:c3 retq
```

Which of the following is most likely to have generated the above assembly?

```
// A)
void sum_example1() {
    int x;
    int y;
    int sum = x + y;
}
// C)
void sum_example1(int x, int y) {
    int sum = x + y;
}
```



#### 0000000000401172 <sum\_example2>: 401172: 8b 47 0c mov 0xc(%rdi),%eax 401175: 03 07 add (%rdi),%eax 401177: 2b 47 18 sub 0x18(%rdi),%eax 40117a: c3 retq

```
int sum_example2(int arr[]) {
    int sum = 0;
    sum += arr[0];
    sum += arr[3];
    sum -= arr[6];
    return sum;
```

What location or value in the assembly above represents the C code's **sum** variable?

#### 0000000000401172 <sum\_example2>: 401172: 8b 47 0c mov 0xc(%rdi),%eax 401175: 03 07 add (%rdi),%eax 401177: 2b 47 18 sub 0x18(%rdi),%eax 40117a: c3 retq

```
int sum_example2(int arr[]) {
    int sum = 0;
    sum += arr[0];
    sum += arr[3];
    sum -= arr[6];
    return sum;
```

What location or value in the assembly above represents the C code's **sum** variable?

%eax

#### 0000000000401172 <sum\_example2>: 401172: 8b 47 0c mov 0xc(%rdi),%eax 401175: 03 07 add (%rdi),%eax 401177: 2b 47 18 sub 0x18(%rdi),%eax 40117a: c3 retq

```
int sum_example2(int arr[]) {
    int sum = 0;
    sum += arr[0];
    sum += arr[3];
    sum -= arr[6];
    return sum;
```

What location or value in the assembly code above represents the C code's **6** (as in **arr[6]**)?

#### 0000000000401172 <sum\_example2>: 401172: 8b 47 0c mov 0xc(%rdi),%eax 401175: 03 07 add (%rdi),%eax 401177: 2b 47 18 sub 0x18(%rdi),%eax 40117a: c3 retq

```
int sum_example2(int arr[]) {
    int sum = 0;
    sum += arr[0];
    sum += arr[3];
    sum -= arr[6];
    return sum;
```

What location or value in the assembly code above represents the C code's **6** (as in **arr[6]**)?

#### **0x18**

## **Our First Assembly**

```
int sum_array(int arr[], int nelems) {
    int sum = 0;
    for (int i = 0; i < nelems; i++) {
        sum += arr[i];
    }
    return sum;
}</pre>
```

#### 000000000401136 <sum\_array>:

b8 00 00 00 00
ba 00 00 00 00
39 fØ
7d 0b
48 63 c8
03 14 8f
83 c0 01
eb f1
89 d0
c3

We're 1/2 of the way to understanding assembly! What looks understandable right now?

mov	\$0x0,%eax
mov	\$0x0,%edx
cmp	%esi,%eax
jge	40114f <sum_array+0x19></sum_array+0x19>
movslq	%eax,%rcx
add	(%rdi,%rcx,4),%edx
add	\$0x1,%eax
jmp	401140 <sum_array+0xa></sum_array+0xa>
mov	%edx,%eax
retq	



### **A Note About Operand Forms**

- Many instructions share the same address operand forms that **mov** uses.
  - Eg. 7(%rax, %rcx, 2).
- These forms work the same way for other instructions, e.g. sub:
  - sub 8(%rax,%rdx),%rcx -> Go to 8 + %rax + %rdx, subtract what's there from %rcx
- The exception is lea:
  - It interprets this form as just the calculation, not the dereferencing
  - lea 8(%rax,%rdx),%rcx -> Calculate 8 + %rax + %rdx, put it in %rcx

# **Extra Practice**

https://godbolt.org/z/hGKPWszq4

# Learning Goals

- Learn about how assembly stores comparison and operation results in condition codes
- Understand how assembly implements loops and control flow
## **Executing Instructions**

# What does it mean for a program to execute?

Executing Instructions	4004fd	fa
	4004fc	eb
Sofar	4004fb	01
50 Idl.	4004fa	fc
<ul> <li>Program values can be stored in memory or registers.</li> </ul>	4004f9	45
<ul> <li>Assembly instructions read/write values back and forth</li> </ul>	4004f8	83
hetween registers (on the CPLI) and memory	4004f7	00
between registers (on the er of and memory.	4004f6	00
<ul> <li>Assembly instructions are also stored in memory.</li> </ul>	4004f5	00
	4004f4	00
Today	4004f3	fc
Touay.	4004f2	45
<ul> <li>Who controls the instructions?</li> </ul>	4004f1	с7
How do we know what to do now or next?	4004f0	e5
	4004ef	89
AIISWEI.	4004ee	48
<ul> <li>The program counter (PC), %rip.</li> </ul>	4004ed	55

# **Register Responsibilities**

#### Some registers take on special responsibilities during program execution.

- %rax stores the return value
- %rdi stores the first parameter to a function
- %rsi stores the second parameter to a function
- %rdx stores the third parameter to a function
- %rip stores the address of the next instruction to execute
- %rsp stores the address of the current top of the stack

#### See the x86-64 Guide and Reference Sheet on the Resources webpage for more!

### **Instructions Are Just Bytes!**





<b>%</b>		fa
	4004fc	eb
	4004fb	01
0000000004004ed <loop>:</loop>	4004fa	fc
4004ed: 55 push %rbp	4004f9	45
400466: 48 89 65 mov % rsp, % rop 4004f1: c7 45 fc 00 00 00 00 movl $$0x0, -0x4(% rbp)$	4004f8	83
4004f8:       83       45       fc       01       addl       \$0x1, -0x4(%rbp)         4004fc:       ab       fc       imp       4004f8       (loop+0xb)	4004f7	00
4004TC. ED TA JIIIP 4004T8 (100P+0XD>	4004f6	00
	4004f5	00

4004f4

4004f3

4004f2

4004f1

4004f0

4004ef

4004ee

4004ed

**00** 

fc

45

**c7** 

**e5** 

**89** 

**48** 

Main Memory
Stack
Неар
Data
Text (code)

	0/_	rin	4004fd	fa
			4004fc	eb
			4004fb	01
00000000004004ed <loop>:</loop>			4004fa	fc
➡ 4004ed: 55	push	%rbp	4004f9	45
4004ee: 48 89 e5	mov	%rsp,%rbp	4004f8	83
4004f1: c7 45 fc 00 00 00 00	movl	\$0x0,-0x4(%rbp)	4004f7	00
4004f8: 83 45 fc 01	addl	\$0x1,-0x4(%rbp)	4004f6	00
4004fc: eb fa		4004f8 <loop+0xb></loop+0xb>	4004f5	00
			4004f4	00
			4004f3	fc
			4004f2	45
The <b>program counter</b> (PC),			4004f1	c7
known as %rip in x86-64, stores			4004f0	e5
the address in memory of the	[		4004ef	89
<i>next instruction</i> to be executed.	0x40	04ed	4004ee	48
	%r	rip	4004ed	55

		0/0	rin	4004fd	fa
		/0		4004fc	eb
				4004fb	01
	00000000004004ed <loop>:</loop>			4004fa	fc
	4004ed: 55	push	%rbp	4004f9	45
$\Rightarrow$	4004ee: 48 89 e5	mov	%rsp,%rbp	4004f8	83
	4004f1: c7 45 fc 00 00 00 00	movl	\$0x0,-0x4(%rbp)	4004f7	00
	4004f8: 83 45 fc 01	addl	\$0x1,-0x4(%rbp)	4004f6	00
4004fc: eb fa	jmp 4004f8 <loop+0xb></loop+0xb>	4004f5	00		
				4004f4	00
		4004f3	fc		
		4004f2	45		
Ţ	he <b>program counter</b> (PC),			4004f1	c7
k	nown as %rip in x86-64, stores			4004f0	e5
the address in memory of the			4004ef	89	
<i>next instruction</i> to be executed.		0x4004ee		<b>4004ee</b>	48
				4004ed	55
		%r	יוף	L	· 1

0/srin		4004fd	fa	
	/0		4004fc	eb
			4004fb	01
00000000004004ed <loop>:</loop>			4004fa	fc
4004ed: 55	push	%rbp	4004f9	45
4004ee: 48 89 e5	mov	%rsp,%rbp	4004f8	83
➡ 4004f1: c7 45 fc 00 00 00 00	movl	\$0x0,-0x4(%rbp)	4004f7	00
4004f8: 83 45 fc 01	addl \$	\$0x1,-0x4(%rbp)	4004f6	00
4004fc: eb fa	jmp	4004f8 <loop+0xb></loop+0xb>	4004f5	00
			4004f4	00
			4004f3	fc
			4004f2	45
The <b>program counter</b> (PC),			4004f1	c7
known as %rip in x86-64, stores			4004f0	e5
the address in memory of the			4004ef	89
<i>next instruction</i> to be executed.	0x40	04f1	4004ee	48
		•	4004ed	55
	%r	קני	L	

	0/srin	4004fd	fa
		4004fc	eb
		4004fb	01
00000000004004ed <loop>:</loop>		4004fa	fc
4004ed: 55	push %rbp	4004f9	45
4004ee: 48 89 e5	mov %rsp,%rbp	4004f8	83
4004f1: c7 45 fc 00 00 00 00	movl \$0x0,-0x4(%rbp)	4004f7	00
4004f8: 83 45 fc 01	addl \$0x1,-0x4(%rbp)	4004f6	00
4004fc: eb fa	jmp 4004f8 <loop+0xb></loop+0xb>	4004f5	00
		4004f4	00
		4004f3	fc
		4004f2	45
The program counter (PC),		4004f1	c7
known as %rip in x86-64, stores		4004f0	e5
the address in memory of the		4004ef	89
<i>next instruction</i> to be executed.	0x4004f8 🖊	4004ee	48
	%rip	4004ed	55

	0/_	rin	4004fd	fa
	/0		4004fc	eb
			4004fb	01
00000000004004ed <loop>:</loop>			4004fa	fc
4004ed: 55	push	%rbp	4004f9	45
4004ee: 48 89 e5	mov	%rsp,%rbp	4004f8	83
4004f1: c7 45 fc 00 00 00 00	movl	\$0x0,-0x4(%rbp)	4004f7	00
4004f8: 83 45 fc 01	addl	\$0x1,-0x4(%rbp)	4004f6	00
➡ 4004fc: eb fa	jmp	4004f8 <loop+0xb></loop+0xb>	4004f5	00
			4004f4	00
			4004f3	fc
			4004f2	45
The program counter (PC),			4004f1	с7
known as %rip in x86-64, stores			4004f0	e5
the address in memory of the			4004ef	89
<i>next instruction</i> to be executed.	0x46	004fc 🚪	4004ee	48
		] •	4004ed	55

%rip

	0/0	rin	4004fd	fa
			4004fc	eb
			4004fb	01
00000000004004ed <loop>:</loop>			4004fa	fc
4004ed: 55	push	%rbp	4004f9	45
4004ee: 48 89 e5	mov	%rsp,%rbp	4004f8	83
4004f1: c7 45 fc 00 00 00 00	movl	\$0x0,-0x4(%rbp)	4004f7	00
4004f8: 83 45 fc 01	addl	\$0x1,-0x4(%rbp)	4004f6	00
➡ 4004fc: eb fa	jmp	4004f8 <loop+0xb></loop+0xb>	4004f5	00
			4004f4	00
			4004f3	fc
Special hardware sets the program	i count	er	4004f2	45
to the next instruction:			4004f1	с7
%rip += size of bytes of current inst	tructio	n 🖊	4004f0	e5
			4004ef	89
	0x40	04fc 🖡	4004ee	48

%rip

4004ed