#### **CS107, Lecture 14** Alignment, Optimization, & Basic Architecture

This document is copyright (C) Stanford Computer Science, Adam Keppler and Olayinka Adekola, licensed under Creative Commons Attribution 2.5 License. All rights reserved. Based on slides created by Nick Troccoli, Chris Gregg, and Raymond Klefstad

#### Attendance

## https://forms.gle/mUWfemVpi1R81VyW6

## **Registers Vs Addresses**

- So far, we've often seen local variables stored directly in registers, rather than on the stack.
- There are **three** common reasons that local data must be in memory:
  - We've run out of registers
  - The '&' operator is used on it, so we must generate an address for it
  - They are arrays or structs (need to use address arithmetic)

#### Data Alignment

- Computer systems often put restrictions on the allowable addresses for primitive data types, requiring that the address for some objects must be a multiple of some value *K* (normally 2, 4, or 8).
- These *alignment restrictions* simplify the design of the hardware.
- For example, suppose that a processor always fetches 8 bytes from the memory system, and an address must be a multiple of 8. If we can guarantee that any double will be aligned to have its address as a multiple of 8, then we can read or write the values with a single memory access.
- For x86-64, Intel recommends the following alignments for best performance:

Κ	Types
1	char
2	short
4	int, float

8 long, double, char \*

#### Data Alignment

- The compiler enforces alignment by making sure that every data type is organized in such a way that every field within the struct satisfies the alignment restrictions.
- For example, let's look at the following struct:

```
struct S1 {
    int i;
    char c;
    int j;
};
```

- If the compiler used a minimal allocation:
- This would make it impossible to align fields i (offset 0) and j (offset 5). Instead, the compiler inserts a 3-byte gap between fields c and j:

Offset

Contents



i

С

So, don't be surprised if your structs have a sizeof () that is larger than you expect!

9

i

## **GCC Optimizations**

# Optimization

Most of what you need to do with optimization can be summarized by:

- 1) If doing something seldom and only on small inputs, do whatever is simplest to code, understand, and debug
- 2) If doing things a lot, or on big inputs, make the primary algorithm's Big-O cost reasonable
- 3) Let gcc do its magic from there
- 4) Optimize explicitly as a last resort

# **Optimizations you'll see**

#### nop

- **nop/nopl** are "no-op" instructions they do nothing!
- Intent: Make functions align on address boundaries that are nice multiples of 8.
- "Sometimes, doing nothing is how to be most productive" Philosopher Nick

#### mov %ebx,%ebx

• Zeros out the top 32 register bits (because a mov on an e-register zeros out rest of 64 bits).

#### **GCC Common For Loop Output**

Initialization Test Jump past loop if success Body Update Jump to test

#### **Possible Alternative**

Initialization Jump to test Body Update Test Jump to body if success

	for (int i = 0; i < n; i++)	// n = 100
GCC Common For Loop Output		
Initialization		
Test		
Body		
Update		
Jump to test		

	for (int i = 0; i < n; i++)	// n = 100	
GCC Common For Loop Output Initialization Test Jump past loop if success Body Update Jump to test	Initialization Test No jump Body Update Jump to test Test No jump Body Update Jump to test 		11

(

	for (int i = 0; i < n; i++)	// n = 100
GCC Common For Loop Output Initialization Test Jump past loop if success Body Update Jump to test	Initialization Test No jump Body Update Jump to test Test No jump Body Update Jump to test 	

for (int i = 0; i < n; i++)	// n = 100	
Initialization Jump to test Test Jump to body Body Update Test Jump to body Body Update Test Jump to body		<pre>Possible Alternative Initialization Jump to test Body Update Test Jump to body if success</pre>

for (int i = 0; i < n; i++) //	/ n = 100
Initialization Jump to test Test Jump to body Body Update Test Jump to body Body Update Test Jump to body	Possible Alternative Initialization Jump to test Body Update Test Jump to body if success

#### **GCC Common For Loop Output**

Initialization Test Jump past loop if passes Body Update Jump to test

#### **Possible Alternative**

Initialization Jump to test Body Update Test Jump to body if success

Which instructions are better when n = 0? n = 1000?

for (int i = 0; i < n; i++)

15

# **Optimizing Instruction Counts**

- Both versions have the same **static instruction count** (# of written instructions).
- But they have different dynamic instruction counts (# of executed instructions when program is run).
  - If n = 0, left (GCC common output) is best b/c fewer instructions
  - If n is large, right (alternative) is best b/c fewer instructions
- The compiler may emit a static instruction count that is several times longer than an alternative, but it may be more efficient if loop executes many times.
- Does the compiler know that a loop will execute many times? (in general, no)
- So what if our code had loops that always execute a small number of times? How do we know when gcc makes a bad decision?
- (take EE108, EE180, CS316 for more!)

## **Optimizations**

- **Conditional Moves** can sometimes eliminate "branches" (jumps), which are particularly inefficient on modern computer hardware.
- Processors try to *predict* the future execution of instructions for maximum performance. This is difficult to do with jumps.

## **GCC Optimization**

- Today, we'll be comparing two levels of optimization in the gcc compiler:
  - gcc -00 // mostly just literal translation of C
  - gcc -O2 // enable nearly all reasonable optimizations
  - (we also use –Og, like –O0 but more debugging friendly)
- There are other custom and more aggressive levels of optimization, e.g.:
  - -O3 //more aggressive than O2, trade size for speed
  - -Os //optimize for size
  - -Ofast //disregard standards compliance (!!)
- Exhaustive list of gcc optimization-related flags:
  - <u>https://gcc.gnu.org/onlinedocs/gcc/Optimize-Options.html</u>

## **Compiler optimizations**

#### How many GCC optimization levels are there?

Asked 11 years, 3 months ago Active 5 months ago Viewed 62k times

How many <u>GCC</u> optimization levels are there?

- 109 I tried gcc -O1, gcc -O2, gcc -O3, and gcc -O4
  - If I use a really large number, it won't work.



5

However, I have tried

gcc -0100

and it compiled.

How many optimization levels are there?

Gcc supports numbers up to 3. Anything above is interpreted as 3

https://stackoverflow.co m/questions/1778538/ho w-many-gcc-optimizationlevels-are-there

# **GCC Optimizations**

- Constant Folding
- Common Sub-expression Elimination
- Dead Code
- Strength Reduction
- Code Motion
- Loop Unrolling

**Constant Folding** pre-calculates constants at compile-time where possible.

int seconds = 60 \* 60 \* 24 \* n\_days;

**Constant Folding** pre-calculates constants at compile-time where possible.

int seconds = 60 \* 60 \* 24 \* n\_days;

int seconds = 86400 \* n\_days;

```
int fold(int param) {
    char arr[5];
    int a = 0x107;
    int b = a * sizeof(arr);
    int c = 1;
    return a * param + (a + 0x15 / c + strlen("Hello") * b - 0x37) / 4;
}
```

```
int fold(int param) {
    char arr[5];
    int a = 0 \times 107;
    int b = a * sizeof(arr);
    int c = 1;
    return a * param + (a + 0x15 / c + strlen("Hello") * b - 0x37) / 4;
}
int fold(int param) {
    char arr[5];
    int a = 0x107;
    int b = a * 5;
    int c = 1;
    return a * param + (a + 0x15 / c + <mark>5</mark> * b - 0x37) / 4;
}
```

```
int fold(int param) {
    int a = 0x107;
    int b = a * 5;
    int c = 1;
    return a * param + (a + 0x15 / c + 5 * b - 0x37) / 4;
}
int fold(int param) {
    int b = 0x107 * 5;
    int c = 1;
    return 0x107*param+(0x107+0x15/c+5*b-0x37) / 4;
}
```

```
int fold(int param) {
    int b = 0x107 * 5;
    int c = 1;
    return 0x107*param+(0x107+0x15/c+5*b-0x37) / 4;
}
int fold(int param) {
    return 0x107*param+(0x11c/1+5* 0x107 * 5 -0x37) / 4;
}
```

```
int fold(int param) {
    int b = 0x107 * 5;
    int c = 1;
    return 0x107*param+(0x107+0x15/c+5*b-0x37) / 4;
}
int fold(int param) {
    return 0x107*param+(0x107 + 0x15/1+5* 0x107 * 5 -0x37) / 4;
}
int fold(int param) {
    return 0x107 * param + 1701;
}
```

### **Constant Folding: Before (-00)**

000000000000	011b9 <fold>:</fold>		
11b9:	55	push	%rbp
11ba:	48 89 e5	mov	%rsp,%rbp
11bd:	41 54	push	%r12
11bf:	53	bush	%rbx
11c0:	48 83 ec 30	sub	\$0x30.%rsp
11c4:	89 7d cc	mov	%edi0x34(%rbp)
11c7:	c7 45 ec 07 01 00	00 movl	\$0x1070x14(%rbp)
11ce:	8b 45 ec	mov	-0x14(%rbn).%eax
11d1:	48 98	clta	•••=•(•••• <b>;</b> ),•••••
11d3:	89 62	mov	%eax.%edx
11d5 ·	89 dA	mov	%edx.%eax
11d7.	c1 e0 02	sh1	\$0x2,%eax
11da ·	01 d0	add	%edx.%eax
11dc ·	89 45 e8	mov	%eax, -0x18(%rbn)
11df	48 8h 05 2a 0e 00	00 mov	$0xe^{2}a(%rin)$ , %rax
11e6.	66 48 0f 6e c0	mova	%rax $%$ xmm0
11eb.	$e^{8}$ h0 fe ff ff	callo	10a0 (sort@n]ts
11f0.	$f_{2} = 0f_{2} = c_{0}$	cvttsd	2si %xmm0 %eax
1141.	89 45 64	mov	$9 = 231$ $\sqrt{10}$
114.	85 45 ec	mov	-0x14(9  rbn) + 900000000000000000000000000000000000
11f2.	00 + 3 = 0	imul	-0x34(%  rbp),%eax
11fa.		mov	% and % 12d
1201.	h8 15 00 00 00	mov	\$0x15 %02x
1201.	00 00 00 00 00	c1+d	\$UXI),%eax
1200.	f7 7d 64	idivl	-0x1c(%nbn)
1207.	89 c2	mov	Yeax Yedy
1200.	85 (2 86 / 5 oc	mov	-0x14(9rhn) %eav
1200.	01 d0		Yody Yoay
1201.	10 62 40	auu	%eux,%edx
1211.	40 05 00 40 2d 2d ad 0d 00	00 102	Avdod(%pip) %pdi
1214. 121h.			1040 (stplop@plts
1210.		Cally	$A_{1040}$ (Strienwpitz)
1220.		movela	Yody Shdy
1225.	40 05 02	inul	%eux,%rux
1220.	40 01 01 02		% NUX, % NOX
1224.	40 01 00	auu	
1220.	40 05 00 57	Sub	φαχ5/,//ax
1221.	40 (1 60 02	SIII	۵۲'dX ر ۵۲'dX % ما ۲ ما ۳
1235:	44 01 60	auu	ALTIC / ACC
1238:	40 03 (4 30 Fb	auu	γοκου, «rsp
1230:		pop	/01'UX % -1 0
123U:	41 DC	pop	%1'12 %aba
1237:	5u	рор	%noh
1240:	63	reta	

# 2010 <\_I0\_stdin\_used+0x10>

# 2008 <\_I0\_stdin\_used+0x8>

## **Constant Folding: After (-02)**

0000000000011b0 <fold>:

11b0:	69 c	7 07 01	00 00
11b6:	05 a	5 06 00	00
11bb:	c3		

\$0x107,%edi,%eax \$0x6a5,%eax

imul add

retq

What is the consequence of this for you as a programmer? What should you do differently or the same knowing that compilers can do this for you?

## **GCC Optimizations**

- Constant Folding
- <u>Common Sub-expression Elimination</u>
- Dead Code
- Strength Reduction
- Code Motion
- Loop Unrolling

### **Common Sub-Expression Elimination**

**Common Sub-Expression Elimination** prevents the recalculation of the same thing many times by doing it once and saving the result.

```
int a = (param2 + 0x107);
int b = param1 * (param2 + 0x107) + a;
return a * (param2 + 0x107) + b * (param2 + 0x107);
```

#### **Common Sub-Expression Elimination**

**Common Sub-Expression Elimination** prevents the recalculation of the same thing many times by doing it once and saving the result.

```
int a = (param2 + 0x107);
int b = param1 * (param2 + 0x107) + a;
return a * (param2 + 0x107) + b * (param2 + 0x107);
// = 2 * a * a + param1 * a * a
```

0000000000011b	<pre>&gt; <subexp>: // param1</subexp></pre>	in %edi, param2 in %esi
11b0: lea	0x107(%rsi),%eax	// %eax stores a
11b6: imul	%eax,%edi	// param1 * a
11b9: lea	(%rdi,%rax,2),%esi	// 2 * a + param1 * a
11bc: imul	%esi,%eax	// a * (2 * a + param1 * a)
11bf: reta		

## **Common Sub-Expression Elimination**

Why should we bother saving repeated calculations in variables if the compiler has common subexpression elimination?

- 1) The compiler may not always be able to optimize every instance.
- 2) Helps reduce redundancy!
- 3) Makes code more readable!

# **GCC Optimizations**

- Constant Folding
- Common Sub-expression Elimination
- Dead Code
- Strength Reduction
- Code Motion
- Loop Unrolling

#### **Dead Code**

Dead code elimination removes code that doesn't serve a purpose:

```
if (param1 < param2 && param1 > param2) {
    printf("This test can never be true!\n");
}
// Empty for loop
for (int i = 0; i < 1000; i++);</pre>
// If/else that does the same operation in both cases
if (param1 == param2) {
    param1++;
} else {
    param1++;
}
// If/else that more trickily does the same operation in both cases
if (param1 == 0) {
    return 0;
} else {
    return param1;
}
```

#### **Dead Code: Before (-00)**

000000000000000000000000000000000000000	)11a	9 <	dea	d_c	ode	>:	
1149:55 11aa:48 11ad:48 11b1:89 11b4:89 11b4:89 11b7:8b 11ba:3b	89 83 7d 75 45 45	e5 ec e8 ec e8	20				
11bd: 70 11bf: 8b 11c2: 3b	45 45 11	ec e8					
11c5:7e 11c7:48 11ce:b8	8d 00	3d 00	36 00 ff	0e 00 ff	00	00	
11d5:c7 11df:eb	45 04	fc	00	00	00	00	
11e1:83 11e5:81	45 7d f3	fc fc	01 e7	03	00	00	
11ee: 8b 11f1: 3b	45 45	ec e8					
11f6:83	45	ec	01				
11fc: 83 1200: 83	45 7d	ec ec	01 00				
1204:75 1206:b8	00	00	00	00			
1200: cb 120d: 8b 1210: c9 1211: c3	45	ec					

%rbp push %rsp,%rbp \$0x20,%rsp mov sub \$0x20,%rsp %edi,-0x14(%rbp) %esi,-0x18(%rbp) -0x14(%rbp),%eax -0x18(%rbp),%eax 11d8 <dead code+0x2f> -0x14(%rbp),%eax -0x18(%rbp),%eax 11d8 <dead code+0x2f> 0x036(%rin) %rdi mov mov mov cmp jge mov cmp jle 0xe36(%rip),%rdi \$0x0,%eax 1ea mov \$0x0,%eax 1040 <printf@plt> \$0x0,-0x4(%rbp) 11e5 <dead code+0x3c> \$0x1,-0x4(%rbp) \$0x3e7,-0x4(%rbp) 11e1 <dead code+0x38> -0x14(%rbp),%eax -0x18(%rbp),%eax 11fc <dead code+0x53> \$0x1,-0x14(%rbp) 1200 <dead code+0x57> \$0x1,-0x14(%rbp) callq movl jmp addl cmpl jle mov cmp jne ăddl jmp \$0x1,-0x14(%rbp) \$0x0,-0x14(%rbp) 120d <dead\_code+0x64> \$0x0,%eax ăddl cmpl ine moν 1210 <dead code+0x67> jmp -0x14(%rbp),%eax mov leaveg retq

# 2004 <\_I0\_stdin\_used+0x4>
### **Dead Code: After (-02)**

000000000011b0 <dead\_code>: 11b0: 8d 47 01 11b3: c3

lea 0x1(%rdi),%eax
retq

## **GCC Optimizations**

- Constant Folding
- Common Sub-expression Elimination
- Dead Code
- <u>Strength Reduction</u>
- Code Motion
- Loop Unrolling

### **Strength Reduction**

**Strength reduction** changes divide to multiply, multiply to add/shift, and mod to AND to avoid using instructions that cost many cycles (multiply and divide).

```
int a = param2 * 32;
int b = a * 7;
int c = b / 2;
int d = param2 % 2;
for (int i = 0; i <= param2; i++) {
    c += param1[i] + 0x107 * i;
}
return c + d;
```

## **Shifting into Shifts**

- int a = param2 \* 32;
  Becomes:
- int a = param2 << 5;
- int b = a \* 7;
  Becomes:
- int b = a + (a << 2) + (a << 1); or // (a << 3)-a
- int c = b / 2;
  Becomes
- int c = b >> 1 // Division by odd numbers is more complex

## **GCC Optimizations**

- Constant Folding
- Common Sub-expression Elimination
- Dead Code
- Strength Reduction
- <u>Code Motion</u>
- Loop Unrolling

### **Code Motion**

Code motion moves code outside of a loop if possible.

```
for (int i = 0; i < n; i++) {
    sum += arr[i] + foo * (bar + 3);
}</pre>
```

Common subexpression elimination deals with expressions that appear multiple times in the code. Here, the expression appears once, but is calculated each loop iteration, even though none of its values change during the loop.

### **Code Motion**

Code motion moves code outside of a loop if possible.

```
int temp = foo * (bar + 3);
for (int i = 0; i < n; i++) {
   sum += arr[i] + temp;
}</pre>
```

Moving it out of the loop allows the computation to happen only once.

#### **Practice: GCC Optimization**

```
int char_sum(char *s) {
    int sum = 0;
    for (size_t i = 0; i < strlen(s); i++) {
        sum += s[i];
    }
    return sum;
}</pre>
```

What is the bottleneck? What (if anything) can GCC do?

#### **Practice: GCC Optimization**

```
int char_sum(char *s) {
    int sum = 0;
    for (size_t i = 0; i < strlen(s); i++) {
        sum += s[i];
    }
    return sum;
}</pre>
```

What is the bottleneck? What (if anything) can GCC do?

strlen is called every loop iteration – <u>code motion</u> can pull it out of the loop

## **GCC Optimizations**

- Constant Folding
- Common Sub-expression Elimination
- Dead Code
- Strength Reduction
- Code Motion
- Loop Unrolling

### **Loop Unrolling**

**Loop Unrolling:** Do **n** loop iterations' worth of work per actual loop iteration, so we save ourselves from doing the loop overhead (test and jump) every time, and instead incur overhead only every n-th time.

```
for (int i = 0; i <= n - 4; i += 4) {
    sum += arr[i];
    sum += arr[i + 1];
    sum += arr[i + 2];
    sum += arr[i + 3];
} // after the loop handle any leftovers</pre>
```

## **Into the Architecture!**

	Level 7	Application Layer (Prompt Engineering, UI/UX)
scanf / printf		Intent Interpretation (User -> Code Translation)
	Level 6	High-Level (Problem/Object Oriented) Programming Languages
		Translation(Compiler)
	Level 5	Assembly Language
		Translation(Assembler)
	Level 4	Operating System (aka the Machine Level)
		Partial Interpretation (Syscall Interface & Hardware Abstraction Layer (HAL))
	Level 3	Instruction Set Architecture Level
		Microprogram Interpretation or Direct Execution
	Level 2	Micro-architecture Level
		Logic Synthesis
	Level 1	Digital Logic / Circuit Design Level
		Physical/Layout Design
	Level 0	Layout for Fabrication (Defined by the OASIS Standard)
		Lithography
Program Specific Inte	eractions	Etched Silicon 49

	Level 7	Application Layer (Prompt Engineering, UI/UX)
		Intent Interpretation (User -> Code Translation)
	Level 6	High-Level (Problem/Object Oriented) Programming Languages
GCC		Translation(Compiler)
	Level 5	Assembly Language
		Translation(Assembler)
	Level 4	Operating System (aka the Machine Level)
		Partial Interpretation (Syscall Interface & Hardware Abstraction Layer (HAL))
	Level 3	Instruction Set Architecture Level
		Microprogram Interpretation or Direct Execution
	Level 2	Micro-architecture Level
		Logic Synthesis
	Level 1	Digital Logic / Circuit Design Level
		Physical/Layout Design
	Level 0	Layout for Fabrication (Defined by the OASIS Standard)
		Lithography
Where GCC	Gets Its Name	Etched Silicon 50

	Level 7	Application Layer (Prompt Engineering, UI/UX)
		Intent Interpretation (User -> Code Translation)
	Level 6	High-Level (Problem/Object Oriented) Programming Languages
Start		Translation(Compiler)
	Level 5	Assembly Language
		Translation(Assembler)
	Level 4	Operating System (aka the Machine Level)
Run a.out		Partial Interpretation (Syscall Interface & Hardware Abstraction Layer (HAL))
	Level 3	Instruction Set Architecture Level
		Microprogram Interpretation or Direct Execution
	Level 2	Micro-architecture Level
		Logic Synthesis
	Level 1	Digital Logic / Circuit Design Level
		Physical/Layout Design
	Level 0	Layout for Fabrication (Defined by the OASIS Standard)
		Lithography
How far GCC	can reach	Etched Silicon 51

Level 7	Application Layer (Prompt Engineering, UI/UX)
	Intent Interpretation (User -> Code Translation)
Level 6	High-Level (Problem/Object Oriented) Programming Languages
	Translation(Compiler)
Level 5	Assembly Language
AS/GAS	Translation(Assembler)
Level 4	Operating System (aka the Machine Level)
	Partial Interpretation (Syscall Interface & Hardware Abstraction Layer (HAL))
Level 3	Instruction Set Architecture Level
	Microprogram Interpretation or Direct Execution
Level 2	Micro-architecture Level
	Logic Synthesis
Level 1	Digital Logic / Circuit Design Level
	Physical/Layout Design
Level 0	Layout for Fabrication (Defined by the OASIS Standard)
	Lithography
GNU Assembler (Inside GCC)	Etched Silicon 52

	Level 7	Application Layer (Prompt Engineering, UI/UX)
		Intent Interpretation (User -> Code Translation)
	Level 6	High-Level (Problem/Object Oriented) Programming Languages
		Translation(Compiler)
	Level 5	Assembly Language
		Translation(Assembler)
	Level 4	Operating System (aka the Machine Level)
RUN		Partial Interpretation (Syscall Interface & Hardware Abstraction Layer (HAL))
	Level 3	Instruction Set Architecture Level
		Microprogram Interpretation or Direct Execution
	Level 2	Micro-architecture Level
		Logic Synthesis
	Level 1	Digital Logic / Circuit Design Level
		Physical/Layout Design
	Level 0	Layout for Fabrication (Defined by the OASIS Standard)
		Lithography
OS Manages	s Program -> Hardware	Etched Silicon 53

Level 7	Application Layer (Prompt Engineering, UI/UX)
	Intent Interpretation (User -> Code Translation)
Level 6	High-Level (Problem/Object Oriented) Programming Languages
	Translation(Compiler)
Level 5	Assembly Language
	Translation(Assembler)
Level 4	Operating System (aka the Machine Level)
	Partial Interpretation (Syscall Interface & Hardware Abstraction Layer (HAL))
Level 3	Instruction Set Architecture Level
RUN	Microprogram Interpretation or Direct Execution
Level 2	Micro-architecture Level
	Logic Synthesis
Level 1	Digital Logic / Circuit Design Level
	Physical/Layout Design
Level 0	Layout for Fabrication (Defined by the OASIS Standard)
	Lithography
Processing the Machine Code	Etched Silicon 54

Level 7		Application Layer (Prompt Engineering, UI/UX)
		Intent Interpretation (User -> Code Translation)
	Level 6	High-Level (Problem/Object Oriented) Programming Languages
		Translation(Compiler)
	Level 5	Assembly Language
		Translation(Assembler)
	Level 4	Operating System (aka the Machine Level)
		Partial Interpretation (Syscall Interface & Hardware Abstraction Layer (HAL))
	Level 3	Instruction Set Architecture Level
		Microprogram Interpretation or Direct Execution
	Level 2	Micro-architecture Level
VLSI		Logic Synthesis
	Level 1	Digital Logic / Circuit Design Level
		Physical/Layout Design
	Level 0	Layout for Fabrication (Defined by the OASIS Standard)
		Lithography
Very-Large-Scale Integration		Etched Silicon 55

	Level 7	Application Layer (Prompt Engineering, UI/UX)
		Intent Interpretation (User -> Code Translation)
	Level 6	High-Level (Problem/Object Oriented) Programming Languages
		Translation(Compiler)
	Level 5	Assembly Language
		Translation(Assembler)
	Level 4	Operating System (aka the Machine Level)
		Partial Interpretation (Syscall Interface & Hardware Abstraction Layer (HAL))
	Level 3	Instruction Set Architecture Level
		Microprogram Interpretation or Direct Execution
	Level 2	Micro-architecture Level
RTL ——		Logic Synthesis
	Level 1	Digital Logic / Circuit Design Level
		Physical/Layout Design
	Level 0	Layout for Fabrication (Defined by the OASIS Standard)
		Lithography
RTL (Registe	er-Transfer Level)	Etched Silicon 56

	Level 7	Application Layer (Prompt Engineering, UI/UX)
		Intent Interpretation (User -> Code Translation)
	Level 6	High-Level (Problem/Object Oriented) Programming Languages
		Translation(Compiler)
	Level 5	Assembly Language
		Translation(Assembler)
	Level 4	Operating System (aka the Machine Level)
		Partial Interpretation (Syscall Interface & Hardware Abstraction Layer (HAL))
	Level 3	Instruction Set Architecture Level
		Microprogram Interpretation or Direct Execution
	Level 2	Micro-architecture Level
		Logic Synthesis
	Level 1	Digital Logic / Circuit Design Level
		Physical/Layout Design
Steps	Level 0	Layout for Fabrication (Defined by the OASIS Standard)
		Lithography
Floorplanning		Etched Silicon 57

	Level 7	Application Layer (Prompt Engineering, UI/UX)
		Intent Interpretation (User -> Code Translation)
	Level 6	High-Level (Problem/Object Oriented) Programming Languages
		Translation(Compiler)
	Level 5	Assembly Language
		Translation(Assembler)
	Level 4	Operating System (aka the Machine Level)
		Partial Interpretation (Syscall Interface & Hardware Abstraction Layer (HAL))
	Level 3	Instruction Set Architecture Level
		Microprogram Interpretation or Direct Execution
	Level 2	Micro-architecture Level
		Logic Synthesis
	Level 1	Digital Logic / Circuit Design Level
		Physical/Layout Design
Steps	Level 0	Layout for Fabrication (Defined by the OASIS Standard)
		Lithography
Wire Routing		Etched Silicon 58
– Don't Cross the V	wires	50

	Level 7	Application Layer (Prompt Engineering, UI/UX)
		Intent Interpretation (User -> Code Translation)
	Level 6	High-Level (Problem/Object Oriented) Programming Languages
		Translation(Compiler)
	Level 5	Assembly Language
		Translation(Assembler)
	Level 4	Operating System (aka the Machine Level)
		Partial Interpretation (Syscall Interface & Hardware Abstraction Layer (HAL))
	Level 3	Instruction Set Architecture Level
Many		Microprogram Interpretation or Direct Execution
	Level 2	Micro-architecture Level
		Logic Synthesis
	Level 1	Digital Logic / Circuit Design Level
		Physical/Layout Design
Steps	Level 0	Layout for Fabrication (Defined by the OASIS Standard)
		Lithography
Clock Tree Synth Time it Just Righ	iesis – Got to t	Etched Silicon 59

	Level 7	Application Layer (Prompt Engineering, UI/UX)
	Level 6	High-Level (Problem/Object Oriented) Programming Languages
	Level 5	Assembly Language Translation(Assembler)
	Level 4	Operating System (aka the Machine Level) Partial Interpretation (Syscall Interface & Hardware Abstraction Layer (HAL))
	Level 3	Instruction Set Architecture Level Microprogram Interpretation or Direct Execution
	Level 2	Micro-architecture Level
Many Steps	Level 1	Digital Logic / Circuit Design Level
	Level 0	Layout for Fabrication (Defined by the OASIS Standard)
Heat & Capacitance		Etched Silicon 60

Level 7	Application Layer (Prompt Engineering, UI/UX)
	Intent Interpretation (User -> Code Translation)
Level 6	High-Level (Problem/Object Oriented) Programming Languages
	Translation(Compiler)
Level 5	Assembly Language
	Translation(Assembler)
Level 4	Operating System (aka the Machine Level)
	Partial Interpretation (Syscall Interface & Hardware Abstraction Layer (HAL))
Level 3	Instruction Set Architecture Level
	Microprogram Interpretation or Direct Execution
Level 2	Micro-architecture Level
	Logic Synthesis
Level 1	Digital Logic / Circuit Design Level
	Physical/Layout Design
Level 0	Layout for Fabrication (Defined by the OASIS Standard)
ASML	Lithography
Checkout EUV Lithography	Etched Silicon 61

Level 7	Application Layer (Prompt Engineering, UI/UX)		
	Intent Interpretation (User -> Code Translation)	$( \cdot \cdot )$	
Level 6	High-Level (Problem/Object Oriented) Programming Languages Translation(Compiler)		
Level 5	Assembly Language Translation(Assembler)	Which layer throws a segfault?	
Level 4	Operating System (aka the Machine Level)		
	Partial Interpretation (Syscall Interface & Hardware	Abstraction Layer (HAL))	
Level 3	Instruction Set Architecture Level		
	Microprogram Interpretation or Direct Execution		
Level 2	Micro-architecture Level		
	Logic Synthesis		
Level 1	Digital Logic / Circuit Design Level		
	Physical/Layout Design		
Level 0	Layout for Fabrication (Defined by the OASIS Standard)		
	Lithography		
	Etched Silicon	62	

Level 7 Level 6 Level 5 Level 4 Level 3 Level 2 Level 1 Level 0	Level 7	Application Layer (Prompt Engineering, UI/UX)
		Intent Interpretation (User -> Code Translation)
	Level 6	High-Level (Problem/Object Oriented) Programming Languages
		Translation(Compiler)
	Level 5	Assembly Language
		Translation(Assembler)
	Level 4	Operating System (aka the Machine Level)
		Partial Interpretation (Syscall Interface & Hardware Abstraction Layer (HAL)
	Level 3	Instruction Set Architecture Level
		Microprogram Interpretation or Direct Execution
	Level 2	Micro-architecture Level
		Logic Synthesis
	Level 1	Digital Logic / Circuit Design Level
		Physical/Layout Design
	Level 0	Layout for Fabrication (Defined by the OASIS Standard)
		Lithography
By The OS		Etched Silicon 63

## **More on the Compiler**

• One Unix Command – A lot of steps!

gcc hello.c -o hello



65

- Preprocessing Handle Programmer Conveniences
  - #Macros convert to normal C code
  - Lines split by \ are joined
  - Comments are removed
    - NOTE: Some comments are added, but our comments are removed
  - Bring in functions and variables from the headers
    - This is how the #include is resolved

gcc -E hello.c > pre\_processed\_hello



• Compilation – C to Assembly

gcc -S hello.c

- Will generate intermediate 'human-readable' assembly
- There are different styles/syntax for x86, we use AT&T
  - AT&T is also the gcc default



• Object Generation – C to Object File

gcc -c hello.c

- "Just compile; Don't link"
- This outputs a non-human readable Object File
  - It is defined as a type of incomplete machine code
  - With extra metadata to power linking
- Using objdump –d hello.o , we can see the assembly



- Linking Bringing All the pieces together
  - Object Files & Libraries -> Fully Executable Machine Code

gcc hello.o -o hello

ld -o hello hello.o -lc -dynamic-linker /lib64/ld-linux-x86-64.so.2 /usr/lib/x86\_64-linux-gnu/crt1.o /usr/lib/x86\_64-linux-gnu/crti.o /usr/lib/x86\_64-linux-gnu/crtn.o

- NOTE: We can get our .o in more than one-way gcc -c hello.c
- OR
- as hello.s



## What does the Assembler Do?

## **A Two Step Process**

- Pass 1: Setup Memory Addresses
  - The program reads in the assembly program identifying and tracking:
    - Labels
    - Literals
    - Data Variables
- Pass 2: Generate the Machine Code (Byte/Binary Code)
  - Identify Opcode from the mnemonic assembly
  - Resolve labels/literals/variables using the tables from Step 1
  - Convert Data to Binary
  - Identifies External (Out of Program) References and places markers for the Linker
  - Setup Metadata for linking if this program has loadable parts

Final Output is not runnable, but has all the parts need if linking can complete

## Why do we need a linker?
# **Many Links**

- Every C file corresponds to a .o
- Libraries can also be made into linkable formats
- We don't want to have to write all our code in 1 file and we want to use the STL
- The linker makes this all possible

#### **How Does GCC Work?**

- Multi-Step Process -> Multiple Failure Points
- Compilation can fail for many reasons at different points
- Mainly two areas that fail 'Compilation' or Linking
- If compilation succeeds, Intermediate Assembly will be good!



#### **Peeking at Memory**

- CPU is the most important place
  - Closer to CPU, less travel time
  - But limited space, so bottleneck getting there
- Think of the CPU like downtown, generally expensive and highly desirable real estate
- The BUS (actual technical name) is our transit system around the computer





76

- All of Memory (Temporary Storage on the right) and the registers is rent only, so data is constantly moving around
- Many algorithms developed to decide which data gets to live where and for how long
- Proper access makes a huge difference on performance



#### • Approximate Access Times

Resource	Latency Time
Register	0 Cycles (already here)
Level 1 Cache	~0.5 ns
Level 2 Cache	~7 ns (14x L1)
RAM	~100 ns (20x L2, 200x L1)
SSD	~100-150 us (~14Kx L2, 200Kx L1)
Hard (Spinning) Disk	~10 ms (~2.8Mx L2, 40Mx L1)
Network Packet CA -> Netherlands -> CA	~150 ms (~21Mx L2, 300Mx L1)
Average Human Response Time to Visual Stimulus	~200 ms (~28Mx L2, 400Mx L1)



For more on speed checkout: <u>https://www.cs.princeton.edu/courses/archive/spring20/cos217/lectures/20\_Mem\_Storage\_Hierarchy.pdf</u> <u>https://gist.github.com/jboner/2841832</u>

- Pre-emptive requests and moving of data is critical
- Orders of Magnitude Improvements from high locality
- Every part of the pyramid is working on making this faster
- Better BUS, faster storage(both temporary and permanent), bigger RAM, better algorithms



# What is Locality?

- Temporal Locality
  - Has the data been used recently? Then we expect to be used again soon
- Spatial Locality
  - The data appears close together in the program/memory, so it will likely be needed at the same time.
- Hardware and OS designers consider algorithms to predict and leverage locality to optimize management of memory resources
- Cache in particular is a limited resource and must be used effectively to leverage benefits

#### Who Gets to Manage the Memory?

- Registers Managed by the Compiler/Assembler
- Cache Managed by Hardware Designers
- Memory Mainly the OS, influenced by hardware
- Disk Managed by the user and occasionally OS



#### **Architecture & The ISA**

# **Programming Levels**

	Level 7	Application Layer (Prompt Engineering, UI/UX)
		Intent Interpretation (User -> Code Translation)
	Level 6	High-Level (Problem/Object Oriented) Programming Languages
		Translation(Compiler)
Level 5		Assembly Language
		Translation(Assembler)
	Level 4	Operating System (aka the Machine Level)
		Partial Interpretation (Syscall Interface & Hardware Abstraction Layer (HAL))
	Level 3	Instruction Set Architecture Level
		Microprogram Interpretation or Direct Execution
Processor	Level 2	Micro-architecture Level
		Logic Synthesis
	Level 1	Digital Logic / Circuit Design Level
		Physical/Layout Design
	Level 0	Layout for Fabrication (Defined by the OASIS Standard)
		Lithography
These levels	are integrally linked	Etched Silicon 83

- MIC-1 Architecture (Tanenbaum -Structured Computer Organization 6<sup>th</sup> Edition)
- IJVM ISA Subset of the Java Virtual Machine
- A 'Vanilla' processor design



- Control Store is the most important part!
- Our ISA is defined by that unit
- 9 wires in -> 2\*\*9 possible combinations, 2\*\*9 (512) possible commands
- Each command drives 36 wires to control the chip
- Assembly/Machine Language is defined by the hardware



- ALU Arithmetic & Logic Unit
  - Performs Math & Logic Operations
- MAR H are the registers
- B + Decoder Enables Register to load onto B Bus
- Z and N act similar to our condition codes, but in a much more limited/simple way
- C controls the C Bus, informing the destination register to receive its value



- Notice how the ALU is only able to take in the left operand from the H register
- All two operand ALU operations, would need to first load the left operand to H
- This would be an example of a hardware based constraint



#### **Better Design Better Performance**

- The MIC-2 Fixes this issue by adding another BUS improving the Datapath
- Design directly impacts the ISA that we can make available



# **Some Extra Reading**

#### **Key GDB Tips For Assembly**

• Examine 4 giant words (8 bytes) on the stack:

(gdb) x/4g \$rsp 0x7fffffe870: 0x000000000000000 0x7ffffffe880: 0x000000000000000

0x0000000000400559 0x0000000000400575

 display/undisplay (prints out things every time you step/next) (gdb) display/4w \$rsp
1: x/4xw \$rsp
0x7ffffffe8a8:
0xf7a2d830
0x00007fff
0x0000000
0x0000000

# **Key GDB Tips For Assembly**

- stepi/finish: step into current function call/return to caller: (gdb) finish
- Set register values during the run (gdb) p \$rdi = \$rdi + 1
- (Might be useful to write down the original value of \$rdi somewhere)
- Tui things
  - refresh
  - focus cmd use up/down arrows on gdb command line (vs focus asm, focus regs)
  - layout regs, layout asm

# gdb tips



- (ctrl-x a: exit, layout split ctrl-l: resize) info reg
- View C, assembly, and gdb **Print all registers**

Print register value Print all condition codes currently set

\*0x400546 b

\$eflags

\$eax

\*0x400550 if \$eax > 98 b

ni

p

р

si

Set breakpoint at assembly instruction Set conditional breakpoint

Next assembly instruction

Step into assembly instruction (will step into function calls) 92

# gdb tips



p/x \$rdi	Print register value in hex
p/t \$rsi	Print register value in binary
x \$rdi	Examine the byte stored at this address
x/4bx \$rdi	Examine 4 bytes starting at this address
x/4wx \$rdi	Examine 4 ints starting at this address

#### **References and Advanced**

- References:
  - Stanford guide to x86-64: <u>https://web.stanford.edu/class/cs107/guide/</u> x86-64.html
  - CS107 one-page of x86-64: <u>https://web.stanford.edu/class/cs107/resources/</u> onepage\_x86-64.pdf
  - gdbtui: <u>https://beej.us/guide/bggdb/</u>
  - More gdbtui: <u>https://sourceware.org/gdb/onlinedocs/gdb/TUI.html</u>
  - Compiler explorer: <u>https://gcc.godbolt.org</u>
- Advanced Reading:
  - Stack frame layout on x86-64: <u>https://eli.thegreenplace.net/2011/09/06/stack-frame-layout-on-x86-64</u>
  - x86-64 Intel Software Developer manual: <u>https://software.intel.com/sites/</u> <u>default/files/managed/39/c5/325462-sdm-vol-1-2abcd-3abcd.pdf</u>
  - history of x86 instructions: <u>https://en.wikipedia.org/wiki/X86\_instruction\_listings</u>
  - x86-64 Wikipedia: https://en.wikipedia.org/wiki/X86-64