EE108A Digital Systems I
Course Policy

Room:	School of Education 334 Mon/Wed 11:00-12:15
Instructor:	Professor Philip Levis pal@cs.stanford.edu Gates 358 (650)725-9046 Hours: Mon 1-2PM / Wed 3-4PM / Fri 1:30-3PM (except as noted – see announcements)
TAs:	Lykomidis Mastroleon lmastro@stanford.edu Hours Sun 4:30-6:00, Tues 1:00-2:30 Brandon Nefcy nefcy@stanford.edu Hours Sun 3:00-4:30, Tues 2:30-4:00
Section Leaders:	Arjun Agarwal arjun.agarwal@stanford.edu Hours TBD David Gal dgal1@stanford.edu Hours TBD Jordan Otomo jotomo@stanford.edu Hours TBD All TA and Section Leader office hours are in Packard 127. (Office hours may change – see the announcements on the web page)
Support:	Marianne Siroker siroker@cs.stanford.edu Gates 435 (650)723-0872
On-Line Info:	Available via http://www.stanford.edu/class/ee108a

Goal

The course is an introduction to digital systems design. It gives the student a working knowledge of the design and analysis of combinational logic, finite-state-machines, system partitioning, timing and synchronization. The course presents this material in the context of modern digital design using a highlevel hardware description language, Verilog, and synthesis to an FPGA for implementation.

Assignments

There will be five weekly homework assignments, six weekly lab assignments, and a class project. All assignments will be posted on the course web page. The project will involve designing a significant digital system and implementing it using Verilog mapped to an FPGA. Homework assignments will be handed out most Mondays in class. Completed assignments shall be handed in by the beginning of class on the Wednesday of the following week. Homework and pre-lab assignments can be handed in before their due date to the course administrator. Don't just put them under the instructor's door.

Laboratory Assignments

Lab assignments will be done in groups of 2. Groups will be assigned one three-hour lab session per week to complete the laboratory. Laboratory assignments will be handed out each Monday. Students shall complete the pre-lab portion of the lab assignment and hand it in before 5PM the following Monday. The pre-lab must be signed off by a TA before starting on the laboratory session. The sequence is that a lab assigned on one Monday has the pre-lab due the following Monday and the lab itself performed during a session scheduled after the pre-lab is checked.

Late Assignments

Homework is due at the **beginning** of class on the due date. There will be no credit given for late homework assignments.

Collaboration

Collaboration on homework assignments is encouraged subject to the following guidelines:

1. No more than three people can collaborate on a homework solution.
2. Groups of people working together should submit a single homework solution for the group.
3. Any assistance received in the solution of a homework assignment should be acknowledged in writing on the homework assignment.

Exams

There will be two Midterm exams held during the regular class period on **January 30** and **March 05**. There is no Final exam. Each Midterm exam will cover material from the beginning of the course through the lecture immediately preceding the exam. Alternative exam times will be made available only under extreme circumstances. Requests to re-grade exams must be submitted **in writing** within one week after the exams are graded. An exam submitted for re-grading may have all questions re-graded, not just the one requested. The exams will be closed-note and closed-book except that each student shall be permitted one 8.5 x 11 inch sheet of notes.

Grading

Midterm Exams	40% (20% each)
Lab Assignments	20%
Homework Assignments	20%
Final Project	20%

Text & Readings

There is no required text. The course will be taught from class notes handed out periodically throughout the quarter. Readings assigned for a particular day should be completed before the start of class on that day.

Section Leaders

Section leaders are undergraduate students who have demonstrated exceptional capability both in digital design and in interpersonal skills. Section leaders work with current students in EE108A to help them understand course material and to develop proficiency in the laboratory. Each section leader will be assigned to a section of students. Depending on enrollment a section may be between 8 and 15 students. Each student will meet weekly with their section leader in a small group (3-4 students) at a time to be arranged. During these section meetings students and their section leader will go over course material, work

practice problems, review Verilog code, discuss labs and projects, and answer questions. All code assignments will be reviewed with a code *walk through* to give constructive feedback on design techniques and coding style. Section leaders will also assist students in the lab, resolving difficulties compiling Verilog to the FPGAs and debugging. During the project period, the section leaders will periodically monitor the progress of each project team.

Workload

EE108A is a four unit course and hence it is expected that the average student will spend an average of 12 hours per week on the course. This time will be divided between attending lectures and section meetings, reading assignments, homework assignments, and labs. The project is structured so that an "A" grade can be achieved while staying within 12 hours per week. The project is open-ended so an ambitious student can spend as much time as they want adding features and improving performance. However, this is not required to get full marks.

Prerequisites

E40 or permission of the instructor.

E102E

EE108A may be taken concurrently with E102E to satisfy the writing in the major (WIM) require-ment. They must be taken concurrently to satisfy this requirement. You cannot take EE108A one quarter and E102E during a different quarter.

Honor Code

We expect all students to conduct themselves in accordance with Stanford's Honor Code. Please see http://honorcode.stanford.edu/ for more information on the Honor Code.