Problem Set 4  

**Due:** Friday, 25 Oct. 2002

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**Reading:** Razavi, Chapters 4 and 5  
*(The material in this and PS#5 are directly relevant to the midterm design.)*

**Problem 1:** A question that we have left unanswered until now is “In small signal analysis, how small is small?” It’s not hard to answer this question analytically for a long channel device. For a modern short channel MOSFET, though, an analytical derivation can be a largely unrewarding exercise. So, we take this opportunity to learn HSPICE. This problem should not be too intellectually challenging, but it does involve a fair amount of busy work. Sorry, but “busy work” and “simulation” are near synonyms, so it’s best to get used to that fact of a working engineer’s life sooner than later.

Using the models from the class website (to be posted soon), build a simple differential pair of minimum length NFETs, biased with an ideal source of 200µA. Set the input common-mode value to VDD/2, again using an ideal source. Connect the drains directly to VDD; we’ll be measuring the currents as our outputs. For each of three widths (5, 25 and 100µm), use HSPICE to discover the differential-mode transconductance as a function of input differential voltage.

a) Let $V_{od}$ be the overdrive voltage of each NMOS transistor in the balanced case. How large can the input differential voltage get (expressed as a fraction of $V_{od}$) before the transconductance drops to 90% of its value in the balanced case? To 50%? To 10%? Are any of these transistors in weak inversion? Comment.

b) Is your answer to a) sensitive to transistor width over the range considered? Explain.

c) If your design goal is to achieve high linearity (with a fixed bias current, as in our example), should you use narrow or wide devices? Explain. Discuss any tradeoffs that designing for high linearity might involve.

**Problem 2:** P4.14 (Do not use HSPICE for this or any subsequent problem).

**Problem 3:** P4.16 (Yes, this problem is a bit tedious, too; it can’t be helped).

**Problem 4:** P5.2 (This bias circuit is extremely common in practical amplifiers).

**Problem 5:** P5.6

**Problem 6:** P5.23 (This circuit is itself a crude op-amp, and is often the heart of more complex op-amp designs).