Problem Set 5

Due: Friday, 1 Nov. 2002

Reading: Razavi, Chapter 9, up to (and including) 9.8

Note: The midterm design problem will be assigned next week, and will be due the week-before the Thanksgiving holiday break. This problem set is particularly relevant to the midterm design, and solving these problems is effectively the first part of the midterm. It is especially important that you understand all of this material thoroughly, so be sure to clear up any unresolved issues with the teaching staff. There’s also lots of SPICE here. For all simulations, use only the models posted on the EE214 website.

This problem set should not be particularly difficult, but it is a bit long, so please don’t wait until the last minute to start (especially since this exercise may crowd your midterm design time). And do keep checking the website for clarifications and hints.

Problem 1: Even the allegedly simple, relatively compact SPICE models we use in EE214 may not convey design information in the most directly useful manner. It’s often handy to have a collection of $I$-$V$ plots to refer to during various phases of a design. The purpose of this problem is to generate such plots for NMOS and PMOS devices of $10/L_{\text{min}}$ and $20/(2L_{\text{min}})$.

To investigate simulation issues at the same time, also compare two ways of realizing the longer device: First, simply specify the $W$ and $L$ values as given; second, create the longer device out of a series combination of two minimum-length devices.

a) Plot drain current vs. drain-source voltage from 0V to 3.5V, while stepping the gate-source voltage in 0.2V increments from 0V to 2.4V (adjust the polarities as necessary for the PMOS case). Comment briefly on any differences you observe between the single long device and the stacked device.

b) Use SPICE to find the output conductance for gate overdrive voltages of 100mV and 200mV. Make your measurements at a drain-source voltage of 2V. Use these measured conductance values to estimate $\lambda$ for the six devices. Again, comment on any differences you observe for the two ways of making a long device.

c) Simple theory, such as that described in the textbook, predicts that $\lambda$ should be proportional to channel length. Point out any discrepancies between your results and the predictions of simple theory (all we’re looking for are statements like “our $\lambda$ varies more like the cube root of L” or some such quasi-quantitative blather). Yet again, comment on any differences between the two long devices.
d) For the same conditions as in b), compute \( g_m \) and \( g_m'_{\text{out}} \), where \( r_{\text{out}} \) is properly interpreted here as the incremental resistance between the drain and ground, and \( g_m \) is the small-signal ratio of short circuit output current, to gate-source voltage. This computation will help convey the level of difficulty associated with achieving a particular gain per stage.

**Problem 2:** Suppose we want to build a basic one-stage op-amp, much like the one shown in Figure 9.6a on page 296 of the text. Suppose one design target is an open-loop gain of 100. As a crude first pass, let’s optimistically assume that the input NMOS differential pair will have an output resistance similar to that of the load structure. In that case, we might want to design the NMOS input stage to have a gain of 200, when using an ideal load whose output resistance is infinite.

a) Assuming that the input pair will be biased with a total tail current of 150\( \mu \)A, use SPICE (or, equivalently, your plots from Problem 1) to determine the device width that produces the desired \( g_m r_{\text{out}} \) product for the longer device realized by stacking. You might be uncertain initially about a factor of two gain here or there; resolving this issue is one important aim of this problem. Also, does it matter whether the bias current source has a finite output resistance? State your assumptions and explain your reasoning. Also pay attention to (and comment on) whether your transistors are indeed in strong inversion. Remember that models may behave oddly near the transitions between boundaries (e.g., between triode and saturation, and near threshold).

b) Now assume that the bias current is supplied by a transistor circuit whose output voltage is not permitted to go below \( V \) volts. What is the lowest permissible input common-mode voltage?

c) What is the expected 3dB bandwidth of the op-amp, if the output is loaded with a 250fF capacitor to ground? Here, assume that the op-amp is driven purely differentially. Assume further that the driving source has a half-circuit resistance of 1k\( \Omega \) (so that its total differential resistance is 2k\( \Omega \)). Finally, assume unrealistically that the PMOS transistors making up the mirror load have precisely the same characteristics as those of the NMOS differential pair, as far as output resistance and capacitances are concerned. Present both an open-circuit time constant calculation as well as a SPICE simulation of the bandwidth. You should feel free to disregard “insignificant” time constants, but you must justify any such neglect.

d) Set the input common-mode voltage at 1V. Using SPICE, what is the lower end of the output common-mode range, defined for our purposes here as the output voltage where the small-signal gain has dropped to 50% of the maximum value? Find this number by applying a differential twist to the input. How does this number compare with simple first-order theory (i.e., one threshold voltage below the input voltage)? Discuss any discrepancy.