Midterm Design Problem

READ THIS ENTIRE HANDOUT THOROUGHLY!

Your job at startup FlyByNight Circuits is to design an op-amp capable of operation with a single supply voltage of 3.5V. After an exhaustive study of the business opportunity, FBN’s marketing department decide that the op-amp should meet the following specifications:

- |voltage gain|: as much in excess of 1000 as you can achieve (open-loop, low-frequency, small-signal, and over input common-mode values ranging from 1V to +3.5V); measured as the ratio of single-ended output voltage to differential input voltage at CM output voltage = 2V.
  - Small-signal bandwidth: > 5MHz; measured in a follower configuration at 2V CM.
  - Output swing within 250mV of both supply rails (measured at 2V input CM).
  - Here, we’ll arbitrarily define “swing” as where the s.s. gain has dropped to 200.
  - On-chip capacitance of no more than 10pF.
  - Load capacitance = 500fF; there is no external load resistance to worry about.
  - Phase margin in follower configuration with specified load connected: > 45°.
  - Maximum quiescent power of 5mW (measured at 2V output voltage and 2V input CM).
  - Low-frequency CMRR of at least 70dB; measured at 2V input CM.
  - Systematic input-referred offset < 250µV; measured at 2V input CM; assume perfectly matched devices (i.e., don’t worry about random offset).
  - Follower rise and fall times (10-90%) < 250ns; measured with +1V to +3V step.
  - Total on-chip resistance < 100kΩ; assume the availability of perfect resistors, but only specify value to one significant digit (this applies also to the total value of a series or parallel string, so you can’t finesse your way out of this constraint that way).
  - Device widths can be specified only in increments of 0.25µm.
  - T = 25°C; V_{DD} = 3.5V; V_{SS} = 0V.

Note that, strictly speaking, you only have to meet these specifications at just one temperature and supply voltage. However, we still require that your circuit not be overly sensitive to either (i.e., no “marble balanced on the tip of a cone” behavior). We will be the final judge of whether such a condition exists. If you are unsure, please consult the teaching staff early on.

Copy the SPICE models from the class website. Do NOT use the models from the textbook (or any other place). That way, the only transcription errors will be ours.
We **require** the following format for your report. Be sure to follow this **EXACTLY**:

Page 1: Schematic diagram, with component values and bias currents **clearly** indicated. **Indicate component values right next to the components, and currents next to the branches** (i.e., absolutely, positively do not make us refer to a look-up table; we will **punish you if you do**). The idea is to make it easy for us to figure out quickly what’s going on (*you* try grading 100+ reports, and you’ll sympathize with this position!);

Page 2: Summary table of specifications achieved, showing bandwidth as predicted by open-circuit time constants, and summary of other specifications as predicted by hand calculations, all compared with what SPICE says;

Page 3+: SPICE deck and output showing that your design meets all specifications.

The rest of the write-up **must** include a discussion of how you did the design, as well as a description of your final circuit. Please be succinct and clear; to enforce this requirement, this portion may not exceed 5 pages (not 5 sheets) of double-spaced text in 12 point Times font. Show your formulas (and values) for all specifications, including (but not limited to) gain and open-circuit time constants. Also comment on any discrepancies between your hand calculations (which should involve simplifying approximations that you clearly state) and SPICE (which uses everything). **Be quantitative whenever possible.** As a final note, leave all formulas in unexploded form, (e.g., if two resistors are in parallel, express that relationship as $R_1||R_2$).

Be sure to check for announcements concerning this design problem. Questions concerning interpretation of specs, etc., invariably arise; we will post clarifications as needed. Furthermore, we will post instructions on how to submit your netlists electronically (we will use scripts to run HSPICE automatically so that everyone’s designs will be evaluated uniformly and independently by us).

While you are permitted, indeed encouraged, to discuss general design ideas with your classmates and staff, your design and write-up are to be individual efforts. Let your conscience and the spirit of the Honor Code guide you.

Finally, and **this is important**: DON’T WAIT UNTIL THE LAST MINUTE TO START. This midterm involves a great deal of just plain old labor; it takes significant amounts of time to run all the necessary simulations for even one design, and most folks will go through several design iterations, especially since this midterm has an open-ended specification on gain. Also, the computers and printers in Sweet Hall and elsewhere have been known to slow down and even go down at the worst possible times. We will be largely unsympathetic to pleas for extensions arising from such problems. To encourage you to start early we make this offer: We will evaluate **one** of your preliminary designs with our (semi-)automated checker if you submit it **electronically no later** than 5pm, exactly one week before the final due date. That way, you can catch gross errors early enough to recover (or, more optimistically, discover that your answers agree with ours, and that you are done). Watch for instructions on how to submit your design. To keep out staff from overloading, we will insist on your slavish adherence to a standard submission format. If your submission does not run, it will simply not be graded.