**Operational Amplifier Simulations**

Opamps have very high differential gain and any small offset voltage can saturate an opamp to the positive or the negative supply rail. Opamp simulation in SPICE can be difficult especially in the open loop as you have to find the exact offset voltage before any kind of open loop test can be performed.

**1- Offset Voltage**

Offset Voltage is an external differential voltage applied at the opamp input which keeps the dc level of the output at the nominal common mode value. If we do not apply proper offset voltage at the input terminals, the opamp devices may not be biased correctly and any AC analysis will use models extracted in the wrong device operation regions (typically resulting in measured values that seem worse than they actually are).

There are many different simulation methods to find offset voltage. Fig. 1 shows a simple approach. Apply a differential voltage source at the opamp inputs and sweep its DC value, measure the value of the input voltage when your output is exactly the common mode voltage required (i.e. 2V in your case). Be careful to set your DC step size to microVolt range so your sweep has high enough resolution. This method is not practical for lab use though, however it works well for simulations.

This is the method that will be used in grading your design. Do not forget that every design change, no matter how simple it maybe, can change your offset voltage completely. So you will need to adjust the offset compensation after design changes. Try to develop a method for extracting your offset voltage quickly.

You have to satisfy the gain requirement for a specific input common-mode range (1V to 3.5V). Extract three offset voltages—one for nominal input common mode voltage of 2V and one for
each of the two extremes (1V and 3.5V). Also keep in mind that the DC value of output voltage should be 2V (nominal common mode value) for the whole range of input common mode.

2-Open Loop Differential Gain, Phase Margin, Bandwidth

Fig. 2 shows the test circuit used for grading. Vin is divided into two halves, each with numerical AC value of 0.5 (to get the convenient value of 1 for total differential AC input signal). Make sure your circuit has correct Vos applied before you can get any meaningful results out of this test. We will extract your DC gain for three values of input common-mode: 1V, 2V and 3.5V. In all the three cases your gain should be greater than 1000, though it does not need to be constant.

![Fig. 2 Open Loop diff gain, BW, phase margin measurement](image)

Fig. 3 shows the follower configuration used to measure bandwidth and phase margin. Note that you do not need to add any offset for the follower configuration as it will automatically balance itself due to feedback. The output DC level will not be exactly 2V, instead it will be equal to the input offset voltage (<250µV). Input voltage, Vin, consists of the 2V common-mode input as well as an AC small-signal input.

![Fig. 3 The follower BW and phase margin measurement](image)
The small signal bandwidth in the follower configuration will turn out to be fairly close to the
unity-gain crossover frequency of the open-loop frequency response. A common mistake is that
you might reverse the positive and the negative terminals when trying to hook up the follower cir-
cuit. An easy way to find the correct polarities is as follows: if you increase the input voltage at
the positive terminal, the output should also increase (and vice versa for the negative terminal).

3-Common mode gain and CMRR

The test circuit of Fig. 1 (above) can also be used to measure common-mode gain, Acm. This
value, along with differential gain, is then used to determine CMRR. Using this method, your
common-mode signal should consist of both a DC (2V) and AC component. Note that you are
only required to maintain a specified CMRR at a common-mode input of 2V and at low-frequency
(i.e. DC).

4-Power

Power can be directly read from the spice output list file. Make sure you include .op in your deck
to perform DC operating point analysis. .OP analysis will give you DC voltages, currents, and
power.

5-Output Swing

Our specification of output swing is based on change in the small signal gain with the change in
the DC output level. Defining small signal gain we assume that the output is at 2V DC level. The
output swing specification requires you to guarantee that your small signal gain does not decrease
below 200 even when output DC level is just within 250mV of the rails. One easy test setup will
be similar to the one in Fig 2. All you need is to find the two offset voltages required to make
your DC output level equal to 250mV and 3.25V. Adjust the output DC level using these offset
voltages and find the small signal gain using ac analysis.

Another method to test your swing is shown in Fig. 4. The opamp under test is forced to maintain
its output at a desired DC level (250mV and 3.25V in this case) by an external amplifier. There is
an RC filter at the output of external amplifier which has a very large time constant (zero band-
width). This filter basically feedbacks only DC and blocks any AC signal. The source Vin con-
sists of a 2V common-mode component and a low frequency (~10Hz) AC component. This
method will give you results similar to the method described earlier however absence of offset
measurement makes it easier to use. We will be using this one to test your opamp.
6-Follower Rise and Fall times

Fig. 8 shows the simulation scheme to measure follower rise and fall times. The opamp is wired in a follower (buffer) configuration. A pulse source of 1V to 3V is connected to the input. At the output you should measure the time which the output takes to change from 10% to 90% of the final value. Note that your amplifier step response may contain ringing, which is acceptable. If, however, the ringing does not diminish to zero amplitude within a reasonable amount of time, you have designed an oscillator, which is unacceptable. This is a *very important* test to pass to ensure you do not get a zero for the project.
7- SPICE Deck Format

Please strictly follow the guidelines given in the accompanied handout on Project Submission Procedure. The script used to evaluate your designs is completely automated, so failure to comply exactly to the submission procedures may result in the scripts rejecting your design. And that’s just not good.

8- Non-Minimum Length Transistors

The level 3 models we are providing are good enough only for 0.5um long device. If you want to use longer devices, you would need to stack up minimum size (0.5um) devices. To ease your job we have provided subcircuits which represent longer transistors. The file transistors.lib, available on the website, provides stacked devices up to L=8.0um. You should copy these files to you own directory and include them with your spice deck using .include command. If you need longer devices, you will have to create them yourself.

Important Points and Suggestions

1- Offset voltage may completely change even if you only slightly change your design ... make sure you find the offset voltage after every design change.

2- Always measure any quantity using .measure statement if you need accuracy. Mwaves can only give you a rough idea if you are not careful enough. Always measure values exactly at the point where you performed your analysis otherwise you will get interpolated results.

3- .AC performs analysis on the extracted AC model, it does not perform analysis on the original circuit. You can easily see voltage swings beyond Vdd because .ac analysis forgets about the original circuit and it only works on AC models. Do not get confused by this.

4- If you are using wrong offset voltage, some of your transistors may be in triode or cut off completely. .AC analysis will extract their AC models in respective regions and will perform AC analysis on that model, giving you completely wrong (and usually pessimistic) answers ... BE CAREFUL to use the right offset.

5- .TRAN performs an analysis on the original circuit. Watch out for "internal timestep too small" which indicates oscillations in most cases.

6- Take a look at your SPICE output file and make sure all the drain currents and node voltages are reasonable. Also watch out for negative mos transconductances which usually indicates that your opamp is oscillating (not good!!)

7- Direct your SPICE output to a file e.g hspice opamp.sp >! opamp.lis note: ! makes it overwrite the previous opamp.lis. View opamp.lis for simulation result details.

8- Before you look at your analysis results, always make sure that your Vout=2V (unless measuring output swing) in the spice output file to verify that you used the correct offset voltage. This is the most dangerous pitfall and you can waste lots of time figuring it out.
9- Any kind of oscillations in the output should eventually diminish to zero in a .TRAN analysis. If they do not, your opamp is oscillating (not acceptable).

The following resources may prove useful:

SPICE Manual (available at the class website):
3-34, 35, 43, 44 thru 47, 56, 59 thru 61, 65 thru 67
4-6, 19 thru 34, 47 thru 50, 52 thru 54
5-37, 38
6-6 thru 9
7-4 thru 7

Razavi text:
Ch8
Ch9
Optional Ch 16, 17