# Lecture 10
# Circuit Design Rules of Thumb

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## Overview

- What:
  - Sets of design guidelines, practices, numerical rules to follow when performing custom designs
- Why:
  - "Construct it right" to begin with
  - Save simulation effort spent on common cases
  - Manage design uniformity/risk
- How:
  - Methodology book
  - CAD tool checker - "If you can't enforce it, the rule does not exist"
- Objective of this lecture
  - Get a sense of what issues are of concern in a real world design environment
  - How trade-offs are made (80/20 rules)

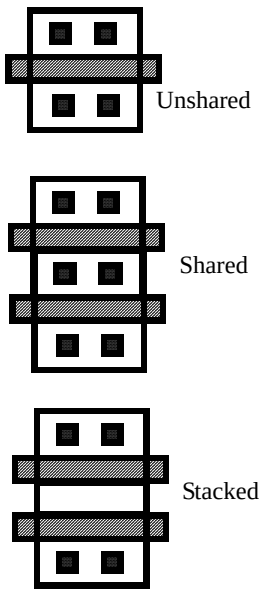
# Topics in “Rule of Thumb” Book

- Basics
  - Tabulated technology parameters
- Schematic design practices
- Layout design practices



# Basic Technology Parameters

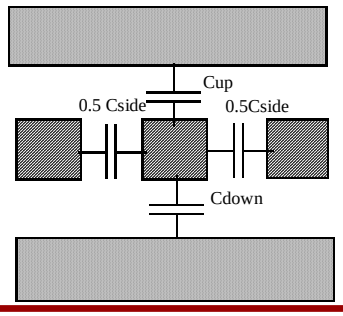
- Inverter delays
  - “Intrinsic” and “fan out dependency”
- Gate cap per um
  - Various flavors of transistors
- Diffusion cap per um
  - Layout topology matters (unshared vs. shared vs. stacked)



# Basic Technology Parameters

- Wire Rs and Cs
  - Impact of width and spacing
  - 1x, 1.5x, 2x of minimum w/s typically tabulated
    - Microprocessor technology typically have “inversely scaled” interconnect technology. For example, 1x w/s for lower level, 2x w/s for intermediate level, 4x w/s for upper level
    - For a particular level (say intermediate level), the minimum w/s is y (y=2x in this example). In that layer the width and spacing of signal lines typically do no go beyond 2y
    - Between y and 2y, increase of width/spacing bring down the resistance per length without much penalty in cap per length

| Width | Spacing | Resistance (Nomalized) | Ctotal (Nomalized) | RC (Nomalized) | Cside/ ($C_{up}$ +$C_{down}$) |
|---|---|---|---|---|---|
| y | y | 2 | 1.1 | 2.2 | 2.1 |
| y | 2y | 2 | 0.8 | 1.6 | 1.0 |
| 1.5y | 1.5y | 1.3 | 1 | 1.3 | 1.1 |
| 2y | y | 1 | 1.2 | 1.2 | 1.3 |
| 2y | 2y | 1 | 1 | 1 | 0.7 |



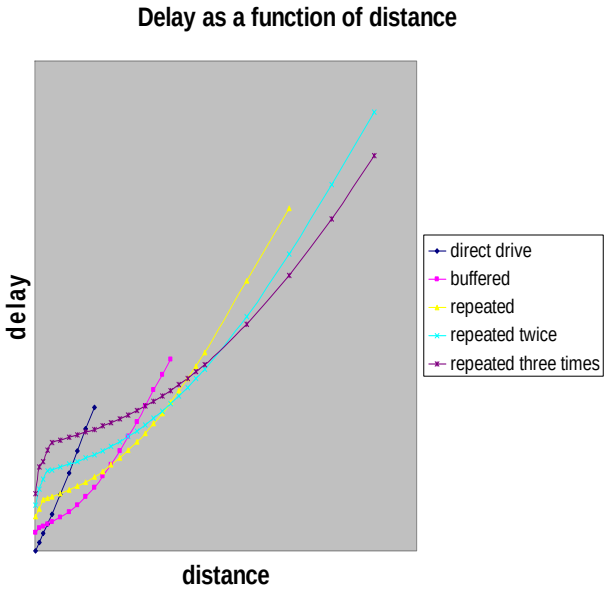



# Schematic Design Practices

- Correctness related rules
- Efficiency (design effort) related rules
- Optimization (performance/area) related rules
- Technology migration related rules
- Power efficiency related rules
- Intertwined
  - A given rule belongs to multiple categories
  - Quantification needs to balance trade-off among several objectives
- Examples given in the following slides
  - Why, how, and scaling trends more important than absolute values

# Repeater (Buffering) & Slew Rate Rules

- Optimum repeater is a well discussed topic in EE 371
- Additional factors to account for in real life design:
  - Need to meet the coupling noise criteria
  - Current carried by the wire meets the reliability criteria
  - The slope at the end of the wire will not cause excessive “shunt” current for the target load
- Slew rate upper limit rules needs to factor in similar consideration






# Beta Ratio

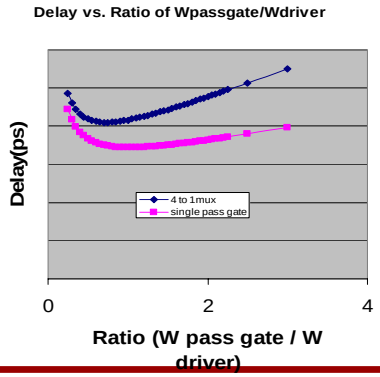
- Criteria:
  - Balancing rising and falling edges
  - Delay consideration
  - Input noise margin consideration
  - Area/power consideration
- Need compromise
- Weights for objectives different between static vs. dynamic styles
- “Typical” 90 nm values
  - See the effect of velocity saturation

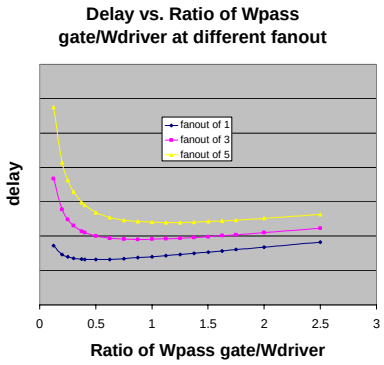
| Gate Type | Beta (Static) | Beta (“Dynamic” - that for the static gate in a complex dynamic gate combo |
|---|---|---|
| inv | 2 | 6 |
| nand2 | 3 | 6 |
| nand3 | 3.5 | 6 |
| nor2 | 2 | 5 |

# Transmission Gate Sizing

- Pass transistor sizing optimization (speed/power area)
  - Ratio of the pass gate vs. driving inverter
    - Optimization result sensitive to the number of inputs

•Also sensitive to the “fan out” between the load and the driver

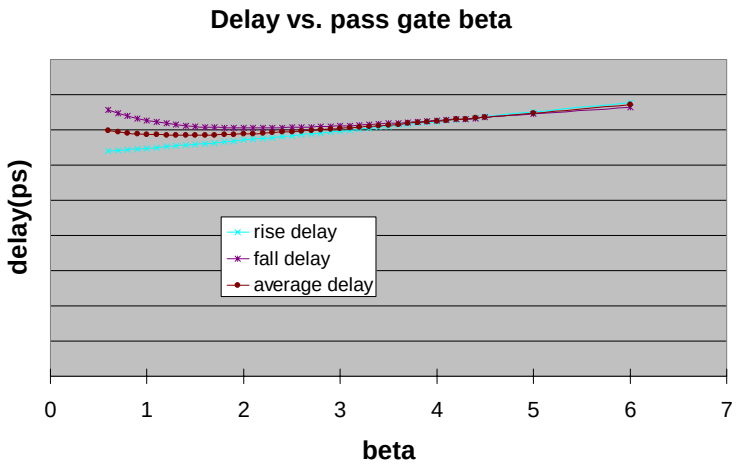





# Transmission Gate Sizing

- Optimization of Beta ratio of the pass gates



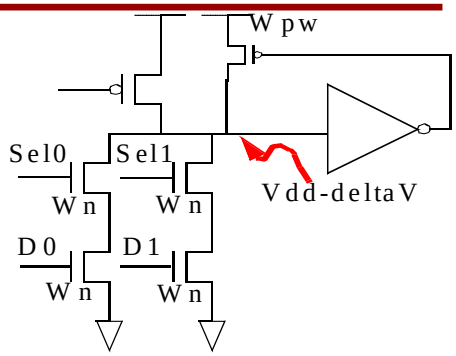
# Rules for Dynamic Circuits

- Dynamic gate:
  - Faster logic (especially for high fan-in) at the cost of design complexity and clock/power overhead
- Three tightly coupled issues:
  - Keeper sizing for leakage fighting and low delay impact
  - Charge sharing effect
  - Input noise criteria
- Other considerations:
  - Rules related to the contention current through the evaluation chain
  - Rules related to the contention current in the inverting buffers



# Keeper Sizing for Leakage Fighting

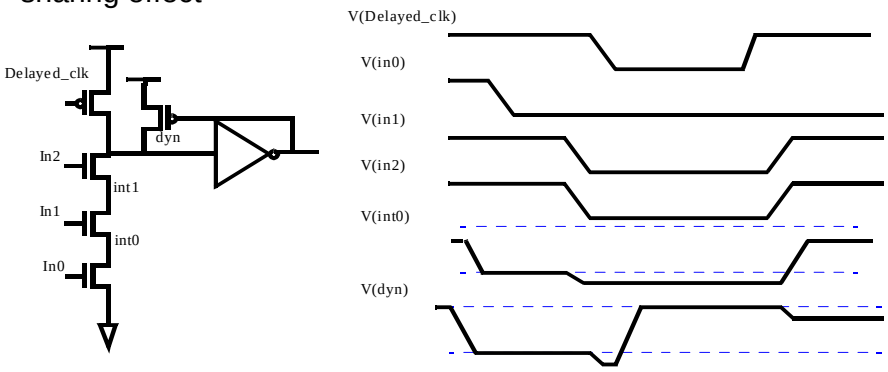
- Part of dynamic node signal degradation budgeted for leakage fighting
- Need to consider the worst case: PVT corners and input topology (fast n, weak p, high Vdd, high T)
- Minimum feedback pull up strength set up “leakage droop” budget
- Delay impact sets maximum limit on feedback pull up strength
- As technology migrates, the “head room” for large fan in topology gradually diminishes
- Non minimum channel and “second to fastest grade” transistor may be better choice for dynamic gate




Worst case for leakage:
Sel0=Sel1=0, D0=D1=1,
Wpw/(2xWn)>Criteria1
Worst case for speed:
Sel0=D0=0, Sel1=D1=1,
Wpw/(Wn/2)< Criteria2
=> 2C1< (Wp/Wn)< C2/2
C2/C1 is getting worse as transistors are getting leaky

# Charge Sharing Effect in Dynamic Circuit

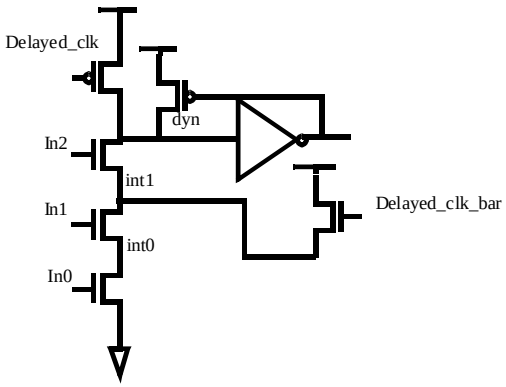
- Charge sharing with the dynamic node degrades signal
- The worst case sequence is worse than typically considered
- Part of dynamic node signal degradation budgeted for charge sharing effect





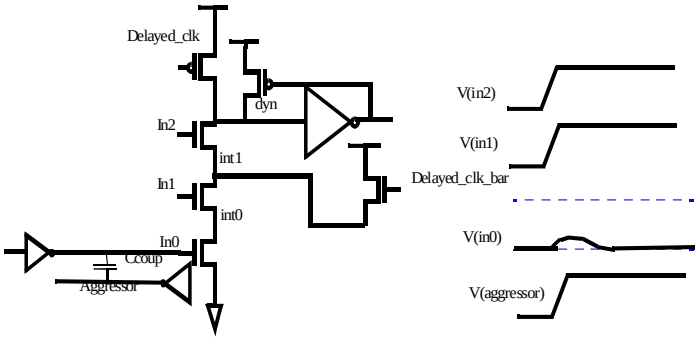

# Charge Sharing Effect in Dynamic Circuit

- Pre-charging internal node is a typically charge sharing solution
- Examples of “rule of thumb” bounding the charge sharing effect
  - Stack height has to lower than x
  - Intermediate node above stack height y has to have pre-charge transistors



# Rules on Noise Limit for Dynamic Gate Inputs

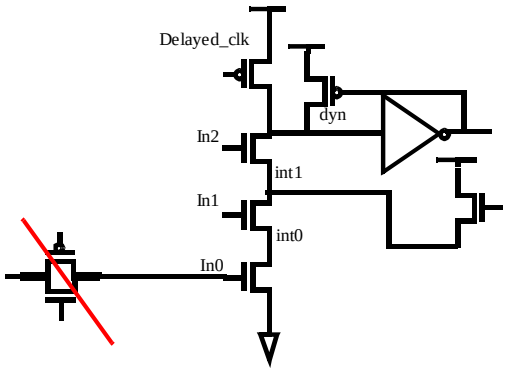
- Portion of dynamic node signal degradation budgeted for charge sharing can be traded-off for the portion budgeted for leakage
- Input noised induced degradation shared the same “total budget”
- “Worst case additive” method no longer provides a reasonable final “degradation budgeting” plan
- Transient nature of the noise has to be taken into consideration





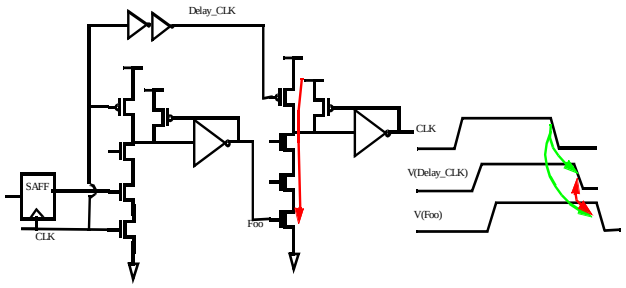

# Rules on Noise Limit for Dynamic Gate Inputs

- Beta of the static inverter is yet another input parameter
- Pass gate/Mux output as driver for dynamic gate input should be banned
- “Noise shape constraints” has to be separately checked



# Power Related Rules for Dynamic Gate

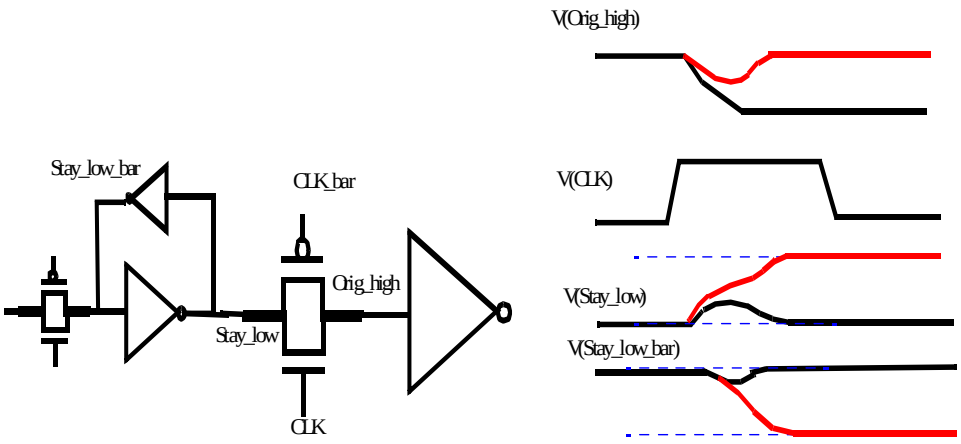
- Slope for pre-charging process affects “shunt” current in the inverter and needs to be limited
- “Shunt” current in the evaluation chain for “footless” domino needs to be checked
  - “Footless” domino saves clock power
  - But possible “power race” during pre-charge
  - “Power race margin” needs to be checked





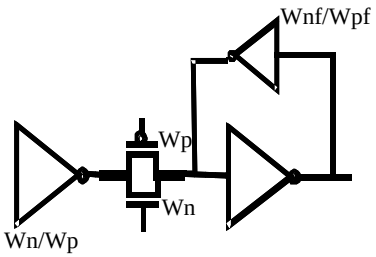

# Charge Sharing in Static Design

- Charge sharing can affect the functionality of a latch node held by static feed back



# Writability Rules

- Contention based circuit used for better area
- Functionality across corners are guaranteed through thorough corner simulations plus margins
- Define min. driver/keeper driving strength ratio



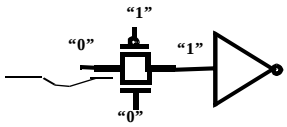

$W_{eff\_driver}/W_{eff\_feadback} > Ratio\_for\_writability$

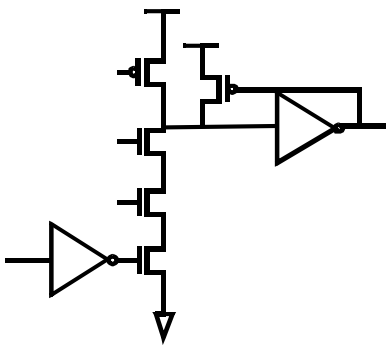
**For example, (Wn/2)/(Wpf/2) > 3, or Wn > 3 Wpf**



# Coupling Noise Limit

- Static gate inputs have most input noise suppression capability
- Topologies that need unique noise limit
  - Dynamic gate input
  - Pass transistor input
  - Input to static gates that drives a dynamic gate



# Rule of Thumbs on Clocks

- Skew budgeting
  - Amount of skew allowed at each level of clock tree
- Clock wire width as a function of per pitch clock load
  - Super linear dependency on load
  - Mandates maximum for per pitch load or size of the flop
- Via constraints at the driver side of a clock wire
  - Resistor at the driving end of a clock wire contributes dis-proportionally to skew
  - Modern processes have high resistive via
  - Need to jump a few layers before get to the clock wire
- Rule of thumb for datapath clock generator selection



# Inductive Noise Prevention

- Inductive noise can be an issue on low R (top level) wire
  - Delay and crosstalk show dependence on inductance when
  - $C_{load} << C_{wire}$
  - $R_{wire}/Z_0 <= 0.5$
  - $Z_{driver} < Z_0$
- “Near return” path is a practical fix – Need “rule of thumb” for triggering threshold
-

## Scalability of the Design

- Full customs design need to survive multiple technology nodes to recoup design cost - scalability important
- Design implications:
  - Buffer insertion needs to be biased in the “buffer delay heavy” end vs. wire delay heavy end for the first design in a series
  - Need to bound the percentages of wire delays within a cycle (also a consideration for voltage scalability)
  - Leakage sensitive circuits – need to think ahead
- SOI “portability”:
  - Allocate area for floating body effect sensitive circuits

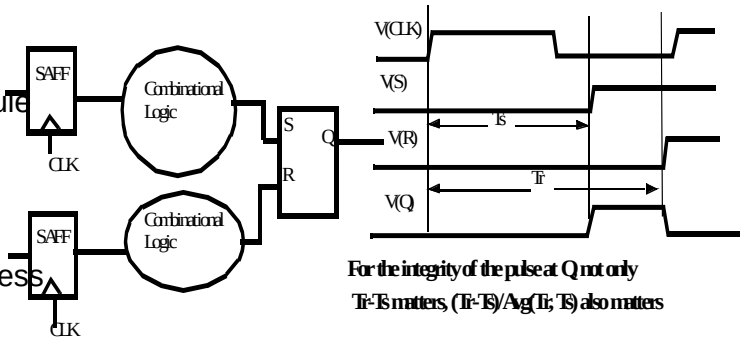


## Usage Limitation of Various “Flavors” of Transistors

- Foundries provide multiple “flavors” of transistors
  - Low Vt grade for higher speed (20%-30%), but with huge (~10X) impact on leakage power
  - Medium and high Vt grade available
  - Medium grade Vt is targeted towards a few watts of leakage power for a “large” chip
- Judicial usage of lower Vt grades are required
  - “Rationing” of faster grades of transistor specified by the methodology book
  - Past design data points needs to be taken into consideration

# Racing Criteria

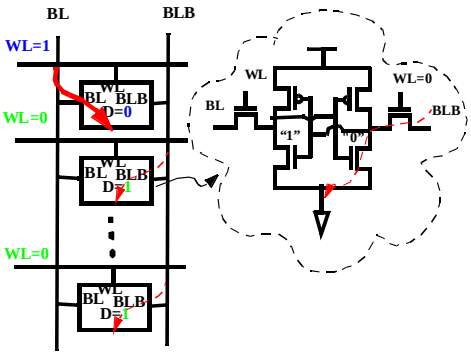
- Minimum number of logic gates between flops
  - Not meant to be a replacement for final hold time check; more for an early feedback for hold time issues or inappropriate hold time fixes
- Minimum % difference rule between racing paths
  - Delay elements with metal option enable are typically used to deal with modeling errors
- Minimum pulse width rule
- "Power races"
  - Dynamic gate in
  - pre-charging process
  - Nodes driven by
  - multiple tri-state drivers





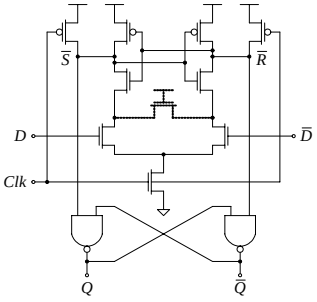

# RAM Structures

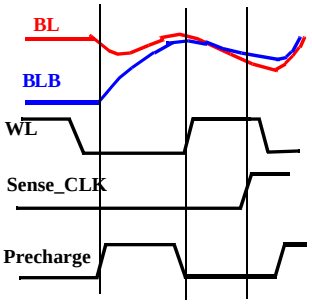
- Speed estimation: bit line separation rate
- Leakage related functionality issue:
  - Pathological worse case: for a bit line of n bits, 1 bit with data active pull down, n-1 bits with data_bar leaking
  - Max bit line length (# of bits)



# RAM Structures (cont.)

- Redundancy rules
  - Number of spare rows/columns per bank of x bits
- Sense Amp margin rule
  - mV of differential signal when “sense amp fires”: V(clk) = Vt
- Simulation sequence
  - RAW case with opposite data typical worse case
  - Need to factor in leakage worst case
  - WAW, RAW, RAR can also be worst case depending on design

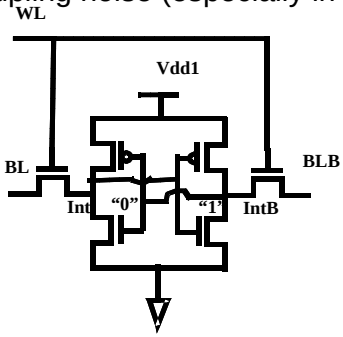


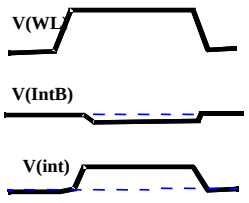






# RAM Structures (Cont.)

- Cell Stability
  - “Text book definition”
- Practical design consideration:
  - Need to consider power supply offset, and wordline/bitline coupling noise (especially in a multi-port cell design)




**For read-disturb, consider V(WL) > Vdd1**
**For writability, consider V(WL) < Vdd1, V(BL) > 0**

## Reliability Related Rules of Thumb

- Electromigration
  - Average current limit
  - RMS current limit: Self-heating accelerated degradation
  - Current industry flow: Post layout static analysis
  - Goal for the “rule of thumb”: reduce # of violations and # of iterations
- Current profile related to: clock rate, activity factor, load cap, fanout
- Rule of thumb characterization
  - De-rated load per “nominal” wire/via



## Rules for Better Productivity

- Direction of data flow
- Sizes of schematics
- Bit ordering
- Matching of hierarch between schematics and layout
- Naming convention

## Min/Max Transistor Width

- Min width
  - Typically the width that allows a single contact
  - Avoid dog-bone style layout and “cliff” for narrow width effect
  - Increase the channel length if “weaker” driver is desired
  - Usually want to avoid L > 2xLmin
  - Putting transistor with same gate driver in series rather than using > 2xLmin if needed

- Max. width (per finger)
  - RC of silicided gate:
    - 0.1um, W=Xum, gate RC = 10% fan of 4 delay (single sided contact)

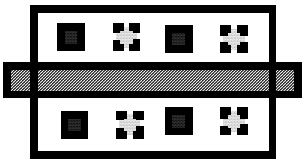


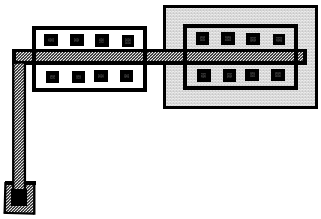
## Datapath Pitch

- Function of design and interconnect technology availability
- Min. width bounded by the need to cover the per bit pitch wire routing band width
- Max. width bounded by impact on clock skew across dp
- Other considerations:
  - DP aspect ratio
  - Delay for control signals
  - Track plan

# Rules for Better Electrical Integrity

- Non-strapped diffusion rule
  - How often can one skip contacts
- "Poly jumper rule"
  - How long can a poly interconnect be

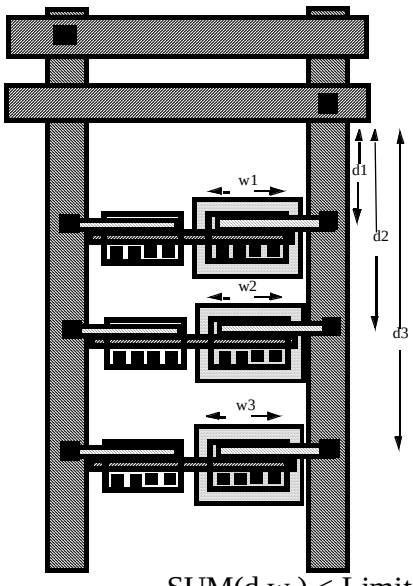






# Rules for Better Electrical Integrity

- IR drop "budgeting"
  - Global vs. local IR drop
  - Maximum distance between power strapping in non grid layers as a function of "current source distributions"




$$\sum_{i=1 \text{ to } N} (d_i w_i) < \text{Limit}$$

# Conclusions

- Rule books provides a way to
  - Ensure the functionality
  - Increase performance
  - Increase productivity
- Compromises are needed
- Dynamic change as design/process technology makes forward progress