Transistors

ENGR 40M lecture notes — July 10, 2017

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A transistor is an electronic device that is used to allow one electrical signal to control another electrical signal, typically larger in either voltage or current. Applications fall into two groups: *amplifiers* and *switches*. There are two main classes of transistors: *bipolar* transistors and *field-effect* transistors. Each class can be used in either application.

In ENGR 40M, we will study a simplified model of a *metal–oxide–semiconductor field-effect transistor*, commonly known as a *MOS transistor* or *MOSFET*, that models its use as a switch.

MOSFETs come in two types: the *n-channel* MOSFET (*nMOS*) and the *p-channel* MOSFET (*pMOS*). Both have three terminals: the *gate*, *drain* and *source*. Their symbols are shown below. It is convention to draw the nMOS with the source at the bottom, and the pMOS with the source at the top.

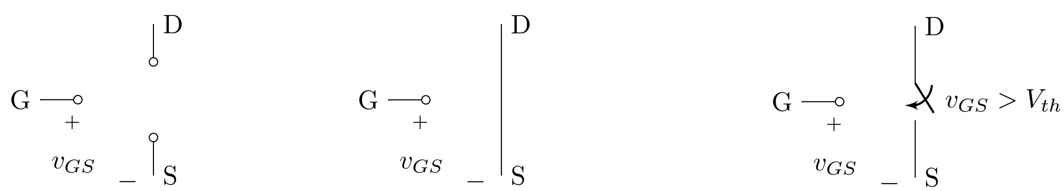
nMOS **pMOS**

Ideal MOS transistor switch

In the ideal transistor switch, the connection between the drain and the source acts like a switch that is controlled by the voltage between the gate and the source, v_{GS}.

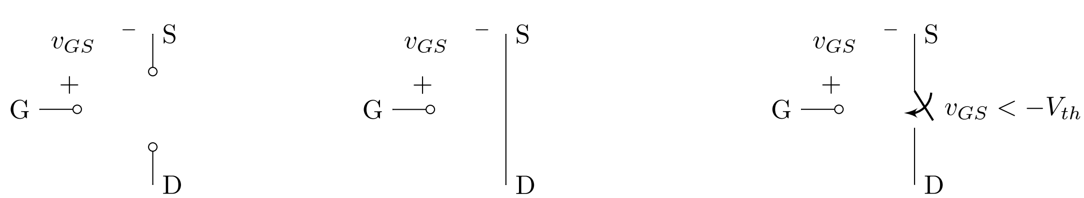
In an **nMOS**, when v_{GS} is greater than the *threshold voltage* V_{th}, the transistor turns on and the "switch" is closed. Otherwise, the transistor is off and the connection between the drain and source is open.

The threshold voltage is typically between 1 V and 2 V.



nMOS off: $v_{GS} < V_{th}$ nMOS on: $v_{GS} > V_{th}$ nMOS model

The **pMOS** is similar, except that it's flipped: it turns on when $v_{GS} < -V_{th}$.

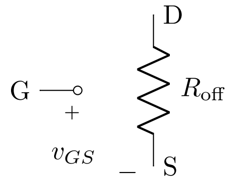


pMOS off: $v_{GS} > -V_{th}$ pMOS on: $v_{GS} < -V_{th}$ pMOS model

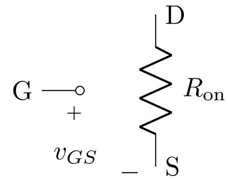
Modeling internal resistance

Real transistors aren't perfect open circuits when off and perfect short circuits when on. In practice, there is a large resistance when off, and a small resistance when on. In some applications, this resistance can be signficant, and needs to be accounted for when designing your circuit.

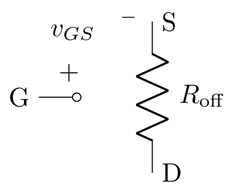
We call the "off resistance" R_{off}, and the "on resistance" R_{on}.



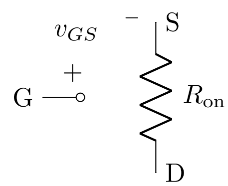
nMOS off: $v_{GS} < V_{th}$



nMOS on: $v_{GS} > V_{th}$



pMOS off: $v_{GS} > -V_{th}$



pMOS on: $v_{GS} < -V_{th}$

Usage notes

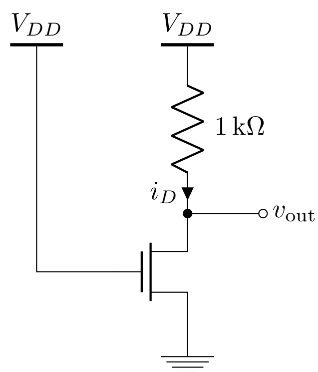
- Because the source is involved in both the "input" (gate) and "output" (drain), it is common to connect the source to a known, stable reference point.
- Because, for an nMOS, v_{GS} has to be (very) positive to turn the transistor on, it is common for this reference point to be ground. Similarly, for a pMOS, since v_{GS} has to be (very) negative to turn the transistor on, it is common for this reference point to be V_{DD}.

  Special penalties will apply if you connect the source of an nMOS to V_{DD}, or the source of a pMOS to ground, in a circuit that you draw in homework, prelabs, labs or an exam.
- In many (digital) circuits, including most (but not all!) circuits that we will study in this class, the input voltage is by design always V_{DD} or $0\,\text{V}$, *i.e.* always well below or well above the threshold voltage.
- Note that, in our model, there is never any current going into the gate of a MOS transistor.

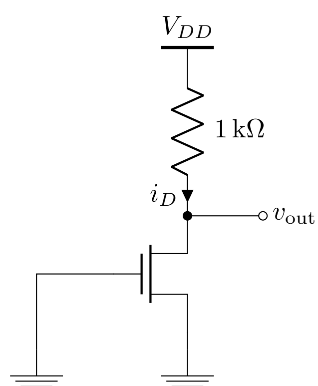
Examples

Unless otherwise specified, $V_D D = 5\,\mathrm{V}$, and $V_{th} = 1\,\mathrm{V}$ for all transistors.

Example 1. In the circuit below, (a) what is v_{out}? (b) what is i_D?

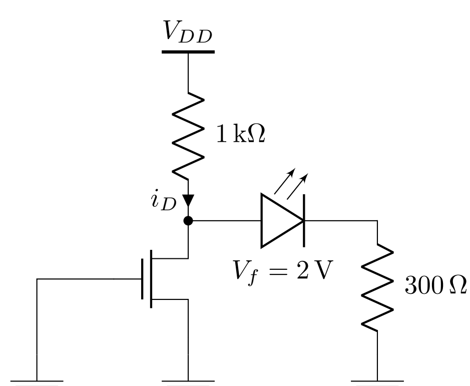


Example 2. In the circuit below, (a) what is v_{out}? (b) what is i_D?



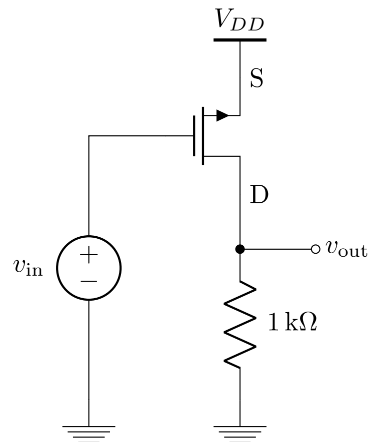
The next example shows that putting a load on the output changes the behavior of the circuit in Example 2.

Example 3. In the circuit below, what is the current through the LED?



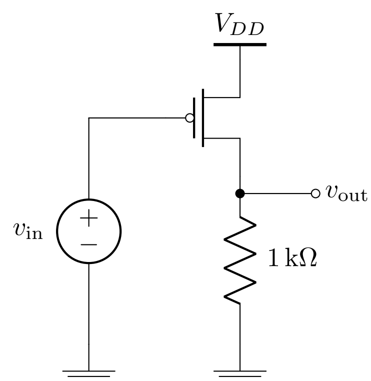
It might be tempting to resolve the problem in Example 3 by connecting the nMOS to V_{DD} instead. Unfortunately, this doesn't work.

Example 4. In the circuit below, if $V_{th} = 2\,\text{V}$, what values of v_{in} would turn the transistor on?



This illuminates one problem: we need voltages higher than V_{DD}, which you don't have access to in most circuits. In fact, this isn't the only problem. In many transistors, when placed in this configuration, the drain will behave like a source and vice versa, and the transistor will no longer act as a switch, making our model inappropriate. For digital circuits, an nMOS can't be used like this: a pMOS must be used to make connections to V_{DD}.

Example 5. What is v_{out} when (a) $v_{\text{in}} = V_{DD}$, (b) $v_{\text{in}} = 0\,\text{V}$?



Example 6. Repeat Example 5 with $R_{\text{off}} = 100\,\text{k}\Omega$ and $R_{\text{on}} = 50\,\Omega$.

Example 7. For both transistors, $R_{\text{off}} = 100\,\text{k}\Omega$ and $R_{\text{on}} = 50\,\Omega$. Find v_{out} when (a) $v_{\text{in}} = V_{DD}$, (b) $v_{\text{in}} = 0\,\text{V}$.