Midterm Examination #2
Open book, open notes. Time limit: 2 hours

Honor Code Acceptance: This examination has been written according to the spirit and principles of the Stanford Honor Code.

<table>
<thead>
<tr>
<th>Problem</th>
<th>Score</th>
</tr>
</thead>
<tbody>
<tr>
<td>#1</td>
<td>/ 12</td>
</tr>
<tr>
<td>#2</td>
<td>/ 13</td>
</tr>
<tr>
<td>#3</td>
<td>/ 20</td>
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<td>#4</td>
<td>/ 20</td>
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<td>#5</td>
<td>/ 10</td>
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<tr>
<td>#6</td>
<td>/ 25</td>
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<tr>
<td>Total</td>
<td>/ 100</td>
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</tbody>
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Signature

Print Name
1. (12 points) Multiplication. The unsigned product of 2-bit numbers \(A_1A_0\) and \(B_1B_0\) is a 4-bit result \(Y_3Y_2Y_1Y_0\). For example,

\[
11_2 \cdot 11_2 = 3_{10} \cdot 3_{10} = 9_{10} = 1001_2.
\]

Find efficient Boolean formulas for the product bits \(Y_3Y_2Y_1Y_0\) as functions of the bits of the multiplier \(A_1A_0\) and the multiplicand \(B_1B_0\).

\[
Y_0 = \quad \text{__________________________}
\]

\[
Y_1 = \quad \text{__________________________}
\]

\[
Y_2 = \quad \text{__________________________}
\]

\[
Y_3 = \quad \text{__________________________}
\]

Hint: the formulas for \(Y_0\) and \(Y_3\) are very simple. Remark: the best equations are not the minimal sums of products.
2. (13 points) Sideways adder: The sideways sum of a signal vector \((X_1, X_2, \ldots, X_n)\) is the number of input signals that are true; that is,

\[
S = \sum_{k=1}^{n} X_k.
\]

Since \(S\) has \(n + 1\) possible values, the sum requires a vector of \(m = \lceil \log_2(n + 1) \rceil\) bits. For \(n = 7\), the sum is represented by \(\lceil \log_2(7 + 1) \rceil = \lceil \log_2 8 \rceil = 3\) bits; that is, \(S = (S_2, S_1, S_0)\).

Using only full adders, design a circuit that calculates the sideways sum \((S_2, S_1, S_0)\) of \((X_1, X_2, \ldots, X_7)\). You may use either of the two alternative logic symbol for the full adder. (Do not try to wire the full adders inside the box above.) Hint: six full adders are more than enough. Bonus points for minimum number of gates and smallest propagation delay.
3. (20 points) Latches?
   a. A committee of logic designers could not agree on whether to use NAND gates or NOR gates to build a set-reset latch. The compromise design is shown below.

   ![Latch Diagram]

   Fill in the function table for this sequential circuit.

<table>
<thead>
<tr>
<th>X</th>
<th>Y</th>
<th>Q</th>
<th>/Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

   Explain what is wrong with this “latch”?

   b. The feedback sequential circuit shown below is intended to change state with each clock pulse; in other words, it is supposed to be a “toggle latch.”

   ![Feedback Latch Diagram]

   Explain why this sequential circuit does not work as intended. What actually happens?
4. (20 points) State machine analysis. Analyze the clocked synchronous state machine below.

![State machine diagram]

a. Draw a state diagram for this state machine.

b. Is this machine a Mealy machine or a Moore machine?

Answer (circle one): Mealy Moore

c. Fill in the transition/output table for the above state machine.

<table>
<thead>
<tr>
<th>/RESET</th>
<th>Q1 Q2</th>
<th>0</th>
<th>1</th>
<th>OUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q1<em>Q2</em></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
5. (10 points) A negative edge-triggered D flip-flop can be built from a positive edge-triggered D flip-flop and an inverter, as shown below.

![Diagram of negative edge-triggered D flip-flop](image)

The propagation delays and timing parameters for the inverter and the D flip-flop are given in the following tables.

<table>
<thead>
<tr>
<th>Inverter</th>
<th>Flip-Flop</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{\text{PLH}} )</td>
<td>( t_s )</td>
</tr>
<tr>
<td>( t_{\text{PHL}} )</td>
<td>( t_h )</td>
</tr>
</tbody>
</table>

Find the setup time \( t_s \) and the hold time \( t_h \) for this negative edge-triggered flip-flop.

Setup time \( t_s = \) _______________

Hold time \( t_h = \) _______________
6. (25 points) Variable-speed counter. The 24-bit binary counter shown below counts either at full speed or at half speed as determined by the speed-control state machine SPEED.

In half-speed mode, SPEED enables counting on every other clock, whereas in full-speed mode, the counter enable CE is always true. The speed is changed by the pushbutton input BIN; each positive pulse of BIN toggles the speed mode, from half to full or from full to half. This input is debounced, and its pulse width is a large number of clock cycles.

a. Draw the state diagram for the SPEED state machine.
b. For a state assignment of your choice, write the transition/output table.

c. For the state assignment of part b, write the transition and output equations.