Laboratory Assignment #2
Laboratory Familiarization: the Real (Analog) World
Due date: to be completed in lab from October 7–11, 2002

The following is an introduction to using the equipment in the EE 121 laboratory and to basic digital debugging techniques. **(In order to save time in lab, you should read through each section and have a basic understanding of the material before your lab time).** There are six sections:

1. Using the HP 54645D mixed signal oscilloscope
2. Using the CADET stations
3. Using the function generator
4. Digital debugging techniques
5. **Laboratory exercises**
6. Time-saving, aggravation-reducing lab tips

Each laboratory station is equipped with the following:
§ HP 54645D digital oscilloscope
§ CADET circuit prototyping station
§ HP 3312A function generator
§ Logic probes

1. Using the HP 54645D Oscilloscope

The oscilloscope you will use in the EE 121 laboratory is the Hewlett-Packard 54645D two-channel oscilloscope. It is similar in operation to the analog scopes you might have used in E-40 and other lab courses. Below is a picture of the front panel of the scope showing the individual controls of the 54645D. Note that the controls are grouped into sections: Analog Channel Inputs/Controls, Horizontal, Measurement, Trigger, Storage, and Digital Channel Inputs/Controls. We will briefly summarize the functions you will need to use in the labs. If you feel fairly comfortable with operating a scope, skip to the **Measure** section, which begins coverage of the new features of this scope.

A. Analog Channel Inputs/Controls
The keys labeled A1, and A2 control parameters for the two analog input channels. Like most of the controls on the 54645D, the channel control keys are menu-driven; that is, when you select one of them, a menu of further options appears at the bottom of the scope screen. Below the screen is a row of six keys, each of which allows you to access the menu option appearing directly above it.

Press key A1. Adjust the settings so that channel 1 is ON (that is, channel 1 is active and displayed on the screen), coupling is DC, BW limit if OFF, invert is OFF, Vernier is OFF, and Probe is set to 1. These are the settings you will usually be using for the labs.

The two Volts/Div knobs control how the signals going into channels 1 and 2 are scaled before being displayed on the screen. The volts-per-division for each displayed channel indicates how many volts each grid division along the y-axis of the scope screen represents for that channel. This number is also displayed on the upper left portion of the screen.

The two Position knobs control the ground (0 V) reference level for each channel. Note that the ground level for each displayed channel is indicated by a small ground symbol on the left side of the screen.
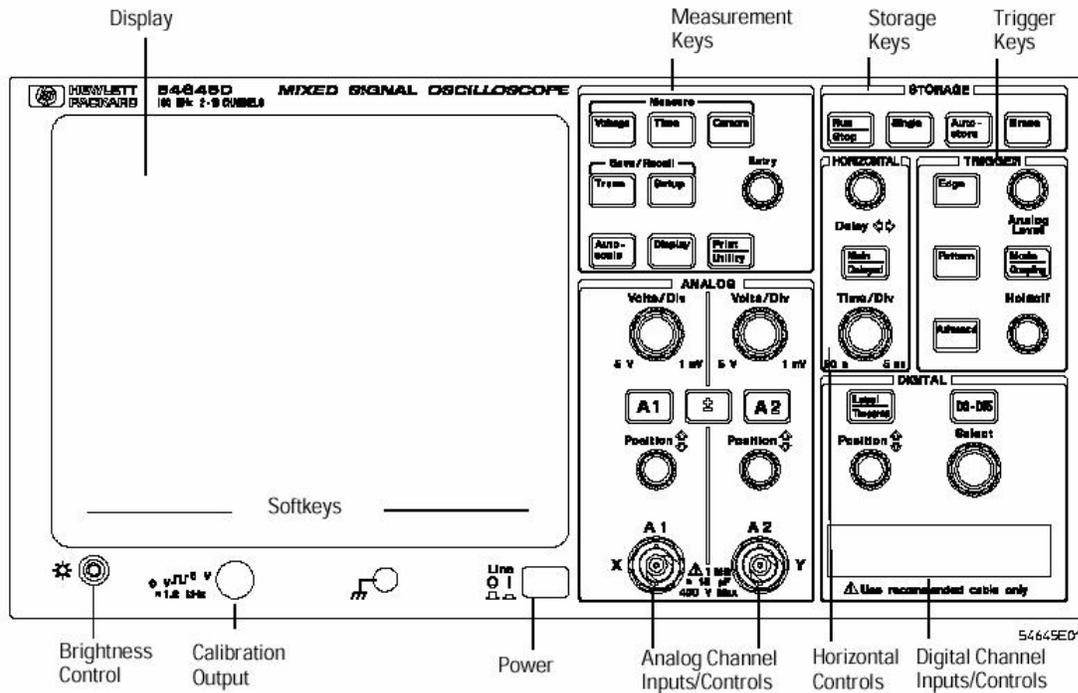
Move the ground level for channel 1. Note that as you move it, the current ground reference level relative to the center line of the scope screen appears as highlighted text on the lower left side of the screen. Also note that it is possible to adjust the ground level to a low or high enough level so that it completely disappears on the screen. Beware of this feature!

B. Horizontal
The Time/Div knob controls the time interval represented by each grid division along the x-axis of the scope screen. This time interval is common to all channels currently being displayed. It is adjustable from 5 nanoseconds to 50 seconds per division. The horizontal Delay knob is analogous to the horizontal adjustment knob on an analog scope. By adjusting it, you can move the displayed waveform either left or right on the screen. The Delay knob controls how long the scope waits after receiving a trigger event before running the actual sweep on the input signal. See below for a discussion of triggering.

C. Measurement
The 54645D can make automatic measurements of various parameters of the displayed waveforms, such as determining signal period, frequency, and peak-to-peak voltage. The results of these measurements are displayed on the screen below the waveform. These features are accessed through the Voltage and Time keys, which when selected bring up a menu of options.

Note the various measurements supported in the Voltage and Time menus. Also note that both menus have more options than can fit on one menu screen. The additional options can be accessed by selecting Next/Previous menu.

Before you select one of these options, you must specify which channel you want the measurement to be applied to. In the Voltage or Time menu, the leftmost menu item allows you to select which channel to apply the measurement to. Manual measurements on the waveform can be made using the 54645D on-screen cursors, which are brought up by pressing the Cursors key. There are two cursors each for measuring voltage and time, and their positions on the screen are adjustable using the knob below the Cursors key. In addition to measuring voltage or time corresponding to a single point on the waveform, pairs of cursors can be used to measure the voltage or time differences between two points on the waveform. As with the automatic measurement functions, the channel to which the cursor measurements are being applied must first be specified.

D. Trigger
Review of Triggering
Triggering is a subject generally not well understood. Most people take it for granted that the scope is able to properly display the input signal on the screen without the user ever having to fiddle with the triggering parameters. Until they encounter a case in which the scope fails to trigger properly, either no image or multiple images on the screen. On the whole, triggering really is not that difficult. The idea of triggering is this: the oscilloscope sees a signal whizzing by on a certain channel and needs to know when to start displaying it. The triggering circuit determines when to begin displaying the signal. The triggering circuit works by examining the signal and when this signal crosses a selected voltage threshold value in a selected direction (low-to-high or high-to-low), it triggers, telling the scope that it is time to start displaying the signal. The signal the trigger circuit examines is determined by the source setting and is usually the same signal you want to display on the oscilloscope screen. For example, if you are looking at the signal going into channel 1, then channel 1 can also be set to be the trigger source. If the trigger threshold is set to 0 volts, every time the signal crosses the 0V level, the scope will detect that a triggering event has occurred. Once a triggering event (subject to an additional constraint explained in the following paragraph) is received, the scope begins its sweep. The sweep lasts as long as necessary to cross the display on the setting indicated by the Time/Div knob. For example, if Time/Div is set to 20 ms per division with 10 grid divisions on the oscilloscope screen, a full sweep requires 10 x 20 = 200 ms. Once the sweep is complete, the scope is ready to begin another sweep as soon as it receives the next trigger event. The scope may do this over and
over again many times per second, so if the input signal is periodic, you should see a fairly stable image on the display.
A problem may arise, with a sine wave, for instance, if the scope triggered at a 0V crossing with a phase of 0 (on an upward slope) one time, and the following time triggered at a 0 V crossing with a phase of 180 (on a downward slope). This would lead to an unstable display switching between the two waveforms. Thus the trigger section not only has a level knob, but also allows the user to select if the scope triggers on an upward or downward slope, so this ambiguity does not arise.

Description of triggering controls
The 54645D has multiple triggering modes. The current mode is accessed through the trigger Mode/Coupling key. The most frequently used triggering mode is Auto Level. In this mode, the trigger threshold is limited to be between the peak voltages of the trigger source signal. This makes it fairly easy to trigger on most signals. Another mode is Normal. In this mode, a sweep is initiated only if the threshold crossing condition is met; otherwise the result of the last sweep is displayed on the screen. In Normal mode, the trigger Level knob sets the trigger threshold at a certain absolute voltage level. Another mode offered is Single, which selected by a button on the scope. In this mode, once the scope receives a trigger event, it will perform only a single sweep. Once the sweep is completed, the result of that sweep is displayed on the screen, and the scope ignores any further trigger events. The scope can be reset by pressing the Run key

located in the Storage section of the front panel. This mode is used for viewing one-time events and non-periodic signals. Exercise 3 of this lab involves operating the scope in Single sweep mode. The Analog Level knob adjusts the current trigger level. As you adjust the voltage level, its value will be displayed in inverse-video text on the lower left of the screen. The Edge key specifies whether the scope triggers on a positive or negative slope. The coupling parameter should usually be set to DC, using the Mode/Coupling menu.

If you have problems getting your signal to trigger properly, two things to check are:
1. Make sure that your trigger threshold voltage is not set at too high or too low a level.
2. Check to see if you have specified the correct trigger source. If you're using only channel and channel 2 is unconnected, make sure that you have not specified channel 2 as the trigger source. If that is the case, the scope will only trigger when the "input" to channel 2 crosses the trigger threshold. However, since channel 2 is unconnected, this event never happens.

E. Miscellaneous

The Autoscale key automatically sets up the oscilloscope to best display all current input signals. Needless to say, this can be a very useful feature. However, using Autoscale requires that the input signal have a frequency greater than 50 Hz and a duty cycle greater than 1%. Running autoscale on signals that do not satisfy these conditions can lead to unpredictable results. When you select Autoscale, the oscilloscope scales all channels that have signals applied, and it selects a time base range based on the trigger source. The trigger source selected is the highest numbered input channel that has a signal applied.

F. Digital Channels

The HP 54645D includes a logic analyzer with 16 digital input channels. The logic analyzer section will be a useful tool in the EE 121 laboratory. Obtain the HP 54645D manual, which is available in the lab, (the manual should remain in the lab) and is also available at HP website (http://www.hp.com), with keyword search, "54645D".) Read pages 1-11 to 1-12 to learn how to attach and use digital probes. Ask your TA for probe grabbers. Be sure to connect the ground lead to ground probing. Warning: Do not pull on and always avoid tension on the probe leads. They are easily damaged and very expensive. Remember to return the probe grabbers after the lab.

Refer to pages 2-25 to 2-36 of the manual. Learn how to turn digital channels on and off and to select and rearrange channels. Time cursors and measurement also work with digital channels. These features can be accessed via the Time button in the Measurement section. You can display all 16 digital channels and use any of them for triggering.

Perform the following measurements to familiarize yourself with the HP 54645D.

1. Select an analog channel using either the leftmost softkey or the Select knob (directly during the D0-D15 button).
2. Attach digital probe leads D3 and D10 and the selected analog channel to the same periodic signal, which you may generate from the CADET board's TTL function generator.
3. Display channels D3 and D10 (use the D0-D15 and Select controls) and compare with the analog signal. Notice the activity indicator for the digital channels at the top of the screen (HIGH, LOW, PULSE).
4. Press the Time button. Rotate the Select knob until D3 is indicated at the bottom left of the screen.
5. Use Freq, Period, and Duty-Cy softkeys to make measurements.
6. Explore the ability to trigger on the occurrence of a certain pattern. Press the Pattern key in the trigger group. Select channel D3. Use softkeys to select L (low level) trigger pattern for D3.
7. Repeat the previous step for channel D10. You should see the two waveforms stabilize.

8. Observe what happens when you change D10 's trigger pattern to high using the H softkey. Also observe the analog channel.

2. Using the CADET stations

The digital circuits you will design for the EE 121 labs will be built on the CADET (Complete Analog/Digital Electronics Trainer) stations. Each CADET station contains a central bread-boarding area on which to lay out your circuit, as well as various built-in circuit accessories, such as multiple power supplies, a simple function generator, and logic LED indicators. The basic layout of the CADET station is shown below. The functions labeled A through G in the picture are the ones you will most likely need to be familiar with for the labs. We will describe each one briefly.
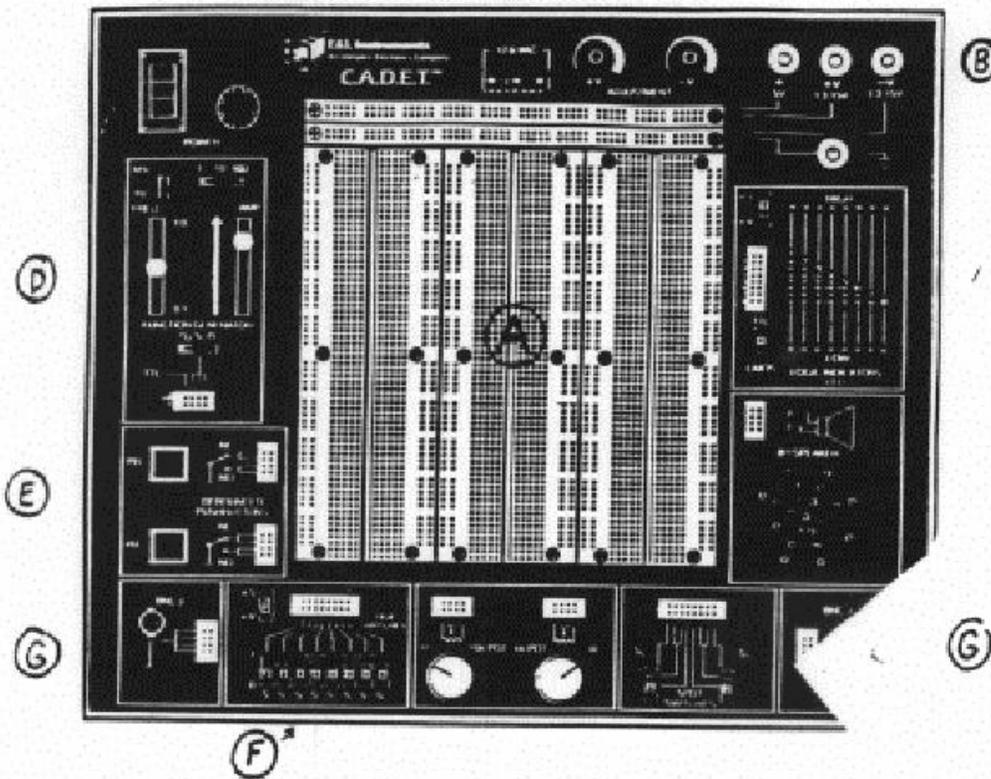

Figure2: CADET board layout

A. Breadboard Sockets

There is a large white area in the center of the CADET full of holes called "tie points" or "contact points." This is the breadboarding area. It is not connected to any circuitry beneath the surface of the trainer except at the top two strips, which are internally connected to the power supplies. This breadboarding area is where you will place your components. There are actually three separate breadboards in the center of the trainer. Each breadboard is arranged as follows: horizontal rows of five holes are the same point electrically. No row of tie points is connected to any other row, however. Vertical columns of 25 tie points, above and below the center mounting screw, are the same points electrically. Note that the vertical columns above and below the center mounting screw are not connected to each other; wiring mistakes have often been made because students have assumed they were connected.

B. Power Supply

At the top of the breadboard area are two horizontal connector strips of breadboarding material. To their right are lines printed on the surface of the trainer indicating how they are connected to the various power supplies. Each entire row is connected to a separate power supply. The bottom row is connected to ground. The CADET features three power supplies: a fixed +5 V supply, a variable positive supply (+V), and a variable negative supply (-V). At the top of the trainer above the power connector strips are two voltage adjustment knobs for setting +V and -V. The positive voltage (+V) can be adjusted from roughly +1.3 V to +15 V and -V from -1:3V to -15 V. If necessary, power can also be taken directly from the read, blue, yellow, and black binding posts on the top of the trainer in addition to the power connector strip.

C. Logic Indicators

On the right side of the trainer are eight LED logic indicators. These LEDs will often be used indicate the outputs of the circuits you build. They are also useful for debugging purposes. A small connector block allows these LEDs to be connected to the rest of the circuit being constructed. There are eight red LEDs at the top of this section, and eight green LEDs at the bottom. The red LEDs indicate a high or "1" logic level. The green LEDs indicate a low or "0" logic level. The indicators work in pairs shown by the numbering from one to eight. Each pair has two tie points on the small connector block to the left. It does not matter which of the two tie points you use. To the left of the LEDs are two switches marked "+5/+V" and "TTL/CMOS". For interfacing the LEDs to digital circuits, the +5/+V switch should be set to +5 and the TTL/CMOS switch should be set to TTL. This sets the threshold voltages for the indicators to be compatible with TTL-level inputs: if the input connected to a pair of LEDs is at a voltage of 2.2 V or higher, the red indicator will light, if the input voltage is 0.8 V or less, the green indicator will light, otherwise, neither LED will light. Setting the +5V/+V switch to +V allows you to vary the threshold voltage for the indicators according to the current value of the CADET board's adjustable +V power supply.

D. Function Generator

On the left side of the trainer is the function generator, which will provide the clock signal needed for most of the experiments. The function generator can produce square, sine, and triangle waves of variable frequency and amplitude. It can also produce a TTL-compatible square wave suitable for use with digital circuitry. We will describe only this last feature of the function generator, since it is the only one you will normally need to use for your experiments. The leftmost two tie points on the function generator connector block provide access to the TTL output. The speed or frequency of the TTL output square wave is adjusted by three other controls. One control is the frequency slide adjustment on the left, which ranges from 0.1 at the bottom to 1.0 at the top. Another control is the decade range selection switch at the top right side of this section. It has positions labeled 1, 10, and 100. The last control is at the top left part of this section, and is a two position switch labeled "KHz" and "Hz". The frequency of your waveform is the number of Hertz or Kilohertz (as indicated by the switch at the top left) found by multiplying the frequency slide adjustment by the decade range selection switch. For example, if the top left switch is in the "KHz" position, the sliding frequency adjustment is at the bottom (0.1), and the decade range selector is in the middle (x10) position, then the output is 0:1 x 10 KHz, or 1KHz. The lowest frequency available is 0.1 Hz, and the highest is 100 KHz. Note that the TTL output is not affected by the setting of the switch with the sine, triangular, and square wave symbols, nor by the amplitude sliding control (marked "AMP"). These are used by the other features of the function generator.

E. Debounced Pushbuttons

There are two pushbuttons on the left side of the trainer. These are labeled "debounced" pushbuttons because they consist of the physical mechanical switch with additional circuitry to eliminate the multiple

switch closures normally found when operating mechanical switches. That is, most switch contacts actually "bounce" very briefly when closed. Even though this period of time is brief (a few milliseconds), digital circuitry is fast enough to falsely interpret this as several closures rather than just one. Thus the need to electronically "debounce" these switches. Each switch has eight tie points of two different types. Four of the points are marked by the letters "NC" meaning "normally closed." These points are connected to ground when that pushbutton is in its unpressed position and become open (disconnected) when the button is pressed. Four of these points are marked by the letters "NO" meaning "normally open" (the exact opposite of normally closed). The small switch diagram printed on the trainer helps illustrate this. To wire the pushbutton as an "active-low" switch suitable for interfacing with digital circuitry. When the button is not pressed, the switch provides a digital high close to +5 V (there is a very small voltage drop across the pull-up resistor). When the button is pressed, the switch output is a digital low (ground). Note that we can't bypass the pull-up resistor and connect the switch directly to +5 V; doing so would cause you to short power and ground when the switch is pressed and lead to a blown fuse!

F. Logic Switches
In the lower left part of the trainer are eight sliding logic switches. These switches are not debounced. Each has two tie points on the connector block above the switches. When a logic switch is in its down position, it places its tie point on the connector block at logic \0" or ground. When a logic switch is in the up position, it places its tie point at logic "1." Just exactly what voltage logic 1 is depends on several factors. In the upper left corner of this area is a switch labeled "+5/+V" If this is in the +5 position, then a high or logic 1 for the switches is +5 V. If the voltage selection switch is in the +V position, then a high or logic 1 will be the voltage of the CADET board's +V adjustable power supply, which in turn depends on the settings of the +V adjustment knob at the top of the CADET board. For your experiments, you will usually use the switches as inputs to your digital circuitry. When this is the case, always make sure that the switch is set in the +5 position.

G. BNC Connectors
At the bottom left and right corners of the trainer are BNC connectors. These connectors allow you to interface the CADET with the oscilloscope, function generator, and other test equipment without using clip leads. Attach a wire from any one of the eight tie points for the BNC connector to the location on the breadboard you wish to connect your test instrument to.

3. Using the HP3312A Function Generator
The operation of the HP3312A function generator is similar to that of the function generator onboard the CADET station. The 3312A is capable of generating triangle, sine, or square waves. The frequency of the output is variable from approximately 0.l Hz to 10 MHz. The frequency of the output is adjustable using the row of frequency Range pushbuttons at the top of the panel, and the frequency adjustment knob on the left-hand side. The Amplitude adjustment knob is actually two control knobs. The setting of the bottom knob specifies the general range of the output amplitude and the top knob is for fine adjustment of the amplitude level. The offset knob varies the DC offset, or center voltage, of the output. (Make sure that the blue calibration button on the knob is in the "out" position.) For example, to produce a 0-5 V square wave, adjust the amplitude of the output so that it is approximately 5V peak-to-peak. Then adjust the DC offset of the
output so that it is centered about 2.5 V. Settings for Normal Operation The output of the function generator is taken from the BNC jack labeled "Vp-p" directly under the amplitude adjustment knob. You will not need to use any of the other knobs, buttons, or features of the 3312A for the labs. However, make sure that the six buttons on the right side of the front panel, under the "Modulation" section, are all in the "out"

(deselected) position. Also make sure that the Trigger Phase knob is turned completely counterclockwise to the "Free Run" setting, and that the blue button on the Sym knob is in the "in" (pressed) position. The output of the HP function generator will often be used to provide a clock or other input for your digital circuitry. A common problem is not using the oscilloscope to first check that the function generator output has been properly set to vary from approximately 0-5 V before attaching it to your circuit.

4. Digital Debugging Techniques

Debugging digital circuits is a whole lot of fun. You might have heard it otherwise, but debugging is like how a detective works, finding the causes of undesirable results. Moreover, it is an integral part of the labs and final project, and we expect you to develop good debugging skills and be able to recognize the causes of various problems as the labs progress. A considerable amount of the time that you will spend in the lab will be devoted to debugging the circuit that you've built on the CADET board, even though the underlying design from your prelab may be correct. The following is a list of things to check when your circuit is not functioning as expected.

§ Basic philosophy: It's usually best to **work backwards when debugging your circuit**.
§ **Identify the problem** (e.g., bad output bit), and begin your debugging at the immediate source of the problem.
§ **First check the wiring** for the IC that produces that output. If you discover that one or more of the inputs going into that chip are incorrect, then check the chip(s) which produce these incorrect inputs, and so on.
§ **Don't be afraid to use the oscilloscope.** The debugging tools you will likely use most are the logic probe and multi-meter. Occasionally, though, you may find yourself in a situation where these tools don't tell you enough about the problem. You will find the oscilloscope to be a valuable debugging tool (especially in the later labs and project), since it is capable of conveying much more information than the other tools, such as signal frequency, peak-to- peak voltage, and pulse width.
§ **Use good wiring practices.** Always color code your connections (generally use red for +5 V and black for ground). Make sure all your wires fit securely in the CADET board holes. Avoid making your wires too long, long wires tend to get inadvertently pulled out of their holes while you're working on other parts
of your circuit. At the same time, don't cut your wires too short, since if you later discover that you've made a wiring mistake, it's nice be able to fix the problem by just rerouting the original wire. **And avoid having wires cross over ICs; this eliminates the hassle of having to remove wires whenever you need to change an IC.**
§ Connecting power and ground: The +V, - V, and +5 V connections are power supplies.
§ Never connect power supplies to each other, or to ground.
§ **Things to consider when an IC is not producing the correct output**:
    1. Are power (+5 V) and ground correctly applied to the chip?
    2. Is the chip plugged in backwards? (There should be a notch or dot at one end of the chip signifying pin 1 on the chip.)
    3. Are any of the chips hot to the touch, or worse yet, do you detect the faint smell of something burning? In this case the first thing to do is turn off power to the CADET board then check the previous two possibilities.
    4. Make sure all external inputs to the circuit are set to the correct voltage levels. If you're providing a clock to your circuit using the output of the HP function generator, make sure beforehand that you've correctly set it to produce a 0-5 V square wave. Or if you're using the logic switches on the CADET board as inputs, make sure they're set to +5 V and not to +V.
    5. Are all the input control lines of the IC connected properly?

6. Do the outputs follow the inputs logically? Check the inputs and outputs via a logic probe or the scope.

§ An IC may produce an indeterminate (i.e., neither high or low) output. In this case, a few other possible causes for this behavior are:

1. Many ICs have output enable inputs (e.g., 74x244, 74x245). If the output enable is not asserted, then the output of the IC with be "tri-stated" (you'll learn about this later in the course). The end result will be that the output of the IC will appear as being indeterminate.

2. The output of the IC may be connected to outputs of other ICs. This leads to the phenomenon known as "fighting," where one output tries to assert a logic low the same time the other output is trying to assert a logic high. Never connect different active outputs together. Disconnect all connections from the output pin of the IC in question so that it is no longer connected to anything. If the output pin now reads a determinate (logic high or low) voltage, then this may very well have been the problem. Restore the connections to the output pin one by one until the problem reappears in order to trace the source of the problem.

§ An occasional problem in the lab is just plain having a bad chip. Make sure you've gone through all the above possibilities, though, before trying a new chip. And if you know you have a bad chip, **please give it to the TA.**

LAB EXERCISES

1. Measure the propagation delay and transition times for the 74LS04 inverter gate. (See Page 329 for SSI pinouts, and Page 13 for general pin numbering on DIPS. All the pinouts are included in the manufacturer's data sheet. The power pins of typical TTL and CMOS SSI/MSI devices in n-pin DIP packages are pin n for VCC and pin n/2 for GROUND, i.e., the upper-right and lower left corners for VCC and GROUND, respectively.)

a) The 74LS04 is a SSI (Small Scale Integration) IC containing six separate inverter gates. The pinout for the 74LS04 can be found in Page 13 of DDPP3. Wire up five of the six inverters into a chain where the output of one inverter drives the input of another inverter:
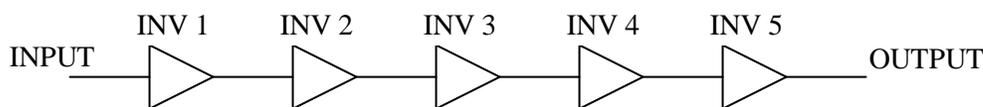
b) Set the HP function generator to produce a 0-5 V 200 KHz square wave. Display the output of the function generator on the oscilloscope and verify that the function generator has been set to the correct voltage and frequency using the automatic measurement capabilities of the scope.

c) Before connecting the function generator output to the 74LS04, make sure you have properly applied +5 V and ground to the chip. Once you have verified that the function generator is producing the correct signal, use the function generator output as the input to the first inverter on the 74LS04 IC.

d) Now use the scope to display the input of the first inverter on channel 1 and the corresponding output on channel 2. Set the Volts/Div for both channels to provide best display results.

e) Measure $t_{p,lh}$ for the first inverter (the propagation delay from when the input goes low to when the output goes high). You'll need to use the Time/Div and Delay knobs to zoom in on the transition region of

the waveform in order to be able to make an accurate measurement. Use the scope cursors to make your measurement. You should measure between the 50% point of the high to low transition of the input to the 50% point of the low to high transition of the output.

f) Now measure $t_{p,lh}$ for the first three inverters by displaying both the input to the first inverter and the output of the third inverter on the oscilloscope. Measure the time from when the input goes low to when the output (of the 3rd inverter) goes high. Then do the same for the first 5 inverters.

g) Plot the three values of $t_{p,lh}$ versus the number of inverters (1, 3 and 5) and comment on the results.

h) Now we're going to measure the transition times of the 74LS04 inverter, so display the output of the first inverter on the oscilloscope. The rise time, t_r, is the time associated with the transition of the output from low to high, and the fall time, t_f, is the time associated with the transition of the output from high to low.

i) Zoom in on the region of the output signal where the voltage is rising from low to high, and then measure t_r using the time cursors. The left cursor should be placed at the 30% point of the transition and the right cursor should be placed at the 70% point of the transition, as shown on page 114 of the textbook.

j) Now zoom in on the region of the output signal where the voltage is falling from high to low and measure the fall time, t_f.

k) Typical values for the transition times are 9 ns for the fall time and 21 ns for the rise time. How do your measurements compare to these typical values?

l) Recall that a ring oscillator is constructed from an odd number loop of inverters. For example, connecting the input to the output of the circuit in Section 1.a forms a ring oscillator. Continue adding pairs of inverters into the loop. Continue until you have 9 inverters. Describe and compare the output of the ring oscillator as you change the number of stages. **Show one of the outputs on the oscilloscope to your TA.**

2. Display the effects of switch bouncing. This exercise demonstrates a possible use of the single-sweep trigger capability of the scope to capture and store a nonperiodic, one-time event.
a) Set the triggering parameters of the scope to:
  i. Make sure that channel 1 is your trigger source.
  ii. In the Edge key menu, set the scope to trigger on a positive slope.
  iii. Set the trigger coupling to DC.
  iv. Set the trigger level to around 2 V using the trigger Level knob.
  v. Set the Volts/Div for channel 1 to 2V per division.
  vi. Set the Time/Div to 500 _s per division.
b) Connect channel 1 of the scope to one of the eight logic switches in the lower left corner of the CADET board. (Make sure the CADET power is on.) Set the switch in the "0" or down position.
c) Press the Single key on the scope. Notice that the scope will not trigger because it has not received a trigger event yet.
d) Move the switch to the "1" or up position. As soon as the input into channel 1 crosses the trigger level, the scope will trigger only once. The waveform that is displayed on the scope is a "snapshot" of what the switch outputs when you move it from the "0" to "1" position.
e) Notice that the transition from a digital high to low is by no means a smooth one. In fact you should see multiple transitions from high to low and vice versa before the switch output finally settles at +5 V. This is known as switch bounce and can potentially be quite troublesome for certain digital circuitry, since what

should be intended as one transition can be interpreted as many transitions instead. A variety of different schemes and sub-circuits exist to eliminate switch bounce, some of which may be employed in the later labs for this course.

f) Try this experiment several times (you might want to change the Time/Div setting in order to better view the switch bounce). Measure the bounce interval (the time it takes for the switch to finally settle down to a stable value) for several tests. Is this interval fairly constant over several tests?

3. Illustrate a static hazard. Construct an XOR gate circuit based on the schematic from Lab 1 using three TTL parts: 7404 (Quad INV), 7408 (Quad AND), and 7432 (Quad OR). Use the +5V and GND connections on the CADET board as power and ground for the logic gates. Create a 10 kHz, 0 to 5 V square wave with the function generator to use as an input for the circuit. To see a hazard, the input should switch in such a way that the output theoretically remains the same. The clock, therefore, must feed both circuit inputs. Set the oscilloscope to trigger on the positive edge of the output. You might need to adjust the timescale. This will show the effect of a static-0 hazard. **Demo the results for your TA.**

4. Sometimes great literature can be a little inaccessible. This is particularly true when it's hiding inside of an FPGA. Your TA will give you an FPGA "bit" file and demonstrate during the lab session how you can use it to program the FPGA on the XSA-100 boards we'll use all quarter. Once it's programmed, the FPGA will transmit a short quote in ASCII from a famous work of literature. Your job is to use the logic analyzer to find out what the quote is and inform your TA. Each group will have a different quote, so eavesdropping on your neighbors won't help.

   The American Standard Code for Information Interchange (ASCII) is a way of representing letters and other common symbols as eight-bit binary numbers. Computers and other digital systems often use it to store and transmit text files. Each letter or other symbol has a unique eight-bit code. For example, the code for the letter 'A' is 01000001, or 41 in hex. The code for the letter 'a' is 01100001, or 61 in hex. Here's a complete listing.

```
Dec Hx Oct Char                     Dec Hx Oct Char   Dec Hx Oct Char   Dec Hx Oct Char
---------------                     ---------------   ---------------   ---------------
  0  0 000 NUL (null)                32 20 040 SPACE   64 40 100 @        96 60 140 `
  1  1 001 SOH (start of heading)    33 21 041 !       65 41 101 A        97 61 141 a
  2  2 002 STX (start of text)       34 22 042 "       66 42 102 B        98 62 142 b
  3  3 003 ETX (end of text)         35 23 043 #       67 43 103 C        99 63 143 c
  4  4 004 EOT (end of transmission) 36 24 044 $       68 44 104 D       100 64 144 d
  5  5 005 ENQ (enquiry)             37 25 045 %       69 45 105 E       101 65 145 e
  6  6 006 ACK (acknowledge)         38 26 046 &       70 46 106 F       102 66 146 f
  7  7 007 BEL (bell)                39 27 047 '       71 47 107 G       103 67 147 g
  8  8 010 BS  (backspace)           40 28 050 (       72 48 110 H       104 68 150 h
  9  9 011 TAB (horizontal tab)      41 29 051 )       73 49 111 I       105 69 151 i
 10  A 012 LF  (NL line feed, new line) 42 2A 052 *    74 4A 112 J       106 6A 152 j
 11  B 013 VT  (vertical tab)        43 2B 053 +       75 4B 113 K       107 6B 153 k
 12  C 014 FF  (NP form feed, new page) 44 2C 054 ,    76 4C 114 L       108 6C 154 l
 13  D 015 CR  (carriage return)     45 2D 055 -       77 4D 115 M       109 6D 155 m
 14  E 016 SO  (shift out)           46 2E 056 .       78 4E 116 N       110 6E 156 n
 15  F 017 SI  (shift in)            47 2F 057 /       79 4F 117 O       111 6F 157 o
 16 10 020 DLE (data link escape)    48 30 060 0       80 50 120 P       112 70 160 p
 17 11 021 DC1 (device control 1)    49 31 061 1       81 51 121 Q       113 71 161 q
 18 12 022 DC2 (device control 2)    50 32 062 2       82 52 122 R       114 72 162 r
 19 13 023 DC3 (device control 3)    51 33 063 3       83 53 123 S       115 73 163 s
 20 14 024 DC4 (device control 4)    52 34 064 4       84 54 124 T       116 74 164 t
 21 15 025 NAK (negative acknowledge) 53 35 065 5      85 55 125 U       117 75 165 u
 22 16 026 SYN (synchronous idle)    54 36 066 6       86 56 126 V       118 76 166 v
 23 17 027 ETB (end of trans. block) 55 37 067 7       87 57 127 W       119 77 167 w
 24 18 030 CAN (cancel)              56 38 070 8       88 58 130 X       120 78 170 x
 25 19 031 EM  (end of medium)       57 39 071 9       89 59 131 Y       121 79 171 y
 26 1A 032 SUB (substitute)          58 3A 072 :       90 5A 132 Z       122 7A 172 z
 27 1B 033 ESC (escape)              59 3B 073 ;       91 5B 133 [       123 7B 173 {
```

```
28 1C 034 FS  (file separator)        60 3C 074 <    92 5C 134 \    124 7C 174 |
29 1D 035 GS  (group separator)       61 3D 075 =    93 5D 135 ]    125 7D 175 }
30 1E 036 RS  (record separator)      62 3E 076 >    94 5E 136 ^    126 7E 176 ~
31 1F 037 US  (unit separator)        63 3F 077 ?    95 5F 137 _    127 7F 177 DEL
```

The FPGA has one input, a clock signal on pin 88; and one output, the data on pin 41. The FPGA shifts out each eight-bit ASCII character one bit at a time, from the most significant bit to the least significant bit. The data output changes each time the clock signal changes from low to high. The FPGA repeatedly transmits 32 consecutive bytes, some of which are legal ASCII characters, and the rest of which are FF, or all 1's.

For example, if the quotation were "hi" you would see the following waveform.
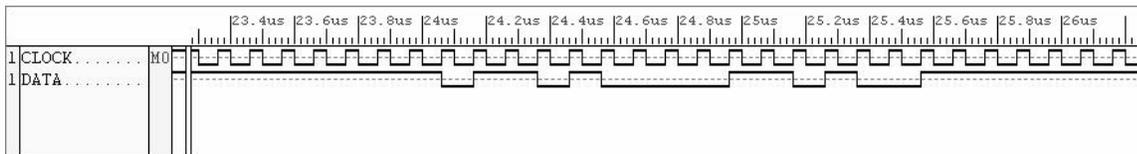
At first, the DATA line is high since it is transmitting FF repeatedly. Then it transmits 0, 1, 1, 0, 1, 0, 0, 0, or 68 (hex), which we look up in the ASCII chart and find to correspond to "h". Then it transmits 0, 1, 1, 0, 1, 0, 0, 1, or 69 (hex), which corresponds to "i". Then DATA goes high as it returns to transmitting all 1's. Since all the ASCII characters of interest have a "0" in the most significant bit, we can easily distinguish the start of the first ASCII character from the FF symbols.

Time-Saving, Aggravation-Reducing Lab Tips

a) Most of the chips used in the labs are dual-inline packages (DIPs). Pin 1 is usually marked with a dimple or a notch in the package. The pin numbers increase in a counterclockwise direction. (Warning: signal connectors use several other conventions.)

b) On standard logic parts, VCC and ground are assigned to opposite corners of the chip. Ground is the last pin in the first row, and Vcc is the last pin in the second row. This is usually the case, although there may be some exceptions. When you are wiring your designs, don't forget to connect Vcc and ground. In fact, make it the first thing you do!

c) When you wire your circuits on the proto-board, try to keep the wiring short, straight, and simple. There are many reasons for this:

     i. You will make fewer wiring errors.
     ii. You will retain your sanity when debugging.
     iii. Your TA will like you better.
     iv. Rats will not nest in it.

d) Often, when you use a brand new chip, the pins will not be at right angles to the seating plane. This makes it difficult to insert the chip into the CADET board. To bend the pins inward, it's best to bend a whole row at a time by laying the chip on its side against the lab bench and gently pushing down with a rotating motion.

e) Chips are typically labeled on the top with three distinct codes. The first, and most important, is the part number. The second code is the date of manufacture, and the third is a lot code. Sometimes the date code and the lot code are combined, so you might only see two distinct codes on the chip. A chip with a date code 9408 was made in the 8th week of 1994.