EE133 - Lab 5
IF Amplification and Filtering

1 Introduction

For the rest of the quarter, we will not hand out explicit prelabs and labs; we will rather give you a circuit to build and some suggested steps to make it work. You are free to simulate and test the circuits as you please, and we will only make sure you have done what's absolutely necessary (i.e. that you have a working circuit). However, be forewarned that you should still be thorough in your descriptions in your lab notebook. This work, while sometimes tedious, will prove invaluable as you try to remember details of your work as you debug or write your final report.

One of the major problems with your receiver is that the signal it receives must ultimately be strong enough for the PLL to lock onto. To get the range we need, we're going to need some amplification in the signal path. We could do this at the input, but as you can see from lab 1, designing an amplifier at 24MHz is not the most straightforward of tasks.

In the early days of radio, Armstrong had this same problem getting gain at high frequencies and therefore invented the "super-heterodyned" receiver. This receiver mixes the high-frequency input signal, say 24.3MHz, down to a lower 'intermediate frequency' (IF) (300kHz) and then amplifies this lower frequency signal where high gain can be easily obtained. Hopefully, this system sounds familiar, since you have spent the first part of the quarter building it.

Our next task is to build an IF Amplifier to work at 300kHz with a large gain (around 5,000 or 74dB). We will use the National LM7171 Op Amp for this building block.

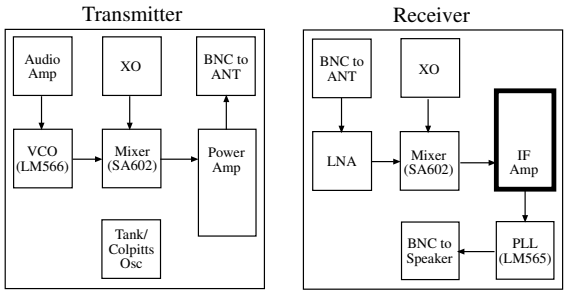

Figure 1: How the IF amp and filter fits into your circuit

As you can see from Figure 1, the IF Amp will be taking the output of your multiplier and amplifying it so that your PLL can still track your input signal.

While we are at it, we'll also be putting in a narrow band-pass filter. Why are we bothering? Imagine if your neighbor was transmitting a large signal at 24.5MHz while you were working at 24.3MHz. If this signal got into your system and was mixed down to 500kHz, it could potentially prevent your PLL from tracking the correct signal. We will therefore build a bandpass filter to make sure these unwanted signals don't interfere with our receiver.

Now you might be saying to yourself, "If a gain of 5,000 is great, then a gain of 1,000,000 is even better!" And you would be partially correct. However, if you aren't careful, Murphy will smite you with one of

two problems. The first is that signals that are already appropriately sized for the PLL can be amplified by excessive gain into distorted signals. The second problem is the gain-bandwidth of your op-amps – if you try to increase the gain too much, you will see undesired and premature rolloff in the magnitude response. As it is, we will be pushing these op-amps right up to their gain-bandwidth limitations in this lab. Alternatively, if you add more amplifiers into the chain, each component adds a certain amount of noise to your signal, degrading your signal to noise ratio until its unintelligble by your PLL.

Modern radios usually solve the first problem by creating what is called an Automatic Gain Control (AGC) circuit. This circuit essentially samples the average voltage of your output and then uses that sample to control a small circuit that can bypass the amplification. Although many books have sample AGC circuits, we will not be requiring them for our radios.

The second is a more complex problem to solve. It turns out that if you perform an analysis of the relationship between noise and gain, you want to have a modest gain up front with a circuit that adds very little noise to the entire circuit. This is why Low Noise Amplifier (LNA) design is such a complex issue. We will be revisiting this issue next week, along with the power amplifier.

2 Designing your IF Amplifier

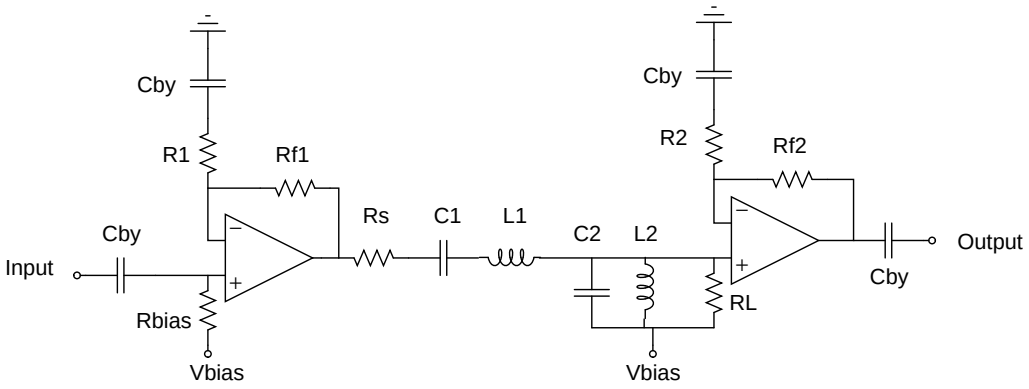

Figure 2: IF Amplification and Filtering

Your task for the week is to design and build the circuit shown in Figure 2. Notice that the incoming signal is ac coupled, amplified by the non-inverting amplifier, band-pass filtered by the L_1, C_1, L_2, C_2 combination, and finally amplified again by the second op-amp. We suggest the following stepwise procedure for realizing this filter/amplifer:

1. **Designing the Passive Filter**

   - **Cooking it up:** Use the *Filter Cookbook* to design a 4-pole Butterworth Filter (a.k.a. maximally flat). Begin with a low-pass filter prototype, then convert it to a bandpass filter (Hint: The low-pass prototype is NOT going to be N=4). We would like a center frequency of 300kHz, a bandwidth of 100kHz, and a rolloff of 40dB to either side. Be sure you understand how these constraints impact the design parameters in the *Cookbook* (i.e. Δ).
   - **Topologically Speaking:** Compare the topology we have given you in Figure 2 to the two possiblities in the *Cookbook*. Given the way we classically model op-amps, why did we choose the topology we did? Note that each topology is symmetric, so you can reverse the order of the LC chains in either topology and still have a valid filter (which is what we have done).

- **Real World Values:** In order to achieve a practical circuit (i.e. to get values of L and C which are actually available on this planet), you may need to relax (i.e. tweak) the bandwidth requirement. This is acceptable and, in fact, expected – but you have to be sure you tweak it in the right direction. Which way did you tweak it, and how much?

Element Values for Maximally Flat Low-Pass Filter Prototype						
N	g1	g2	g3	g4	g5	g6
1	2.0000	1.0000				
2	1.4142	1.4142	1.0000			
3	1.0000	2.0000	1.0000	1.0000		
4	0.7654	1.8478	1.8478	0.7654	1.0000	
5	0.6180	1.6180	2.0000	1.6180	0.6180	1.0000

Table 1: ($g_o = 1$, $w_c = 1$ N=1 to 5)

- **Characteristic Impedance:** Although it may be tempting to pick a characteristic impedance of 50Ω, this can put a strain on the opamps, which have trouble driving low impedances. We recommend you use a characteristic impedance in the range of 400Ω to 600Ω to keep the op amps happy, and to keep the component values reasonable. Unfortunately, this also makes measuring the characteristics of the IF stage a little more difficult.
- **Bypass Caps:** Since this stage is meant to handle signals around 300kHz, the bypass caps should present a small impedance around that frequency while still operating as capacitors at that freqeuncy. Therefore all the bypass caps should be in the range of .1uF or so.
- **DC gain and Rbias:** Notice that due to the bypass caps in the feedback loops we've gotten rid of the DC gain in these amplifiers. This is to get rid of amplification of the offset caused by nonzero bias currents at the inputs. Particularly at the input of the first opamp, we want Rbias to be large compared to the output impedance of the previous stage ($1.5k\Omega$ from the multiplier), so this needs to be on the order of $10k\Omega$ or so. But to get a gain of 100 out of the amplifier, R1 needs to be relatively small, on the order of $1k\Omega$ or so. This puts a mismatch at the inputs of the opamps and could cause problems if that mismatch is amplified at the output. We get rid of this problem by getting rid of the DC gain with the bypass cap to ground.
- **Frequency Response:** We recommend that you simulate the frequency response of your filter using either MATLAB or HSPICE. It might be a good idea to do this with standard components. (see http://www.stanford.edu/class/ee133/parts.html) for standard component values.

2. **Building the Passive Filter**

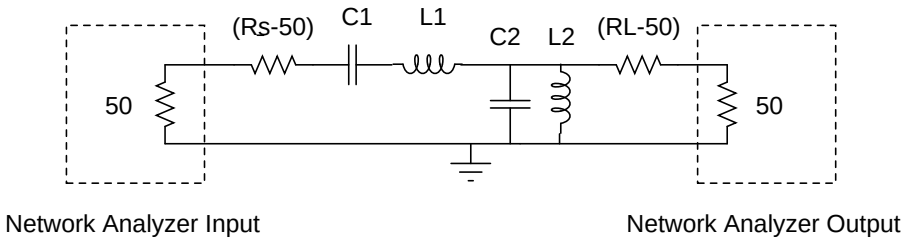

Figure 3: Building your IF Filter

- **Soldering Tips:** Solder up the filter you designed on your receive board (refer to the roadmap in Figure 1 for the proper location). Also, be sure when laying out the circuit to keep in mind that the final incarnation will consist of 1 IC (containing the two op-amps), several resistors for

setting the gain, and all the L's and C's in the filter. As you can see in Figure 3, you will need to account for the 50Ω impedance of the network analyzer input and output, which will affect the characteristic impedance of your circuit when you measure your circuit. If you designed for a 510Ω characteristic impedance, for instance, you you will want to first solder 470Ω (closest value to $510 - 50 = 460\Omega$) resistors where the 510Ω resistors will ultimately go. Also, notice that eventually you will want to be using your 4.5V rail as 'ground' for the filter elements.

- **Network Analyzer:** Now, ask your TA how to use the network analyzer (not the 8712E) to characterize the frequency response of your filter. Be sure to record this plot in your lab notebook as well as the loss caused by the insertion of your filter.
- **Impedance Matching:** Since the network analyzer already has an internal source and load impedance of 50Ω, you should add about 460Ω (470Ω is a standard value) in series with the analyzer input and output ports. This will allow you to characterize your filter with (roughly) the correct characteristic impedances.
- **DC biasing:** Be sure not to hook up any power to your circuit at this point, and also be sure that the BNC connectors you use to interface with the network analyzer are grounded to your 4.5V rail (since that's where the filter elements should be grounded).

3. **Designing the First Gain Stage**

- **The Op-Amp:** Once your passive filter is working properly, it's time to add the first gain stage. Look at the data sheet for the op amp you have chosen and design a non-inverting stage with a gain of near 100. How close does this put you to the gain-bandwidth product of this amplifier? How close to this limit do we typically like to operate? Note that you not get as much gain as you'd like out of this stage, due to the opamp's inability to drive the load. The second stage should be able to provide enough gain to compensate.

4. **Building the First Gain Stage**

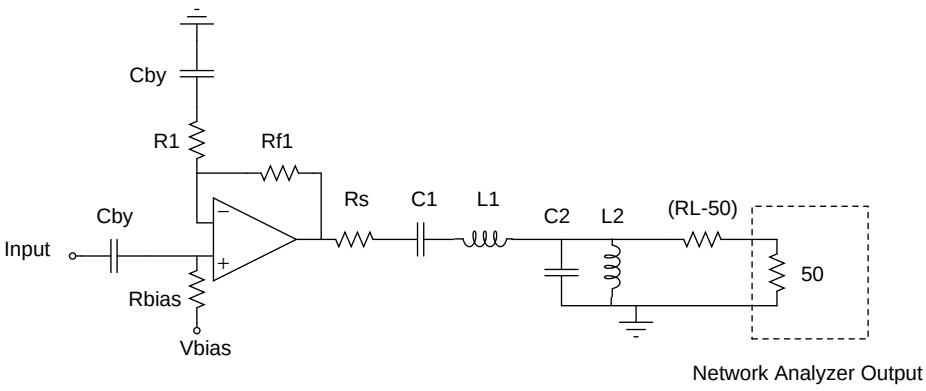

Figure 4: Adding your first stage behind the filter

- **Soldering Tips:** Solder up the op-amp you designed in the portion of the board you reserved when building the filter.
- **Impedance Matching:** You will now need to add the first of the impedance-matching resistors (R_s) at this time (That is, remove the 470Ω (or equivalent) resistor at the input to your filter and replace it with 510Ω (or equivalent)), but you do not need to change the resistor R_L (the remaining 50Ω of the characteristic impedance is provided by the test equipment.)
- **DC Biasing:** Since you will be operating the op-amps with $\pm 4.5V$ rails, you will use your $4.5V$ reference as 'ground'. This means all signals coming into and out of the IF amp will need to be re-biased at $4.5V$. For this reason, be sure to use a coupling cap and bias resistor at the input of

the op-amp (See Figure 4) as well as a BFC at the output of the filter (to protect test equipment from seeing the $4.5V$ bias). The bias resistor should be large compared to the $1.5k\Omega$ (the output impedance of the multiplier), but it shouldn't be so large that it causes a large input offset voltage (look at the spec on input bias current and use Ohm's law to figure out how much offset will be caused by the resistor you choose - notice that we are purposefully mismatching impedances here. Do you see why?). Once you have inserted the coupling caps to isolate the $4.5V$ bias in your circuit from the external connections, you'll need to be sure all the BNC connectors that provide those connections are referenced to real ground (*not* $4.5V$).

- **Signal Size:** Note that your IF amp is designed to amplify very small signals. In fact, with a gain of 5,000, the only way to prevent it from railing is to use signals on the order of microvolts. In addition, we want to see how it will respond to signals from a decade below 300kHz to a decade above it. Can you see how these requirements affect which lab equipment we can use?
- **Characterization:** Using the HP 8904A low frequency function generator in conjunction with the oscilloscope, test the frequency response (gain and bandwidth) of your circuit. Does it match your design? If not, do you have an idea as to why? Think about the load at the output of the op-amp.

5. **Designing the Second Gain Stage**

- **Rinse and Repeat:** Once the first stage of gain is in place, add the second by designing the second non-inverting amplifier with a gain of 100. This second stage should be adjustable, so you can use a potentiometer to realize the feedback resistance.

6. **Building the Second Gain Stage**

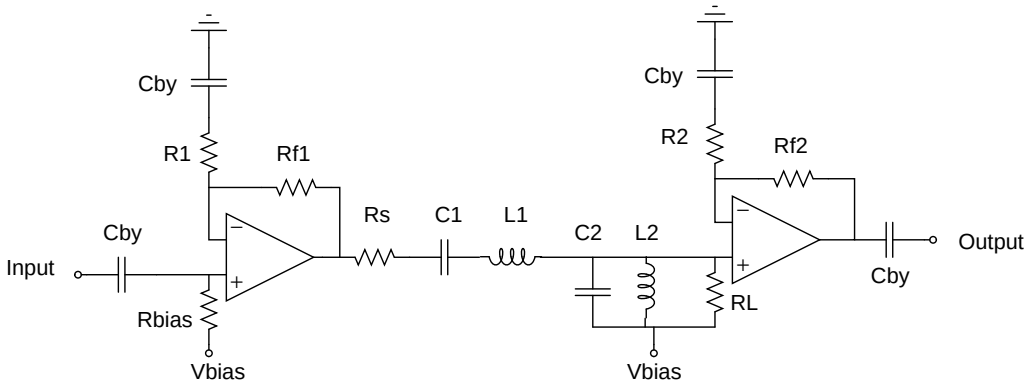

Figure 5: Adding your second stage on after the filter

- **Soldering Tips:** When soldering the second op-amp on your op-amp chip, note that you will now need to add the correct R_l to the output of the passive filter. However, you can remove the BFC that you used in the previous section. Also, you should implement R_{f2} with a potentiometer so that you can tune the gain as necessary. Please refer to Figure 5 for further clarification.
- **Characterization:** Use the 8904A function generator to examine the gain in your pass band, as well as the lower-side roll-off. To examine the upper-side roll-off, use the 8647A (higher frequency). What is your overall gain and bandwidth? (Be sure to measure the actual voltage at the input and output using the active probe).
- **Measuring the Minimum Detectable Signal of your Receiver:** We now introduce a useful metric for seeing how your receiver stacks up to other receivers. The Minimum Detectible Signal (MDS) of your receiver is the smallest input signal that your receiver can demodulate. This can be sometimes a subjective argument, but two versions are usually given. One is the MDS for a voice talking. The other is the MDS for a signal that is alternating between a 1KHz and 400Hz

signal. In both cases, the input signal is generated by your RF signal generator.

Hook up the entire receiver with the IF amp in place, measure MDS and find the new range of your transmitter/receiver pair. For the sake of your neighbors, please be sure to turn off your transmitter and speakers when you are not testing them.