EE133 - Prelab 4
FM Demodulation

1 Introduction

From a very high level, we can describe the operation of the PLL as simply the inverse of the VCO operation. So, whereas the VCO outputs a signal whose frequency varies as a function of the input voltage, the PLL outputs a voltage whose size varies as a function of the input signal frequency. After Lab 3, you should have a sense of how the VCO is able to perform its function (if not, please review the handouts on VCO's - this will be important to understanding the PLL). Now, let's look at how the PLL is implemented...

Please refer to Figure 2 in the course of this discussion. At the heart of the PLL is a VCO. In fact, the VCO is nearly identical to the LM566 which you used in lab last week (I told you it would be important). The rest of the PLL is nothing more than a feedback loop placed around the VCO so that it can be automatically adjusted to replicate the frequency of the incoming signal.

The feedback loop is straightforward as well. The first element (moving left to right in the diagram) is a phase comparator. Essentially, this is just a multiplier (and is in fact represented by the multiplier symbol in the diagram) which takes as its inputs the incoming signal and the output of the VCO. Assume for the moment that each signal is a square wave of a single frequency, but that the frequencies of the two are not the same. Then, when they are multiplied together, the result is a train of pulses whose widths vary in time as a function of the frequency offset between the two signals.

Integrating this pulse train, which is the job of the low-pass filter that follows the phase comparator, yields a slowly varying signal whose amplitude at any instant in time is proportional to the width of the pulses at that time and (by transitivity) to the frequency difference between the signals. This signal, gained up by an amount A, is then used to adjust the VCO output until the VCO and input signal are at the same frequency. At that point, there will be a constant phase difference between the two, yielding a constant DC voltage from the integrator that 'locks' the VCO at the correct frequency.

Note that the input voltage which 'locks' the VCO is actually the output of the PLL - it is a voltage whose amplitude is proportional to the frequency of the input! Now, if the input is not at a single frequency, but instead is FM modulated so that its frequency changes in time according to some modulating signal, then the PLL output voltage will be changing in proportion to that frequency variation and will therefore resemble the modulating signal - Presto, FM demodulation!

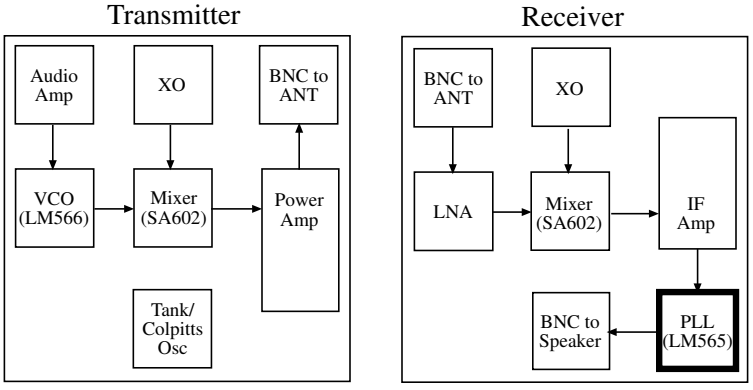

Figure 1: Roadmap for Lab 4

2 The Phase-Locked Loop

To provide you with a feel for the operation of the phase locked loop, you will simulate the phase locked loop using the SPICE deck that has been provided on the server. The deck is a behavior model of the PLL found in the HSPICE manuals. You are expected to test the model with the various different input signals that have been commented out in the SPICE deck. These inputs are:

- A sinusoid at the free running frequency of the VCO ($f_{mod} = f_{VCO}$)
- A sinusoid greater than the free running frequency of the VCO ($f_{mod} > f_{VCO}$)
- A sinusoid less than the free running frequency of the VCO ($f_{mod} < f_{VCO}$)

For the three input signals at 1MHz, 0.99MHz and 1.01MHz, do the following:

1. Using the Spice deck from the web, plot the transient output that appears on $v_{control}$, the output voltage, and record its final DC value.
2. For each of the three locked conditions, plot the input signal, v_{in}, and the signal from the output of the VCO v_{vco}, on the same page. Change the x-axis so that you are only looking at the signal from 195us to 200us. This will allow to get past the startup transient, and will also allow you to see greater detail.
3. Comment on the final DC voltage of the output for each of the three input signals. Do they agree with the expected results?
4. Comment on the phase difference between the input signal and the VCO output for each of the three inputs. Are they what you would expect?

3 FM Demodulation using the PLL

If a FM signal is fed as input to a PLL, the output voltage of the PLL will vary according to the frequency variations in the FM signal. But the instantaneous frequency of an FM signal varies according to the voltage of the modulating signal. As a result, the output voltage of the PLL becomes a scaled version of the modulating signal. What we have achieved therefore, is demodulation of the FM signal.

1. Using the SPICE deck, change the input to the FM input and plot the transient on $v_{control}$, the output voltage of the PLL for a FM input. Be sure to change the transient time in the .tran statement. Your simulation should take about 5 to 10 minutes. What is the frequency of the output obtained? Is it the same as the frequency of the waveform encoded in the FM input signal?
2. Calculate the total harmonic distortion of the demodulated signal.

4 Using A Practical PLL: the LM565

To use the LM565 for FM demodulation, we set the free-running frequency of the PLL to be equal to the carrier frequency of the FM signal so that frequency variations (modulation) of the input signal will not exceed the loop lock range. Pins 4 and 5 should be joined for our purposes. The demodulated signal is obtained from pin 7 through a coupling capacitor to remove any DC offset.

From the LM565 datasheet, you can find that the free running frequency of the LM565 can be set by the timing resistors and capacitors, as well as many other useful pieces of information on the 565.

1. Read the LM565 datasheet.
2. Using a timing capacitor of 100pF and supply voltage of 9V, choose a value for the timing resistor required for a free-running frequency of 300kHz.

3. Compute the hold range for our PLL? Is this sufficient for our $\Delta f = 50kHz$ from Lab 3?

4. What is the "Loop Gain" ($K_D K_O$) for your design? We desire the "Loop Bandwidth" to be greater than 100kHz, so we will place a 330pF capacitor from pin 7 to V_{cc} to act as a Lag Compensator (if you remember control theory). Verify that this is the correct choice for C.

5. Build the circuit in Figure 2 for lab. You will use the circuit for FM Demodulation so it should go on the receiver board. (Make sure to re-check all your connections before powering this chip on, you want to be sure to get this one right the first time.)

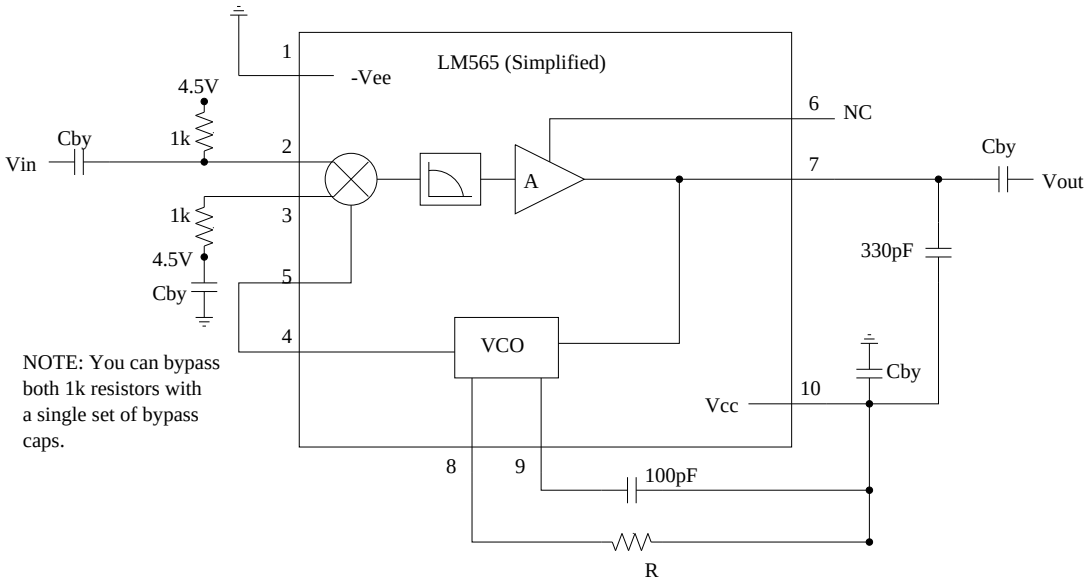

Figure 2: LM565 PLL

- **Soldering Tips**

  1. Be sure when soldering up the LM565 that you also solder in two BNC connectors to use for attaching the input and output cables to the PLL. We only have enough BNC connectors for every team to have two, so please just use the connectors you already have.
  2. **DO NOT CONNECT THE LM565 TO THE SAME POWER AND GROUND RAILS AS THE SA612 OR CRYSTAL OSCILLATOR.** Since the LM565 operates on 9V, while the SA612 and oscillator are expecting 4.5 V, you wil do serious damage to these other parts if you put everything on the same rails. In general, it is a good idea to power each stage separately while developing and characterizing them during the labs.
  3. To realize the timing resistor (R) we suggest you use two terminals of a 100 kΩ pot. That way, you can adjust the free-running frequency with minimal effort.