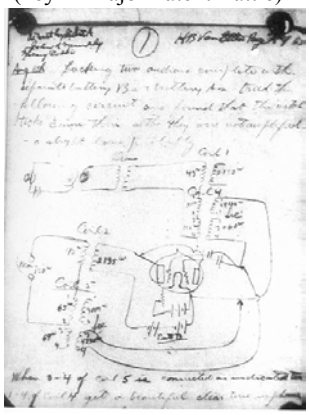
More about Notebooks and T-Shirts…

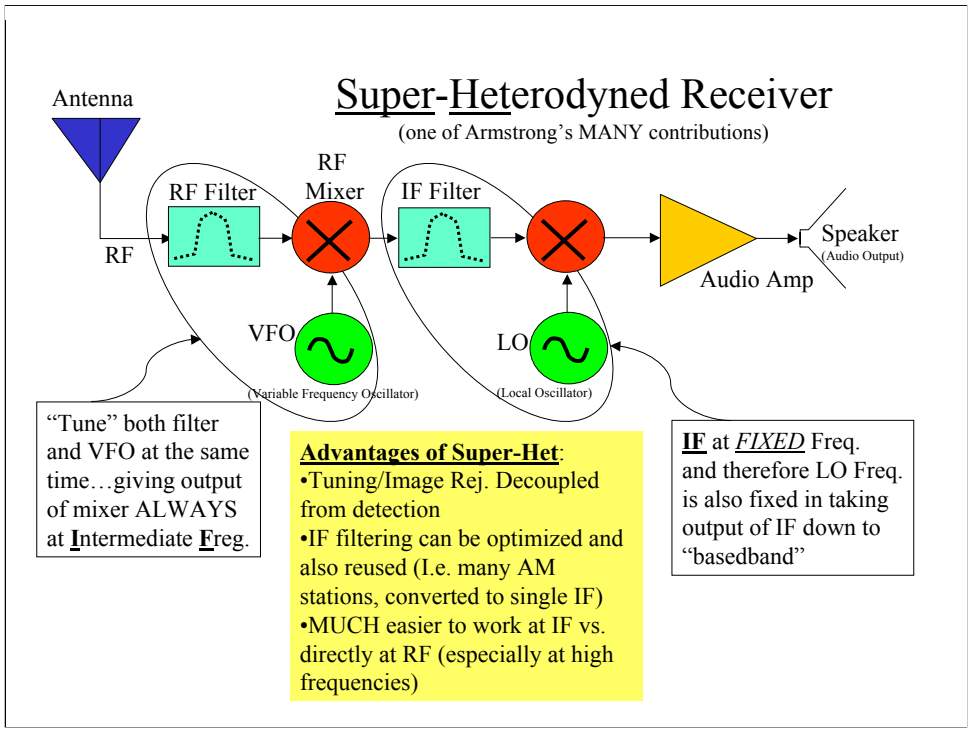
Lab Notebook from DeForest (key in Major Patent Battle)



Dear Lab Notebook
Lab 1--They say things are a bit different down here in the basement. Like how your biological clock no longer works. How the boiling point of water is slightly elevated. And how light slows down just a bit.
Lab 2--Hey, this lab wasn't that bad! (It's all downhill from here.)
Lab 3--On Valentines Day, I made for my significant other a witty valentine card. I used phrases like "dB my valentine" and "let's resonate." I'm not sure why I got slapped.
Lab 4--I stayed really late in lab last night, so I couldn't avoid falling asleep during Dutton's lecture. I dreamed that he was delivering our Commencement address, and he said that we had to impedance match our college years with the next stage of our lives.
Lab 5--My doctors tell me that somehow the presence of lead in my blood is three times the federal health limit, and if I don't stop whatever I'm doing, I will become mentally retarded. (Obviously, it's too late.)
Lab 6--I had a horrible nightmare that nothing worked, and the TAs told us to rebuild the whole damn thing. Wait, was that a dream?
Final--If we scream and no one cares, do we make a sound?

You need to get and keep a hard-bound lab notebook. This is stuff that is absolutely KEY for defining and protecting IP. When you go for a job inteview after graduation and you show them your EE133 Notebook (and IF you've done a careful, diligent job), you might find it to be a major asset (="job experience")

The DeForest story is amazing. He and his arch rival John Armstrong (inventor of FM and Hetero-dyning) had a pitched battle over IP. Unfortunately, this "B-" lab book was used as "evidence" even though DeForest couldn't actually explain his "invention"



One more pass on the Receiver side, this time giving a quick preview of how your commercial radio receivers work…

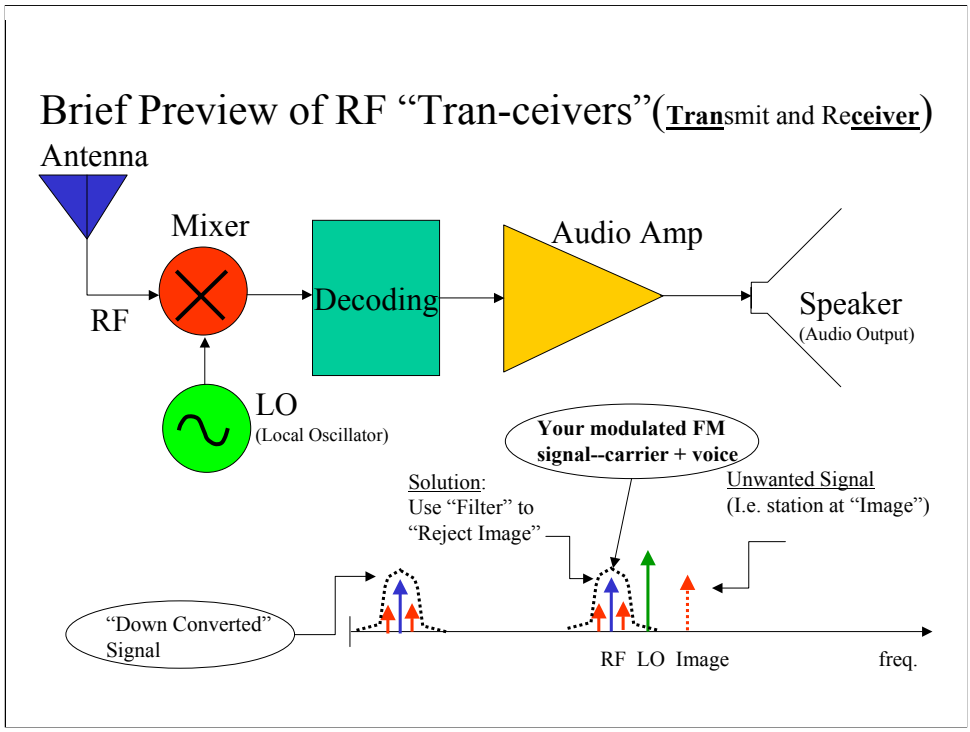
As you will certainly see (by doing in Lab #5), down conversion to a nicely controlled and well-defined intermediate frequency (IF) is very useful.

In commercial radio this is at 455KHz (and for your projects it will be a bit lower). It is at a FIXED frequency for ALL stations.

That means that the stage before the IF needs to have it's local oscillator (LO) "tuned" (using a Variable Frequency Oscillator=VFO) such that the resulting spectrum (I.e. the difference term from the law of the cosines) ends up exactly at the IF.

Then, when the spectrum (your station's signal) modulated about the IF is multiplied times the IF/LO, the signal is NOW at baseband.

The above slides and discussion are definitely a "fast forward" on things we will spend the rest of the quarter working on. This discussion is purely motivational in terms of block diagrams of transmitters and receivers….



What do RF signals look like in the frequency domain and how do we get them down to "baseband" where we can hear the information?

In the simplest case (90%+ of what EE133 is about) the RF band signal will be a carrier with sidebands…the sidebands are the information.

To get the RF signal down to baseband we use our good friend, the law of cosines:

$$Cos(\omega_1 t)Cos(\omega_2 t) = \frac{1}{2}\left[Sin(\omega_1 t - \omega_2 t) + Sin(\omega_1 t + \omega_2 t)\right]$$

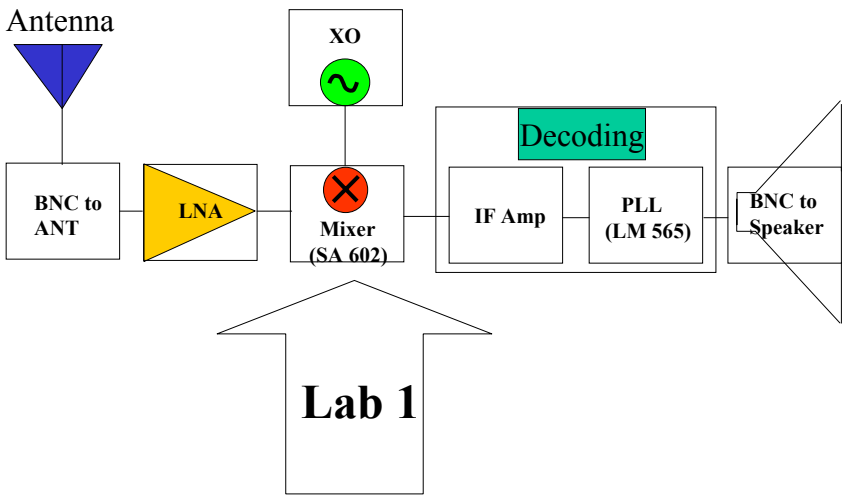
Now the math is the same but we are trying to only keep the difference terms that bring our signal back to "baseband". (and filter out the sum terms)

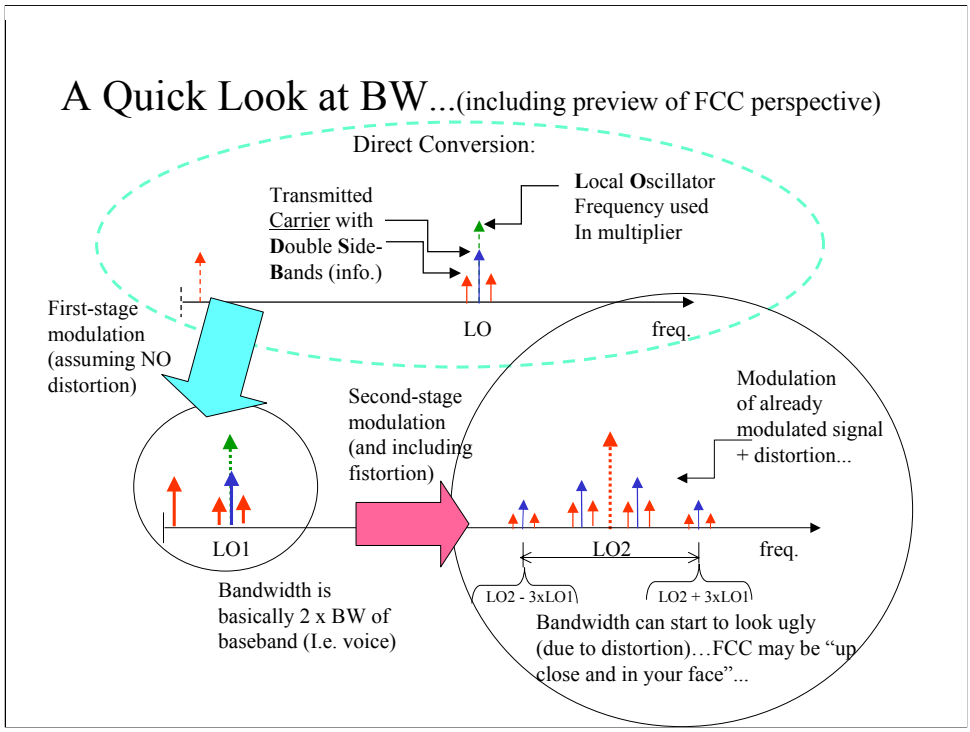
What's also shown in the figure is an unwanted "image" signal. Unfortunately, the multiplier will do its job on ALL signals present, unless we filter them out. If we don't filter out the "image"…

Both the local oscillator (LO) frequency minus our RF and the Image Freq. Minus the LO will BOTH end up in the same "down converted" frequency range.

Comment: in this example we did NOT convert the modulated signal all the way to zero frequency. That is, we down-converted by a different frequency than we up-converted. We'll be talking about this more in the demodulation labs--especially for FM [This NEW frequency will be the "IF"]

Blocks for SPAM Receiver (HO#1 p.12a)





The top figure is a very simple story (in theory) that is the wished for future--Direct Conversion. Basically, simply to move the information (double side bands) directly up to the carrier frequency and, by means of the LO (exactly at that carrier frequency) to again down convert the spectrum to baseband.

The lower figure shows that exact same figure PLUS the second stage modulation (hetero-dyning) to a second (and obviously higher) frequency.

The new piece of information here is the fact that various blocks, for example amplifiers, may not be linear and the process of distortion creates additional signals. Basically, the multiplier is happy to send them up in frequency and the overall bandwidth (BW) of the system can get large and ugly.

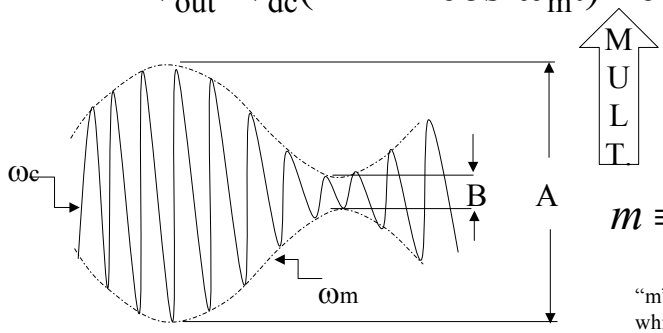
The Federal Communications Commission (FCC or "big brother") doesn't really like to see this ugliness. If we are in commercial radio band this may be putting your signals into some else's licensed band (a serious NO-NO…you get "shut down" for not obeying the rules)

Bottom-line: We will spend time as we go along learning more about spectra, bandwidth and linearity issues

Multipliers

Motivation about Multipliers--
based on our discussion of AM

$$v_{out} = v_{dc}(1 + m \cos \omega_m t) \bullet \cos \omega_c t$$



$$m \equiv \frac{v_m}{v_{dc}} = \frac{A - B}{A + B}$$

"m" is modulation index, which can be determined graphically using A and B*. It corresponds to the v_m and v_{dc} terms that we will see shortly for real voltages (and currents).

*** B cannot be NEGATIVE!** Over-modulation means that information is lost. Conversely, small "m" means inefficiency--power wasted in carrier and not sidebands

In the first lecture we talked very broadly about modulation and demodulation. To do these VERY COOL information processing steps we use multipliers (and the law of the cosines identity rules)

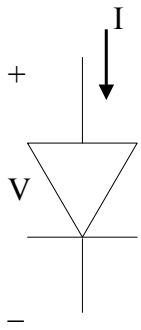
The above slide is again an AM signal; this time we've re-written the expression for some assumed "v_out" such that there are TWO terms…a "dc" term that will give us the carrier frequency (un-modulated) as an output and "m" times the product term we looked at before.

We can think of the "m" factor (or "index") in two ways:

1) The ratio of the "v_m" divided by "v_dc" or
2) GRAPHICALLY it's very nice to extract the "m" (MODULATION) index in terms of the difference and sum of the "A" and "B" terms as shown.

Key warning--"B"=0 ->"m"=1…beyond this condition (m>1) is NOT a useful region of operation! It's called "overmodulation" and information is lost (I.e. things don't "sound good" anymore). Also, we do like to have some of the carrier around for demodulation anyway. [The story about "the bet"…]

A Trivial Multiplier…[and Preview of Distortion Issues]



$$I = I_s[e^{\frac{qV}{kT}} - 1] \approx I_s[(1 + x + \frac{x^2}{2} + \frac{x^3}{3!}...) - 1]$$

$$I \approx I_s[x + \frac{x^2}{2} + \frac{x^3}{3!}...]$$

$$where:$$

$$x \equiv \frac{qV}{kT}$$

Comment: At very high frequencies and for older systems diodes are often used. Historically, it was easier to make a "fast diode" compared to a fast transistor (with amplification).

This is multiplication… but, one only gets x-times-x (assuming that one can filter out the higher and lower frequencies…) and…
All the other terms are higher order distortion. We'll have more serious discussion of this soon.

So, let's start talking about multipliers…

Here's a rather trivial device--either a diode with no gain or the base-emitter junction of a bipolar transistor which will give gain at the collector terminal. [Ch. 19 in the text is virtually ALL diodes]

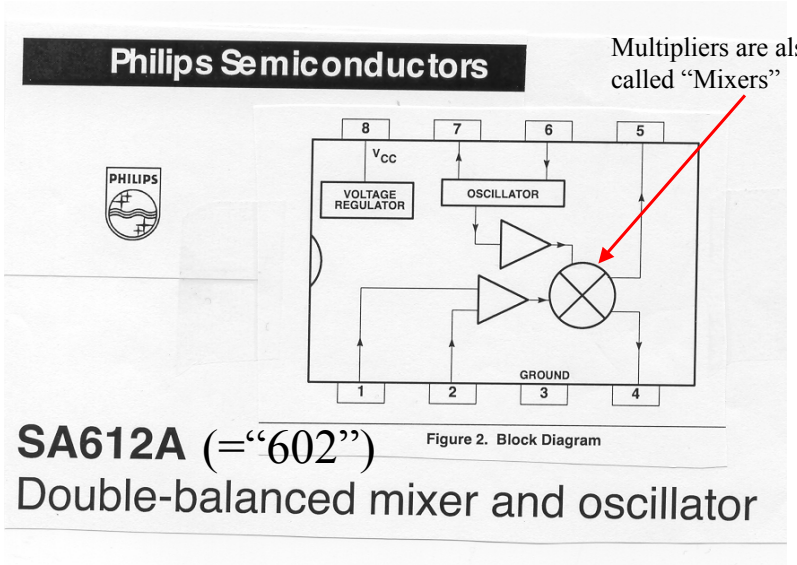
Just thinking about the diode (for the moment), as an exponential device. This means that if we take the Taylor Series expansion, there are terms in "x", "x^2" and higher order terms.

So, if the input variable (voltage=x) is the sum of two different frequency terms, there will be terms that include those frequencies (the "x" term) as well as a "squared term" (the x^2 term) etc.

Thus, we actually can get the multiplication function performed using this simple two-terminal device. In fact, at very high frequencies this is a great option since FAST diodes can be fabricated relatively easily.

BUT…since there are TONS of higher-order terms also present, the output needs to be carefully filtered to remove the unwanted frequency components. [I'll comment here about distortion]

Preview of an IC "Mixer"



This block diagram and Integrated Circuit (IC) is a classic example of integrated building blocks.

Namely, this chip contains not only the multiplier but also a single-transistor "oscillator" (you still need to add the feedback around it to make it oscillate) plus…

Biasing and Buffering so that you can quickly implement most all of what you need for modulation or demodulation of signals.

You'll come to know and love this chip…it's really COOL and AWESOME!

But…

We'd better go back to the basics of how the multiplier works at the transistor level.

Looking inside the IC…

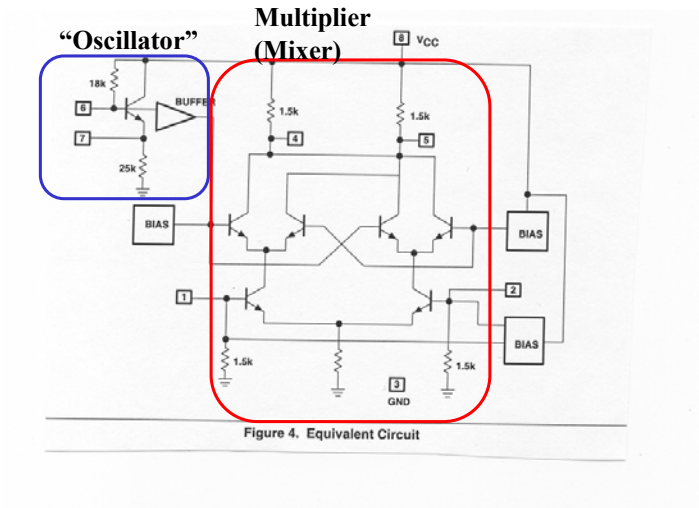


Figure 4. Equivalent Circuit

This is the details of the two key blocks inside the 612:

The "four quadrant multiplier"

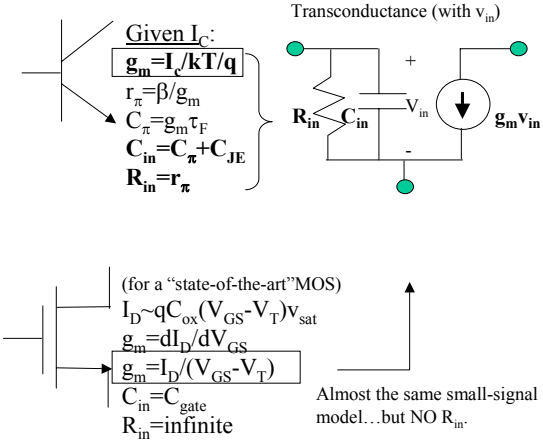
The single-transistor "kit part" for making an "Oscillator"

Note: the multiplier looks basically like three differential pairs of transistors stacked together.

Again, we won't discuss this yet, but it's coming VERY SOON :)

A word about Transistors…

•We will be using bipolar junction transistors (BJTs) frequently in EE133. The reasons are two-fold: 1) they are **very forgiving** when you touch them (vs MOS devices where you can "blow-out" the gate oxide due to "Electro-Static Discharge"=ESD); 2) there are really **cool chips and simple circuits** that use BJTs.
•But, this will require some "fast forward" learning for you. For basics of BJTs see notes from EE116 or EE216.
•Next year there will be a new BJT circuits class (taught by Prof. Wooley and yours truly)…in the future it can be taken concurrently with EE133.
•Alas, since this new course is not here yet, I will be giving you BJT circuits lessons for the next few weeks.
•The following is lesson number one…



This slide has been added to QUICKLY help you ramp-up on small-signal models, without worrying too much about their derivation or details of MOS versus BJT.

In fact, we plan to mostly be doing BJT circuits in EE133 so this slide is the DEFINITION of TERMS (ie R_{in}, C_{in} and g_m)

There are TWO pieces of REALLY GOOD NEWS:

1) For BJT, given I_C it's really easy to get gm (and if you're running SPICE, it's not that hard to get I_C!)
2) The small-signal model--either for MOS or BJT--looks identical, with the slight extra concern that for BJT there is a finite R_{in} (whereas for MOS this term is infinite)

So, given this very quick introduction to BJT model and its small-signal version, we now launch into the zero- and first-order models for the multiplier

The most basic multiplier

(called the "transconductance multiplier")

$$v_o = -g_m R_L \cdot v_{in1}$$

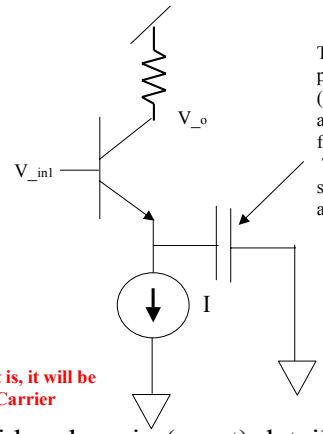
but...what_if :

$$g_m = I(v_{in2}) \cdot \frac{q}{kT}$$

then :

$$v_o = -R_L \frac{q}{kT}[I(v_{in2}) \cdot v_{in1}]$$

But: $I(v_{in2})$ should vary SLOWLY--that is, it will be the Modulating Signal rather than the Carrier



This capacitor is here to provide a "virtual" ac ground. (for the high frequency terms at v_{in1}; but not for lower frequency v_{in2} terms) That is, so that the small-signal gain expression for CE applies…

The following slides show in (great) detail how we actually realize this simple circuit in practice…

Here's a more elegant (and from our perspective more practical) multiplier circuit.

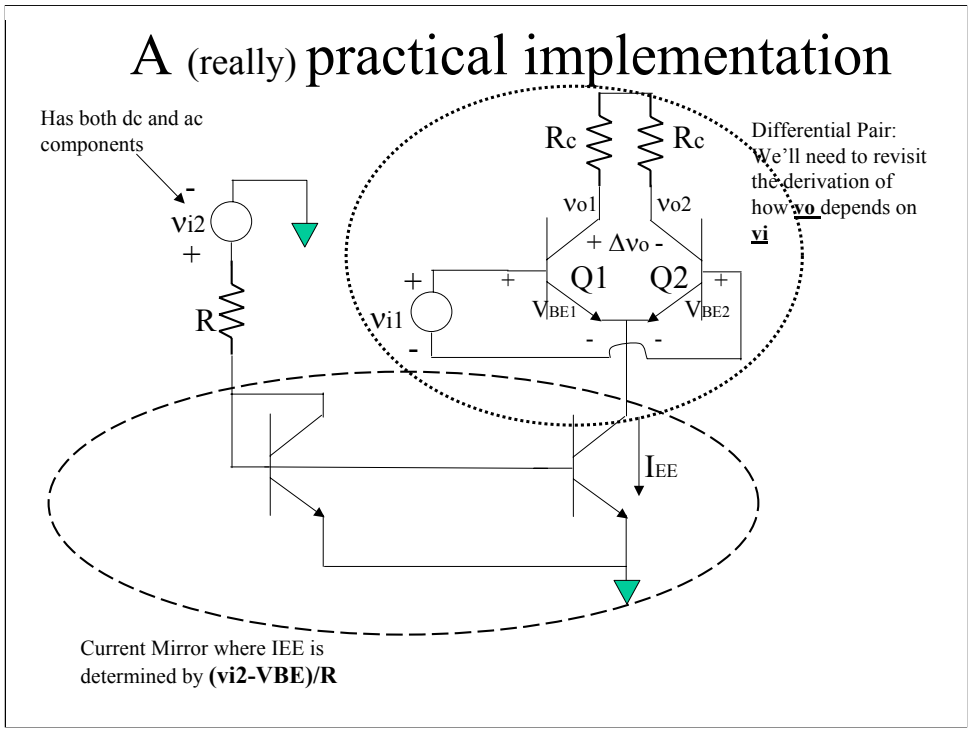
If we just thought about it in terms of EE113 where the capacitor allowed the high-frequency signals to see an ac "ground", then the top equation for small-signal (ac) gain would apply.

Now, if we let the dc current vary at a much, much slower frequency (than v_in1), then the ac small-signal transconductance (g_m) varies at this frequency.

Following the simple math in terms of how g_m depends on I, it becomes clear that the small-signal (ac) output voltage becomes a product of the two frequency components.

This circuit is:

1) A trivial example (that needs to be embellished to realize a still more "practical" circuit)
2) Has limitations that the current (I) must always be positive which implies that it's operation is limited to two quadrants (two-quad) in the total space of (+/-) v_out versus (+/-) v_in



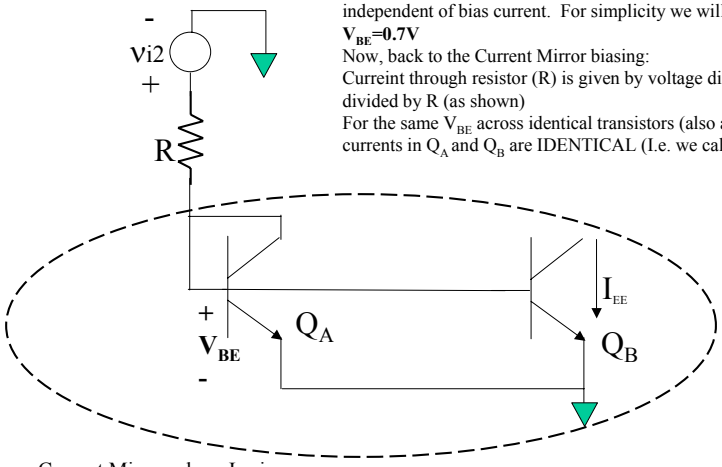
So, here's the "real" implementation of the circuit shown in the last figure…

Using a differential pair (diff-pair) on the upper part of the circuit, we now see how the "ac ground" is actually implemented--it's a virtual (differential mode) ground.

The current source is our old friend the current mirror. Hence, the [dc + ac] voltages applied across the resistor in series with the "diode-connected-transistor" needs to always have positive current flowing (as the per direction of the arrow)

The next set of slides will walk us through the sub-blocks and math of this simple "two-quad" multiplier…

Review of Current Mirror (w.BJTs)



Assumption, that makes BJT circuits simple and COOL (compared to more difficult MOS bias calculations)…V_{BE} is a constant, roughly independent of bias current. For simplicity we will use the value of **V_{BE}=0.7V**

Now, back to the Current Mirror biasing:

Curreint through resistor (R) is given by voltage difference (v_{i2}-V_{BE}) divided by R (as shown)

For the same V_{BE} across identical transistors (also assumed) then the currents in Q_A and Q_B are IDENTICAL (I.e. we call it a "Mirror")

Current Mirror where I_{EE} is determined by (v_{i2}-V_{BE})/R

I've added this slide as a review and reminder about current sources.

Assuming (a good assumtion I hope!) that you have done current sources in EE113 or EE101B, then the only NEW point here is the convenient assuption that V_{BE} is a constant (versus having to compute it based on an equation for either I_D for MOS of I_C for BJT)

The basic BJT "Laws" and their applications

$$I_C = I_S e^{\frac{V_{BE}}{V_T}}$$

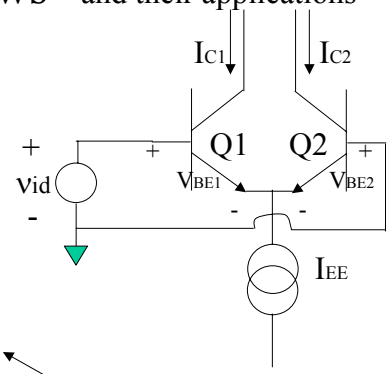
$$V_T = \frac{kT}{q}$$

$$\therefore V_{BE} = V_T \ln\left(\frac{I_C}{I_S}\right)$$

$$and\_for\_each\_Q_x$$

$$V_{BE1} = V_T \ln\left(\frac{I_{C1}}{I_S}\right); V_{BE2} = V_T \ln\left(\frac{I_{C2}}{I_S}\right)$$

$$\therefore v_{id} = V_T \ln\left(\frac{I_{C1}}{I_{C2}}\right)$$



Each transistor (Q) has it's V_{BE} determined by the log of the ratio Ic/Is

And the differential input $v_{id} = V_{BE1} - V_{BE2}$ is determined by the log of the ratio I_{c1}/I_{c2}

This slide reminds us of several important definitions and related properties of the bipolar transistor (BJT) and their use in the differential pair (diff-pair)

With BJTs we often use V_T as defined…NOT to be confused with "threshold voltage" for a MOS

The device is EXPONENTIAL; therefore the necessary "V_{BE}" for a given I_C is given by the $\log_e$ (or simply ln) function shown.

If we have two different I_C values, corresponding to differences in the respective V_{BE}'s for the transistors, then the total difference in voltage v_{id} around the loop (with input shown) is given by the log of the ratio of the two I_C's.

Given this set of definitions (and properties), let's go on to consider again the two-quad and then the four-quad multipliers…

In terms of the two Ic's and v_{id}…

$$I_{C1} = I_{C2} e^{\frac{+v_{id}}{V_T}} \; ...or... I_{C2} = I_{C1} e^{\frac{-v_{id}}{V_T}}$$

$$I_{C1} + I_{C2} = I_{EE}$$

$$and\_with\_\text{mod}est\_"hacking"$$

$$I_{C1} = I_{EE} - I_{C2} = \frac{I_{EE}}{1 + e^{\frac{-v_{id}}{V_T}}}$$

$$I_{C2} = I_{EE} - I_{C1} = \frac{I_{EE}}{1 + e^{\frac{+v_{id}}{V_T}}}$$

Basically, we express each Ic interms of the total "tail current" I_{EE} and the total input (differential) voltage v_{id}

$$\Delta I_C = I_{C1} - I_{C2} = I_{EE}\left(\frac{1}{1 + e^{\frac{-v_{id}}{V_T}}} - \frac{1}{1 + e^{\frac{+v_{id}}{V_T}}}\right)$$

$$\Delta I_C = I_{EE} \tanh\left(\frac{v_{id}}{2V_T}\right)$$

This is the general expression for the difference of the two collector currents in terms of the input voltage…we will soon see that in small-signal it reduces to gm times vid

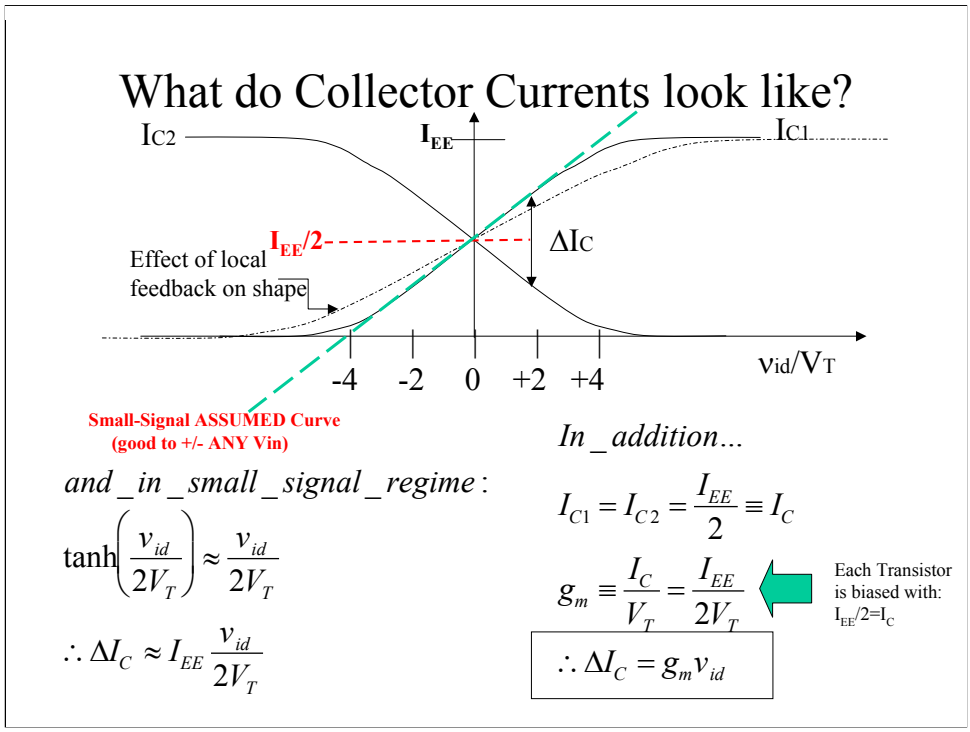
This slide has a fair bit of algebraic manipulations. The key points are as follows:

Since this circuit is a diff-pair, the two collector currents add up to I_{EE}

By manipulating the expressions for I_{C1} and I_{C2} in terms of I_{EE} and the "differential input voltage" the two rather messy looking formulae are obtained…BUT!

If we take the DIFFERENCE between the two currents (which will correspond to a differential output VOLTAGE if the currents flow through equal valued resistors), and again after a bit of manipulation, we get an elegant hyperbolic tangent ("tanh") result, as shown.

We'll use this formulation several times in the future. Hence, it's useful for you to be sure you believe the result :) Derive it?



This graphical view of the results to this point, including some (optional) simplifying approximations, should help to visualize how the two collector currents vary with input differential voltage (NORMALIZED with respect to the "thermal voltage" V_T)

The difference current (ΔI_C) is shown; within a range of only a few V_T the currents swing from being dominated by I_{C2} (negative v_{id}) to dominated by I_{c1} as shown for positive v_{id}

For small input voltages (compared to V_T) the tanh function is approximately equal to its argument.

Under these conditions the observed ΔI_C is identical to what we would compute using the ac small-signal model where each transistor has current determined by $I_C=I_{EE}/2$

We'll come back to the dashed line part of the curve in a few minutes…

And now for more details about I_{EE}

$$I_{EE} = \frac{v_{i2} - V_{BE}}{R} \ldots where \ldots v_{i2} = v_{i2}(dc) + v_{i2}(ac)$$

$$= \frac{v_{i2}(dc) - V_{BE}}{R} + \frac{v_{i2}(ac)}{R}\cos(\omega_m t)$$

$$I_{EE} = \frac{v_{dc}}{R} + \frac{v_m}{R}\cos(\omega_m t) \ldots where:$$

$$v_{dc} \equiv v_{i2}(dc) - V_{BE}$$

$$v_m \equiv v_{i2}(ac)$$

Basically, we've achieved the form we initially assumed for the "Amplitude Modulating" part of our AM signal

The results from the previous page were identical to what would follow from an EE113-style problem…namely only ONE input voltage v_{id} on the diff-pair.

As stated earlier, to get multiplication we need to let I_{EE} also become a function of frequency.

Hence, v_{i2} now is the driving force (through the current mirror) as shown by the first equation. Note: we have both a "dc" and "ac" term for v_{i2} (BOTH are needed to keep current positive and the diode and transistor ON)

So, after a bit of re-arranging, we get the two components for I_{EE} as shown…

And using the above results in ΔI_C

$$\Delta I_C = I_{EE}\tanh\left(\frac{v_{id}}{2V_T}\right) = \frac{1}{R}\left(v_{dc} + v_m\cos\omega_m t\right)\tanh\left(\frac{v_{id}}{2V_T}\right)$$

$$and\_now\_considering\_R_C\_loading:$$

$$\Delta v_o = -\Delta I_C R_C = \frac{-R_C}{R}\left(v_{dc} + v_m\cos\omega_m t\right)\tanh\left(\frac{v_{id}}{2V_T}\right)$$

$$(and\_for\_small\_signal...)$$

$$\Delta v_o = \frac{-R_C}{2V_T R}\left(v_{dc} + v_m\cos\omega_m t\right)\cdot \overbrace{v_{id}}^{v_{id}}\cos\omega_c t$$

$$where\_v_{id}\_now\_has\_frequency\_\omega_c$$

Now we've realized the final AM signal based on the two blocks:
- Differential pair to handle the carrier (ωc)
- Current Mirror to provide a "modulating" tail current (ωm)

Using this expression for I_{EE} along with the previous derivation for the differential pair, we get the expression for Δv_o, by applying the ΔI_C across "load resistors"

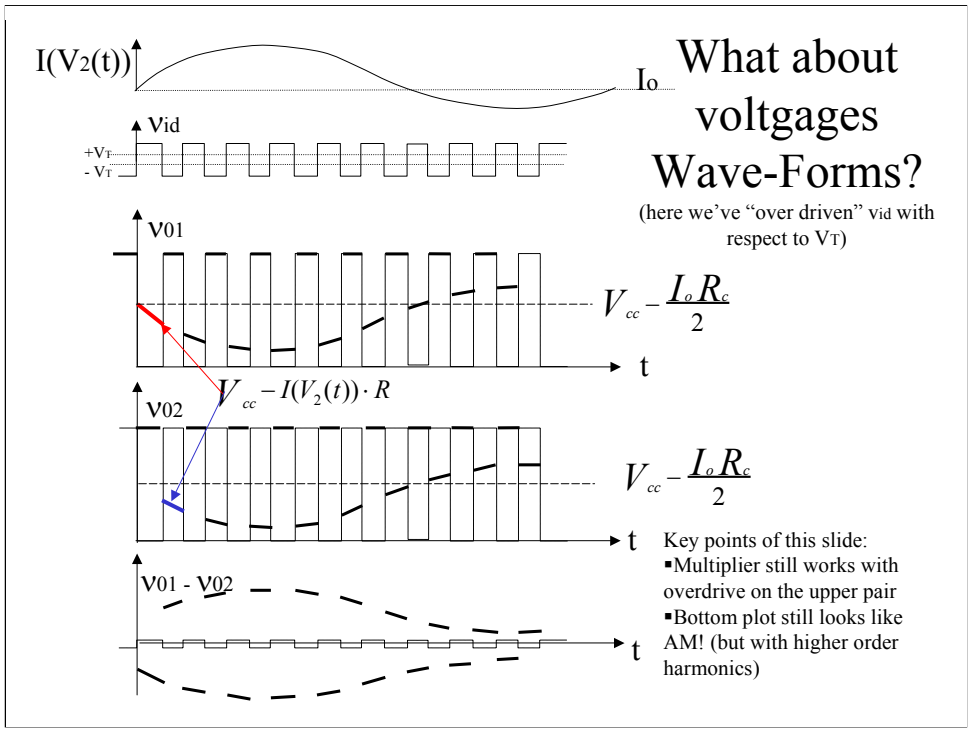
Again, using the "small argument" approximation to the "tanh" function, we get a simple expression (IN BOX) for the output voltage.

And…

PRESTO! We have multiplication (of the two-quad variety).

I'm sure there's more to be discussed and reviewed in going over the previous set of half-dozen slides. But, let's keep on moving in order to get to the FOUR-QUAD version….

Oh, but before we do that let's look at what happens if we "overdrive" the high frequency input (v_{i1})…



This is a VERY interesting set of plots.

The top plot shows I_{EE} varying very SLOWLY with frequency. Where it "crosses the horizontal axis" should NOT be understood to be negative current--the reference is I_O.

Assuming that we look at each collector voltage (v_{o1} and v_{02}) referenced to V_{CC} (the supply voltage).

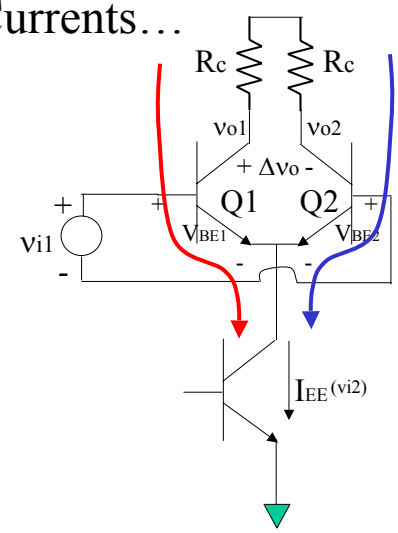
If the input v_{id} is sufficiently large compared to V_T then the current is "switched" (in basically a "digital" sense) between the two transistors. Hence, when it is flowing through Q1 then that collector voltage drops by the corresponding I_{EE}*R.

During the opposite swing of v_{id} then the current (all of it!) switches to Q2 and that collector voltage drops.

If we take the DIFFERENCE between the two voltages we see an "ENVELOP" that follows the shape of the I_{EE}

In class let's talk a bit about the "spectra" of this signal versus what we traditionally think of as AM…

Reference for Currents…

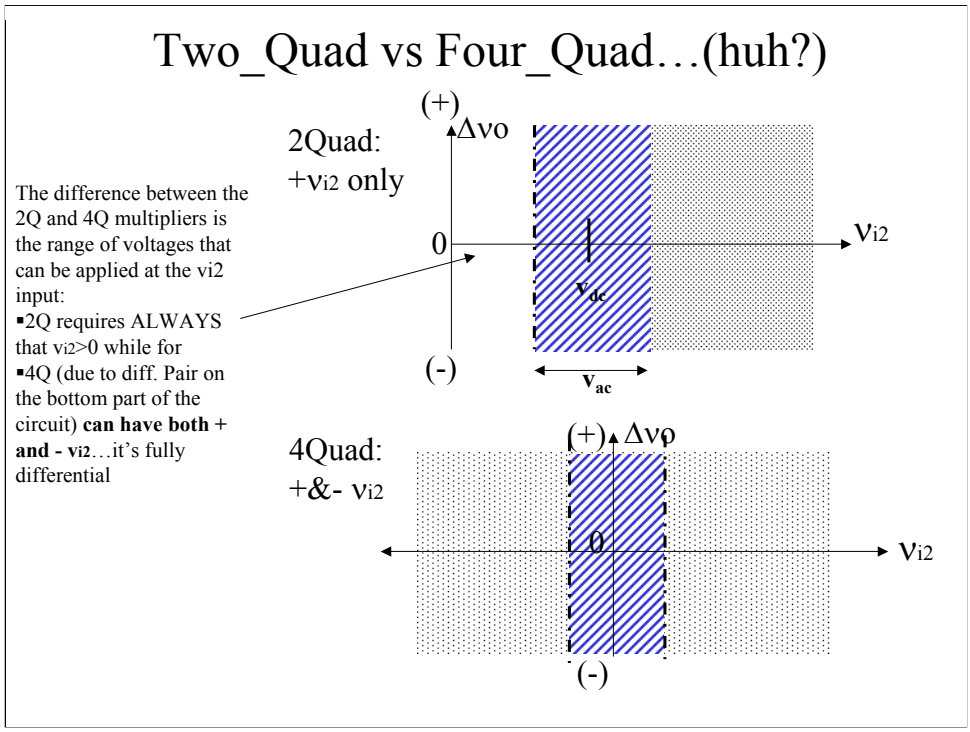


So, here's the "real" implementation of the circuit shown in the last figure…

Using a differential pair (diff-pair) on the upper part of the circuit, we now see how the "ac ground" is actually implemented--it's a virtual (differential mode) ground.

The current source is our old friend the current mirror. Hence, the [dc + ac] voltages applied across the resistor in series with the "diode-connected-transistor" needs to always have positive current flowing (as the per direction of the arrow)

The next set of slides will walk us through the sub-blocks and math of this simple "two-quad" multiplier…



We've mentioned "two-quad" and "four-quad"…now let's see what that means.

The top figure indicated that for only a limited range of v_{i2} that is positive do we get multiplication in terms of the output swing.

The "cross hatched" region indicates the range where the multiplication has minimum distortion.

This corresponds to a "two-quad" multiplier…we can't get multiplication in the left-half plane for negative v_{i2}

The bottom figure shows the "four-quad" multiplier.

Here we can have v_{i2} with both positive and negative values.

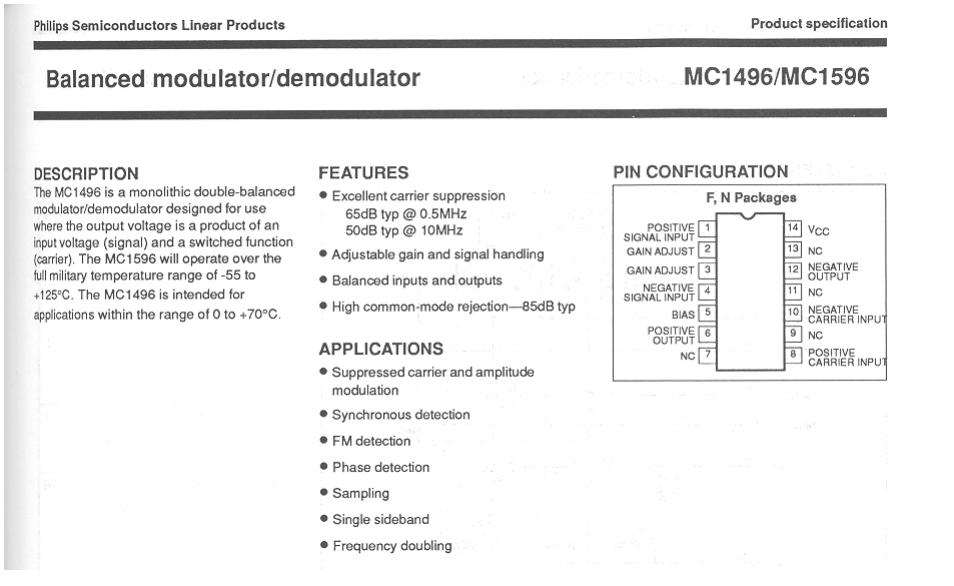
So…

What does it take to create the additional two-quadrants?

Let's see…

(the following will be somewhat more qualitative, only because the math gets a bit tedious and time is short in terms of getting into lab)

A Classic Multiplier IC



Philips Semiconductors Linear Products — Product specification

Balanced modulator/demodulator — **MC1496/MC1596**

DESCRIPTION

The MC1496 is a monolithic double-balanced modulator/demodulator designed for use where the output voltage is a product of an input voltage (signal) and a switched function (carrier). The MC1596 will operate over the full military temperature range of -55 to +125°C. The MC1496 is intended for applications within the range of 0 to +70°C.

FEATURES

- Excellent carrier suppression
  65dB typ @ 0.5MHz
  50dB typ @ 10MHz
- Adjustable gain and signal handling
- Balanced inputs and outputs
- High common-mode rejection—85dB typ

APPLICATIONS

- Suppressed carrier and amplitude modulation
- Synchronous detection
- FM detection
- Phase detection
- Sampling
- Single sideband
- Frequency doubling

PIN CONFIGURATION

F, N Packages

POSITIVE SIGNAL INPUT	1	14	V_{CC}
GAIN ADJUST	2	13	NC
GAIN ADJUST	3	12	NEGATIVE OUTPUT
NEGATIVE SIGNAL INPUT	4	11	NC
BIAS	5	10	NEGATIVE CARRIER INPUT
POSITIVE OUTPUT	6	9	NC
NC	7	8	POSITIVE CARRIER INPUT

Here's another version of a 4-Quad Multiplier…the Grand-Daddy of them all, the 1496

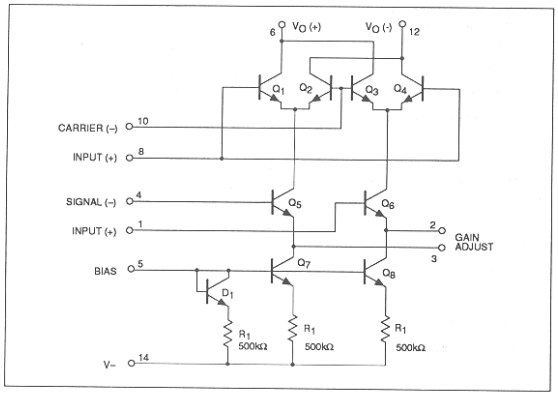
Discussion of this chip will be considered in the Lab.

The main point of showing this and the next page here is to give you positive reinforcement that the following discussion is not purely an "academic exercise"

Details of the IC

Balanced modulator/demodulator
MC1496/MC1596

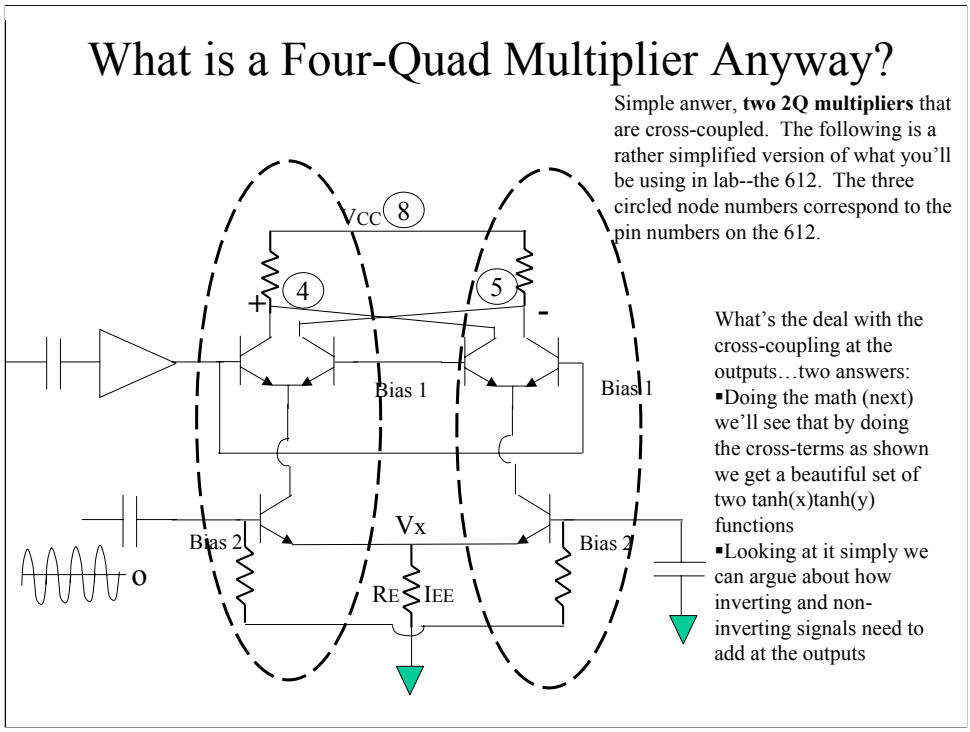
EQUIVALENT SCHEMATIC



In contrast to the 612 IC, the 1496 is a bare-bones multiplier, whereas the 612 gives much more integrated functionality.

Nonetheless, what you see is indeed what you get.

And, based on the following lecture materials, you should be able to 100% understand the function of each transistor and resistor in the IC :)

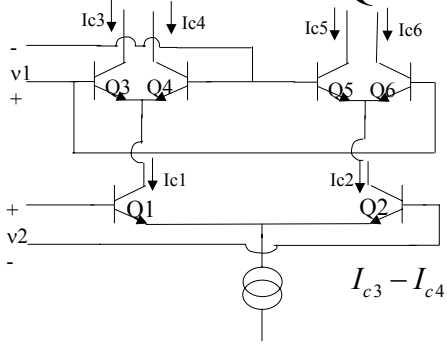


Basically, the 4-Quad is the combination of TWO x 2-Quad, where the cross-coupling of the outputs at nodes 4 & 5 is needed to correctly add the phases of collector currents (as will be seen shortly from the math)

Why is it now a 4-Quad? The bottom diff-pair can now handle both positive and negative signals (per the sine wave shown with a "0" volts reference)--complete biasing circuitry is NOT SHOWN.

I'm sure there are other things we'll discuss in class but, let's move on and do the needed math to show how this configuration becomes a 4-Quad multiplier…

Derivation of 4Q Results--defining Ic's



$$I_{c3} - I_{c4} = \frac{I_{c1}}{1 + e^{-\frac{v_1}{V_T}}} - \frac{I_{c1}}{1 + e^{+\frac{v_1}{V_T}}}$$

$$= \tanh\left(\frac{v_1}{2V_T}\right) \cdot I_{c1} <-- I_{c1} = \frac{I_{EE}}{1 + e^{-\frac{v_2}{V_T}}}$$

$$I_{c5} - I_{c6} = \tanh\left(\frac{v_1}{2V_T}\right) \cdot I_{c2} <-- I_{c2} = \frac{I_{EE}}{1 + e^{+\frac{v_2}{V_T}}}$$

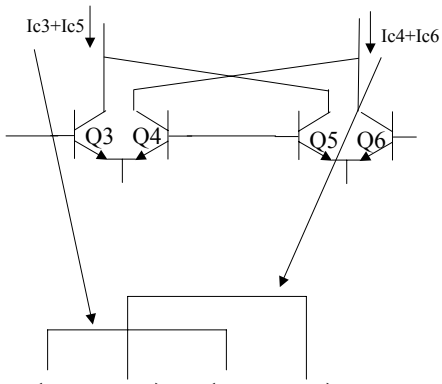
Remember when we first derived the "tanh" solution for the diff-pair and I said it was a good idea to be sure you understand how the math works out to give that solution?

Here we are again, now with TWO diff-pairs, and each of the pairs--Q3-Q4 and Q5-Q6--yields the same "tanh" solution with respect to it's input variable v1 (normalized with respect to V_T)

Note that now each of the two terms have the collector currents from I_{C1} and I_{C2} as the other part of the multiplication.

The next slide shows how we further manipulate the above two expressions….

How to get the final "Tanh" at Outputs



Note: The two (bracketted) terms, after working with the terms in Ic1 and Ic2, give the final expression in terms of tanh(v1) and tanh(v2). From the circuit connection point of view, the two terms (Ic3+Ic5) and (Ic4+Ic6) respectively appear at the two collectors as shown. This explains why the respective collectors are "cross coupled".

$$(I_{c3} - I_{c4}) + (I_{c5} - I_{c6}) = I_{EE} \tanh\left(\frac{v_1}{2V_T}\right) \cdot \tanh\left(\frac{v_2}{2V_T}\right)$$

As shown above, if we ADD the two (bracketed) terms, by looking at the "regrouped" pair of terms called out with the [Square] brackets, we see that…

At node 4 (two slides back) we are summing collectors 3&5 and at node 5 we are summing collectors 4&6.

By summing the two differential terms from the previous slide

And…

Expressing them each in terms of I_{EE} rather that I_{C1} and I_{C2} we get a beautifully symmetric answer which is "tanh" x "tanh".

For the small-signal case where the input voltages are smaller than or comparable to V_T then we have, using the small argument expansions, an ideal multiplier.

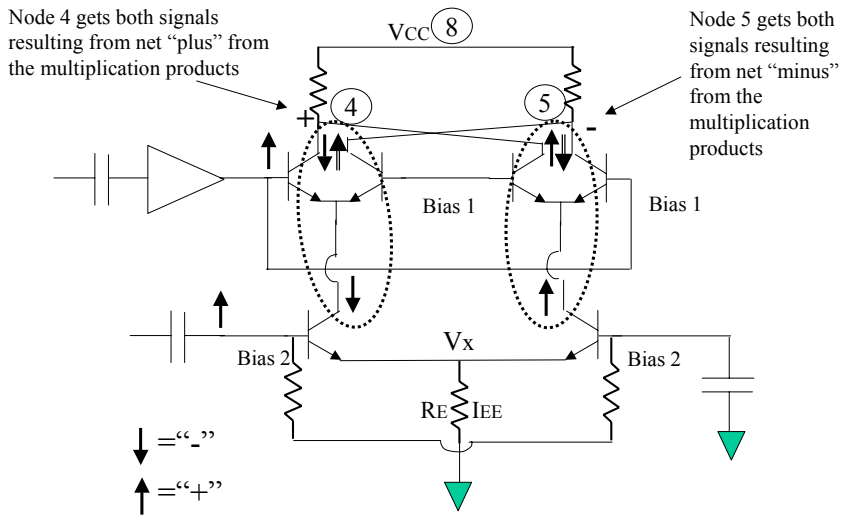
But…unfortunately, limiting ourselves to the thermal voltage as input signals does NOT provide enough voltage for most circuits.

So…

We have to consider circuit improvements or regimes of operation where this limitation won't hurt us.

Physical argument about connections

(plus x plus=**plus**; minus x plus=**minus**; minus x minus=**plus**)



This slide is a physical “walk through” considering what happens when input voltages go “up” , in turn, what are the changes output voltage at the respective collectors.

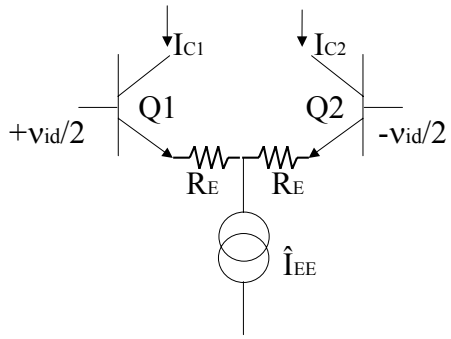
The KEY point is to note (following the “rules” about +/-) that at node 4 BOTH pairs of transistors (and their “arrows”) yield a net “+”

And…

At node 3 BOTH pairs of transistors (again following the “rules” for sign convention) yield a “-”

This discussion is simply qualitative; it’s probably more useful ultimately for you to do the math that goes along with the “double tanh” expression on the previous slide.

Way to improve input range for bottom differential pair (versus 612 limits)



Add RE to each transistor which degrades it's transconductance; gm'=gm/(1+gmRE)

A KEY challenge with the 4-Quad from the previous several slides is the limitation that BOTH inputs need to be "small signal"

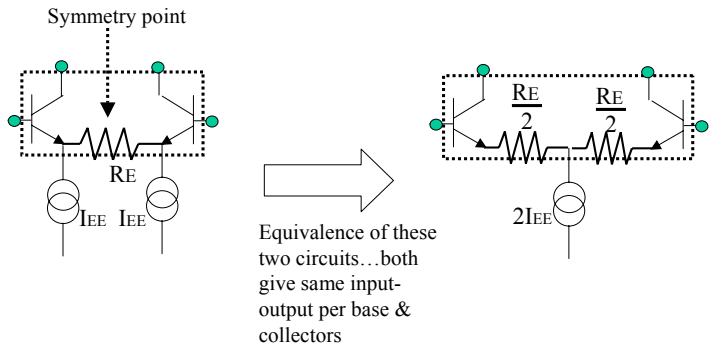
This limitation can be overcome for the lower diff-pair by adding local feedback ("series-series" as discussed in a separate handout) that in effect LINEARIZES the two currents with respect to v_{i2}

The multiplier still works, especially as viewed from the upper diff-pairs and their cross-coupling.

The math is not that beautiful (we loose the second "tanh" function)

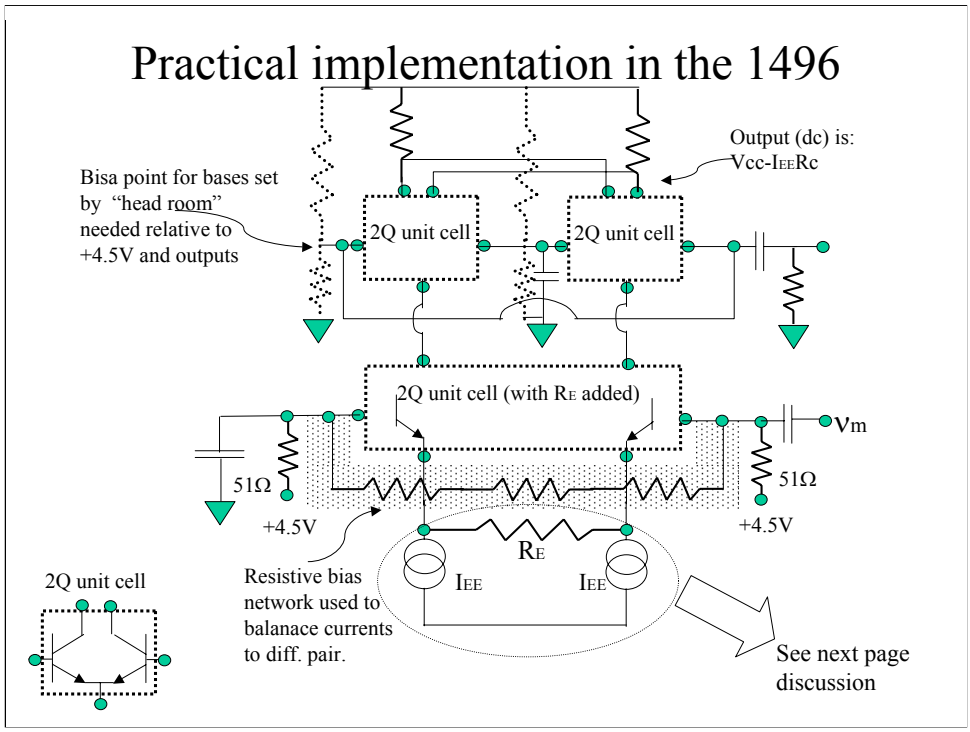
Considering the earlier plot of ΔI_C versus v_{id}, we can now discuss the effect of adding R_E in terms of extending the input range at the expense of lowering the gain…(to be discussed in class)

An Equivalent way to do it with single R_E



This slide reminds us about some of the "half circuit" issues that allow us to implement the emitter-degenerated diff-pair with a single R_E.

Again, I'll probably discuss a bit more in class.



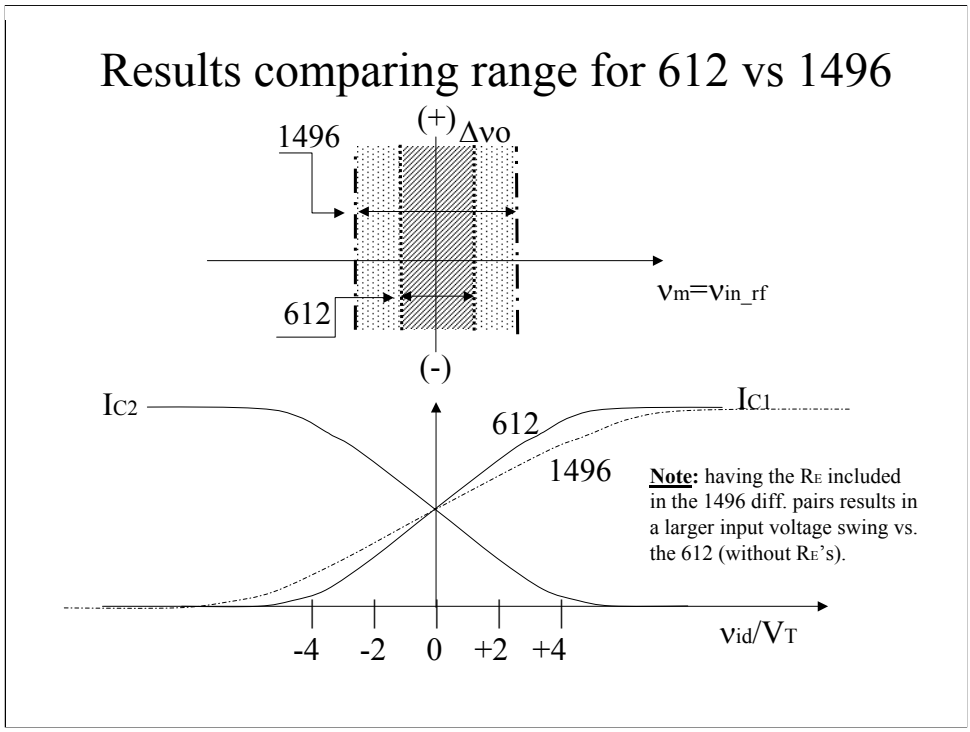
The reason for the discussion on the previous page is manifest in this circuit…a simplified version of 1496--a very popular and powerful multiplier circuit.

There's a LOT of additional circuitry surrounding this block--both inside the chip and what you add externally.

Internally, obviously we need to provide bias voltages to the bases as well as certain "trimming" resistors to balance the bottom diff-pair.

The 51 Ω "bias" resistors have been added to match the (ac) impedance to the generator and measurement instruments.

There are surely other additional points to be discussed in class



Finally, here are a few review points about the 4-Quad picture, now augmented with symbolic versions of what the signal range looks like for the 1496 (discussed in the last figure) ad the 612 which DOESN'T have emitter degeneration.

Clearly, the input dynamic range for v_{i2} is markedly improved by adding the emitter degeneration.

In lab you will see the effects of having (or NOT having) such linearization on the lower diff-pair.

Basically, for some applications we really want (or need) the linearization.

If we don't have linearization then signal distortion occurs (added spectra) that we must deal with.

The discussion of distortion is very important and will be added as we move closer to the final project.

Armstong, Antennae & Wireless