BIPOLAR AND MOS ANALOG INTEGRATED CIRCUIT DESIGN

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PART I: FUNDAMENTALS OF PHASE-LOCKED LOOPS

12.1. PRINCIPLE OF OPERATION OF A PLL SYSTEM

The basic PLL system is comprised of three essential blocks: (1) a phase detector, (2) a loop filter, and (3) a voltage-controlled oscillator (VCO). These three blocks are interconnected to form a feedback system, as shown in Figure 12.1. With reference to the block diagram of Figure 12.1, the principle of operation of a PLL can be qualitatively described as follows.

The phase detector compares the phase of the periodic input signal $V_s(t)$ with the output frequency of the VCO and generates an error voltage $V_d(t)$. This voltage signal is then filtered by the loop filter and is applied to the control terminal of the VCO in the form of the error voltage $V_e(t)$ to control its frequency of oscillation.

Normally, with no input signal applied to the PLL, the filtered error voltage $V_e(t)$ in the feedback loop is equal to zero. This is known as the free-running condition of the PLL, where the VCO operates at a steady-state frequency $\omega_o = 2\pi f_o$, which is called the VCO free-running frequency. If a periodic input signal is applied to the PLL such that the input frequency $\omega_s = 2\pi f_s$ is sufficiently close to the VCO free-running frequency, the feedback nature of the PLL causes an error voltage to be generated, forcing the VCO to synchronize with the input frequency. When this happens, the PLL is said to be *locked* on the input signal frequency.

When the PLL is locked on the input signal, the VCO frequency is *identical* to the input frequency f_s, except for a finite phase difference ϕ_o. This net phase difference, or *phase error*, ϕ_o is necessary to generate the corrective error voltage $V_e(t)$ to shift the VCO frequency from f_o to f_s and thus maintain lock. If the input signal frequency varies slowly, the PLL can still stay locked and track the input signal by generating additional phase error, which would result in a necessary change in the filtered error voltage $V_e(t)$ to maintain lock. The VCO control voltage $V_e(t)$ necessary to maintain lock is proportional to the frequency shift of the incoming signal, relative to the VCO free-running frequency. This self-correcting ability of the system allows the PLL to track the frequency changes of an input signal, once it is locked. The range of frequencies over

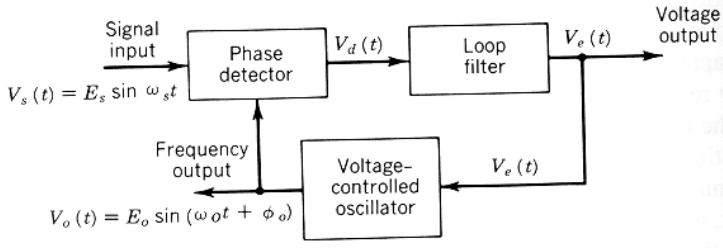


FIGURE 12.1. Block diagram of PLL system.

which the PLL can maintain lock with an input signal is defined as the *lock range* of the system. This is different from the range of frequencies over which the PLL can acquire lock with the incoming signal. This latter range of frequencies is known as the *capture range,* or acquisition range, of the PLL. For reasons that will be described later, the capture range is always smaller than the lock range in practical PLL circuits, and the difference between the two is related to the loop filter characteristics.

The output from a PLL system can be obtained either as the voltage signal $V_e(t)$ corresponding to the filtered error voltage in the feedback loop, or as a frequency signal at the VCO output terminal. The voltage output is used in frequency discriminator applications, whereas the frequency output is used in signal conditioning, frequency synthesis, or clock recovery applications. Many of these classes of application will be discussed further in Section 12.4.

First, consider the voltage output. When the PLL is locked on an input frequency, the error voltage $V_e(t)$ is proportional to the frequency difference between the input signal at frequency f_s and the original VCO free-running frequency f_o, since $V_e(t)$ corresponds to the corrective voltage applied to the VCO to shift its frequency from f_o to f_s to maintain lock. If the input frequency is varied, as is the case with FM signals, the error voltage also varies proportional to the input frequency changes in order to maintain lock. Thus, the voltage output serves as a frequency discriminator and converts the input frequency changes to voltage changes.

Next, consider the frequency output. When the PLL is locked on an input signal, the VCO output provides a periodic waveform which is at the same exact frequency as the input signal, except for a finite phase difference ϕ_o, which is the phase difference necessary to generate the error voltage to keep the PLL in lock. If the input signal is comprised of many frequency components, along with noise and other disturbances, the PLL can be made to lock, selectively, on one particular frequency component at the input. The output of the VCO would then regenerate that particular frequency while attenuating or eliminating the other undesired frequencies. In other words, the VCO output can be used to regenerate or extract a desired frequency signal out of many other undesirable signals. This property of a PLL makes it particularly attractive for regenerating or reconditioning weak signals buried in noise.

Capture Phenomenon

A very important characteristic of the PLL performance is the capture process by which the PLL acquires lock with an input signal, starting with a free-running condition. This capture or acquisition phenomenon is highly complex and inherently nonlinear; it does not lend itself to simple mathematical analysis. Therefore, it will be described here only in a qualitative way.

First, assume that the PLL feedback loop is opened between the loop filter output and the VCO control input. This would cause the error voltage to be artificially reduced to zero, and the VCO would continue to oscillate at its

free-running frequency f_o. Next, assume that an input signal is applied to the loop whose frequency f_s is close but not equal to f_o. The phase detector normally functions as a multiplier or mixer. Thus, coming out of the phase detector will be two frequency components, a sum frequency

$$f_{\text{sum}} = f_o + f_s \tag{12.1}$$

and a difference frequency

$$\Delta f = |f_o - f_s| \tag{12.2}$$

Normally, the low-pass loop filter bandwidth is sufficiently narrow such that the sum component is filtered out completely. If f_s is sufficiently close to f_o, then the difference frequency is very small and falls within the passband of the low-pass loop filter; it appears at the output of the loop filter as a sinusoidal *beat note*. This is the waveform shown at the left side of Figure 12.2, where, for illustrative purposes, $f_o > f_s$ is assumed.

Next, assume that the loop is suddenly closed by connecting the low-pass filter output to the VCO control terminal. This would cause the VCO frequency itself to be modulated by the beat note or the difference signal. When this happens, the beat note frequency Δf becomes a function of time. Since the VCO frequency is now a varying function of time, it will alternately move closer to and away from the incoming frequency. Since the filtered error voltage is the difference of the VCO frequency and the input signal, it will also alternately seem to reduce and increase in frequency in its positive and negative half-cycles. Therefore, under this condition, the beat note becomes asymmetrical and looks like a series of cusps, as shown in the middle portion of Figure 12.2. Note that the portion of the beat note that modulates the VCO *closer* to the input signal

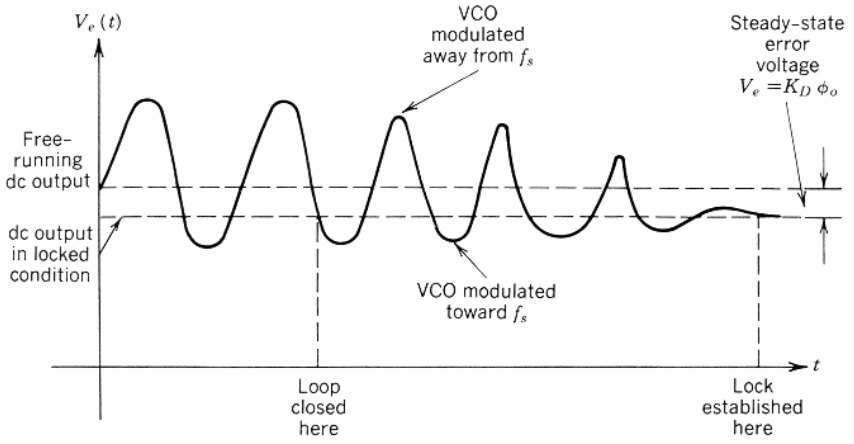


FIGURE 12.2. Typical error voltage transient during capture process.

appears more rounded and the portion that modulates the VCO *away* from the input signal appears more peaked. Because of this asymmetry, the beat note contains a finite dc voltage which steadily pushes the VCO frequency toward the input signal. As the VCO drifts toward f_s, the beat note frequency rapidly decreases, the asymmetry increases, and the transient rapidly converges to a steady-state dc value, corresponding to the lock condition where the VCO frequency is exactly equal to f_s. Once the system is locked, the difference frequency Δf is identically equal to zero, and only a dc voltage remains at the loop filter output. This dc voltage is generated by the phase difference ϕ_o between the VCO output and the input signal. Assuming that the loop filter has unity gain at dc and the phase detector has a conversion gain of K_D V/rad, this steady-state error voltage is

$$V_e = V_e(t)\Big|_{\text{steady state}} = -K_D\phi_o \tag{12.3}$$

The negative sign in Eq. (12.3) is due to the implicit assumption in the example of Figure 12.2 that $f_o > f_s$ and that a negative voltage had to be generated at the control terminal of the VCO to shift f_o to f_s. This point will be clarified further in the next sections as we study the characteristics of phase detector circuits.

The total time taken by the PLL to establish lock is called *pull-in* time. The pull-in time depends on the initial phase and frequency difference between the two signals, as well as on the overall loop gain and loop filter characteristics. Under certain conditions, the pull-in time can be shorter than the period of beat note, and the loop can lock without an oscillatory error transient of the form illustrated in Figure 12.2.

The main purpose of the loop filter is to filter out the difference components due to undesired signals which are far removed from the VCO free-running frequency. In this manner, it enhances the interference rejection characteristics of the PLL. In other words, qualitatively speaking, the PLL would capture only those signals that are close to the VCO free-running frequency, such that the difference frequency Δf falls approximately within the bandwidth of the loop filter. A second and equally important function of the low-pass filter is that it provides a short-term memory for the PLL and ensures a rapid recapture of the signal, if the system is briefly thrown out of lock due to an interfering transient. In other words, the low-pass loop filter constrains the error voltage $V_e(t)$ to be a slowly varying function of time, such that if the PLL is temporarily thrown out of lock due to a noise or interference transient, the VCO frequency does not change significantly over a short period of time. This condition, then, would facilitate a rapid recapture of the input signal once the transient has passed.

Since the low-pass loop filter attenuates the high-frequency components of the error voltage in the PLL, it has a dominant effect on the capture and transient response characteristics of the system. The reduction of filter bandwidth has the following effects on the system performance:

1. The capture process becomes slower and the pull-in time increases.
2. Capture or acquisition range decreases.
3. Once locked, the interference–rejection characteristics of the PLL improve since the error voltage caused by an interfering frequency is attenuated further by the low-pass filter.
4. The transient response, that is, the response of the PLL to sudden changes of the input frequency within the capture range, becomes underdamped.

This last point also brings about a practical limitation of the loop–filter bandwidth and its frequency rolloff and phase characteristics from the point of view of feedback system stability. These points will be explored further in Section 12.3.

Tracking Characteristics

Once the PLL is locked on an input signal, it can track small frequency changes of the input signal by generating additional phase error ϕ_o between the VCO and the input signal, which is then converted to a dc error voltage V_e by the phase detector. This error voltage, then, keeps the VCO frequency in step with the input. While the PLL is tracking an input signal, the loop error voltage V_e is a direct measure of the *frequency difference* of the input signal from the VCO free-running frequency f_o. In other words, while the PLL is tracking an input signal, the voltage output of the loop functions as a frequency-to-voltage converter.

The tracking range of a PLL is determined by how much corrective error voltage V_e can be generated internally. Assuming that no other amplification or gain stage is present in the loop, the maximum amount of error voltage $(V_e)_{\max}$ that can be generated depends on the phase detector gain K_D. Normally, $(V_e)_{\max}$ is generated when the phase difference ϕ_o has reached its limiting value of $\pm \pi/2$ rad, about its equilibrium (zero error) point. Then the tracking range of the PLL is given as

$$\pm \Delta f_L = \pm (V_e)_{\max} K_0 \tag{12.4}$$

where K_0 (Hz/V) is the voltage-to-frequency conversion gain of the VCO.

Figure 12.3 illustrates the typical frequency-to-voltage transfer characteristics of a PLL. The input is assumed to be a sine wave whose frequency is swept slowly over a broad frequency range, first from low frequencies across the PLL capture and lock ranges to high frequencies and then back down to low frequencies. The vertical scale is the filtered loop error voltage V_e, and the VCO is assumed to have linear control characteristics where increasing the control voltage causes the frequency to increase. With reference to Figure 12.3*a*, the transfer characteristics of the PLL can be described as follows. The PLL does not respond to the input signal until its frequency reaches f_1, corresponding to

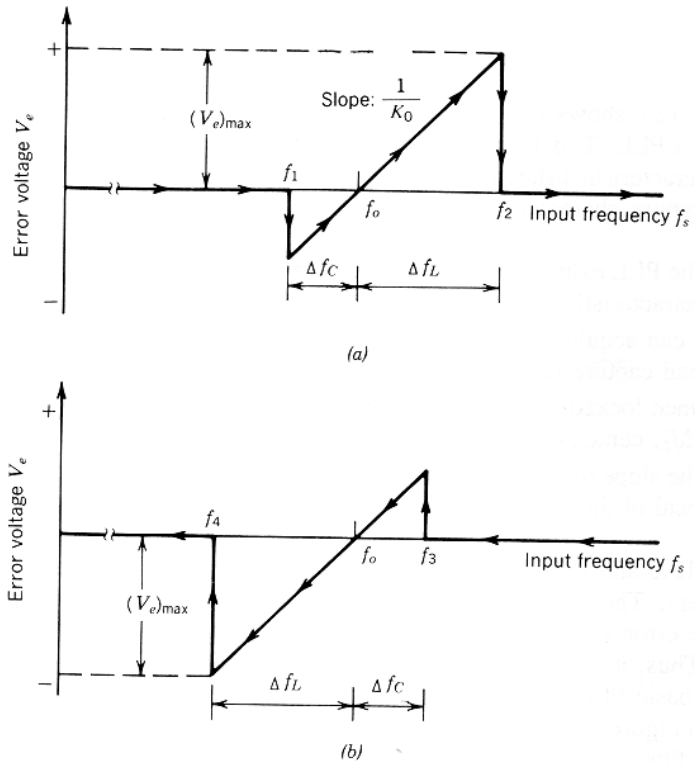


FIGURE 12.3. Typical PLL frequency-to-voltage transfer characteristics: (*a*) Slowly *increasing* input frequency; (*b*) *decreasing* input frequency.

the lower edge of the capture range. Then the loop suddenly locks on the input signal, causing a negative jump of the loop error voltage. As the input frequency continues to increase, the loop tracks the input signal and V_e continues to increase with a slope equal to the reciprocal of the VCO conversion gain $1/K_0$, and goes through zero at $f_s = f_o$. The loop tracks f_s until the input frequency reaches f_2, corresponding to the upper edge of the tracking range. As the PLL loses lock, the error voltage drops to zero and the VCO frequency returns to f_o.

If the input frequency f_s is now slowly swept back toward low frequencies, the cycle repeats itself, as shown in Figure 12.3*b*, where the loop recaptures the signal at $f_s = f_3$ and tracks it down to $f_s = f_4$. The frequency spread between f_1, f_3 and f_2, f_4 corresponds to the total capture range and the total tracking range of the system, that is,*

$$f_3 - f_1 = 2\Delta f_C \tag{12.5}$$

*In describing PLL characteristics, the term *acquisition range* is used interchangeably with *capture range*. Similarly, the term *tracking range* is used interchangeably with *lock range*.

and

$$f_2 - f_4 = 2\Delta f_L \tag{12.6}$$

Figure 12.4 shows a composite set of frequency-to-voltage transfer characteristics for a PLL. This is essentially a superposition of the capture and tracking range characteristics shown in Figure 12.3. With reference to Figure 12.4, the basic response characteristics of the PLL can be summarized as follows:

1. The PLL exhibits a frequency-selective frequency-to-voltage conversion characteristic, centered around the VCO free-running frequency f_o.
2. It can acquire lock (capture) with only those signals that fall within the total capture range of $2\Delta f_C$, centered about f_o.
3. Once locked, it can track an input signal over a total tracking range of $2\Delta f_L$, centered about f_o.
4. The slope of frequency-to-voltage conversion characteristics is the reciprocal of the VCO voltage-to-frequency conversion gain.

Figures 12.3 and 12.4 also indicate the significance of some of the PLL design parameters. The total lock range is primarily determined by the maximum available error voltage $(V_e)_{max}$ and the VCO conversion gain as given by Eq. (12.4). Thus, it can be increased by increasing $(V_e)_{max}$ and adding an amplifier into the basic PLL to provide additional voltage gain in the feedback loop, as shown in Figure 12.5. When the PLL is in lock, V_e is primarily a dc voltage, and the loop filter does not affect the tracking range.

The capture range is always equal to or smaller than the lock range, if a low-pass loop filter is present. As will be described in later sections [see Eq. (12.41)], the capture range decreases as the loop filter bandwidth is reduced.

The VCO free-running frequency f_o determines the nominal center frequency of the capture and lock ranges. Therefore, its accuracy and stability are ex-

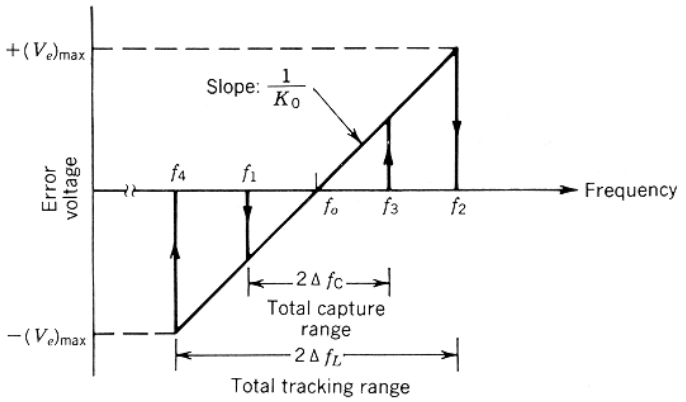


FIGURE 12.4. Composite voltage-to-frequency transfer characteristics of a PLL.

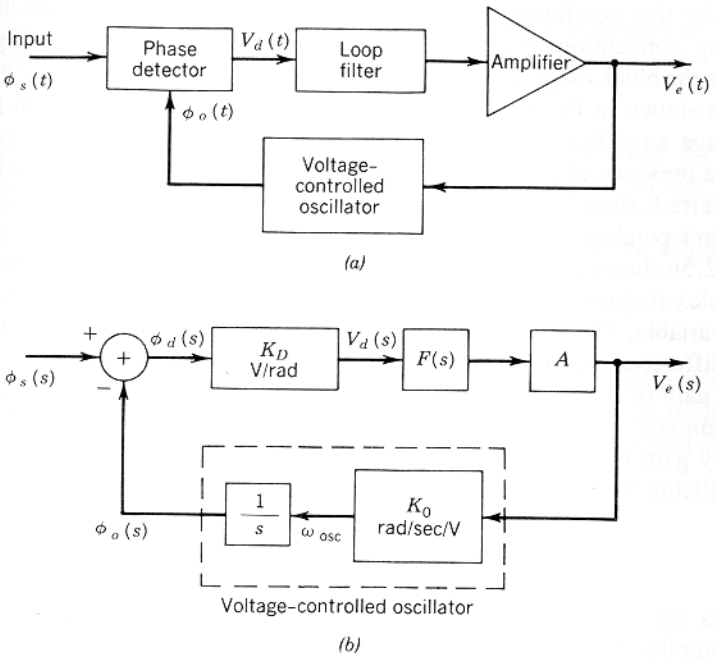


FIGURE 12.5. Block diagram of PLL system in locked condition: (*a*) Generalized block diagram; (*b*) its representation as linear feedback system in frequency domain.

tremely important. As the capture and/or tracking range of the PLL are made very narrow by design, these accuracy and stability requirements become more critical.

The VCO control characteristics are particularly important, as shown in Figure 12.4, because the PLL frequency-to-voltage conversion characteristics are solely determined by the VCO control characteristics. The slope of the PLL voltage output, that is, the frequency-to-voltage conversion characteristics, is determined by the VCO conversion gain constant K_0. Similarly, the linearity of the frequency-to-voltage conversion characteristics is solely determined by the linearity of the VCO control characteristics.

Thus, in summary, the overall dc loop gain, loop filter characteristics, VCO stability, and VCO control characteristics make up the four basic parameters in the design of monolithic PLL circuits.

The Lock Range

The lock range of a PLL is defined as that range of frequencies, centered about f_o, over which the PLL can track an input signal once it is locked. It is shown as the frequency range $\pm \Delta f_L$ in Figure 12.4. As described in Eq. (12.4), Δf_L is directly proportional to the maximum error voltage $(V_e)_{\max}$ that can be generated within the PLL. The maximum error voltage which can be generated is, in turn, related to the maximum phase error $(\phi_s)_{\max}$ and phase detector gain K_D. If a generalized PLL configuration, such as the one shown in Figure 12.5, is used, the amplifier gain A also enters into the equation.

In the phase detector circuits most commonly used in IC PLLs (see Section 12.5), the maximum phase error $(\phi_s)_{\max}$ which can be detected is

$$\pm (\phi_s)_{\max} = \pm \frac{\pi}{2} \text{ rad} \tag{12.30}$$

Thus, assuming a fully switched, balanced-modulator-type phase detector such as the one shown in Figure 12.19, the maximum error voltage that can be generated in the loop is

$$\pm (V_e)_{\max} = \pm (\phi_s)_{\max} K_D A \tag{12.31}$$

Note that in the calculation of the tracking range, we are talking about steady-state operation with a dc error signal in the loop. Thus, the loop filter characteristics do not enter into the equation. The loop filter is assumed to have unity gain at dc or very low frequencies.

Then, from Eqs. (12.4) and (12.31), one can express the lock range in radians per second as

$$\Delta\omega_L = 2\pi\Delta f_L = \frac{\pi}{2}K_D A K_0 = \frac{\pi}{2}K_L \tag{12.32}$$

In terms of frequency, this simplifies to

$$\Delta f_L = \frac{\Delta\omega_L}{2\pi} = \frac{K_L}{4} \tag{12.33}$$

where, for consistency, K_0 is expressed in radians per second per volt. Thus, the tracking characteristics, or lock range, is directly proportional to the total dc loop gain K_L.

An exception to the above condition can arise when a nonlinearity is present in the feedback loop to limit either $(V_e)_{\max}$ or the pulling range of the VCO. In that case, the lock range will be set by the *clipping limit* of the nonlinearity rather than the loop gain, provided that the clipping limit is reached before the gain limit. In some IC designs, such a nonlinearity is introduced into the PLL feedback loop intentionally in order to limit the tracking range or make it asymmetrical about f_o. This technique is particularly useful in the presence of strong out-of-band interference signals near the PLL center frequency.

Capture Range

The capture range is the range of input frequencies in the vicinity of f_o over which the PLL can acquire lock on an input, starting with the no-lock condition. As described briefly in Section 12.1 (see Figs. 12.3 and 12.4), the capture range Δf_C or $\Delta\omega_C$ $(=2\pi\Delta f_C)$ is always less than the lock range if a low-pass loop filter is present. As a result, the PLL exhibits a hysteresis characteristic, as shown in Figure 12.4, where it can track a signal over a wider frequency range than it can capture. The qualitative reasons for this effect will be discussed in this section. Since the rigorous analysis of the capture phenomenon is cumbersome and difficult, the following analysis is primarily intended as a rule-of-thumb estimate.[5]

With reference to Figure 12.5*a*, assume that the loop is opened at the output of the amplifier, and a signal frequency f_s, which is close but not equal to f_o, is applied to the input. Then a sinusoidal beat note, similar to that shown on the left-hand side of Figure 12.2, would appear at the phase detector output as

$$V_d(t) = \frac{\pi}{2}K_D \cos(\Delta\omega_i t) \tag{12.34}$$

where

$$\Delta\omega_i = \left|\omega_s - \omega_o\right| \tag{12.35}$$

is the beat note frequency. The amplitude of $V_d(t)$ is

$$V_d(t)\Big|_{\text{peak}} = \frac{\pi}{2}K_D \tag{12.36}$$

The amplitude of the corresponding filtered and amplified error voltage appearing at the loop voltage output is

$$V_e(t)\Big|_{\text{peak}} = \frac{\pi}{2}K_D A\left|F(j\Delta\omega_i)\right| \tag{12.37}$$

where $|F(j\Delta\omega_i)|$ is the magnitude of loop filter response at the beat note frequency. Due to low-pass characteristics, $|F(j\Delta\omega_i)|$ is always less than unity.

In order for capture to occur, the magnitude of the voltage that must be applied to the VCO control terminal is

$$\left|V_{\text{osc}}\right| = \frac{\Delta\omega_i}{K_0} = \frac{|\omega_s - \omega_o|}{K_0} \tag{12.38}$$

As a rough estimate, the capture effect can take place only if the peak error voltage given by Eq. (12.37) is equal to or greater than that required by Eq. (12.38) to shift the oscillator frequency. Thus, the condition for capture can be estimated by setting Eqs. (12.37) and (12.38) to be approximately equal at the point of capture, that is,

$$\frac{\Delta\omega_i}{K_0} \approx \frac{\pi}{2}K_D A\left|F(j\Delta\omega_i)\right| \tag{12.39}$$

However, at the frequency where the capture occurs, $\Delta\omega_i = \Delta\omega_C$ by the definition of capture range. Substituting this into Eq. (12.39) and rearranging terms, one gets

$$\Delta\omega_C \approx \frac{\pi}{2}K_L\left|F(j\Delta\omega_C)\right| \tag{12.40}$$

or in terms of the lock range, from Eq. (12.32),

$$\Delta\omega_C \approx \Delta\omega_L\left|F(j\Delta\omega_C)\right| \tag{12.41}$$

Since the magnitude of the low-pass filter response is always less than unity, the capture range estimated from Eq. (12.40) or Eq. (12.41) is always less than the lock range. The difference becomes more significant as the filter bandwidth is reduced.

Equation (12.41) is a parametric equation which can be solved by numerical

techniques for any generalized filter function. However, in the case of a high-gain second-order loop with a narrowband one-pole low-pass filter of the form shown in Figure 12.7, it can be approximated in a closed form. In such a case,

$$\left| F(j\Delta\omega_C) \right| = \left| \frac{1}{1 + j\Delta\omega_C/\omega_1} \right| = \frac{1}{\sqrt{1 + (\Delta\omega_C/\omega_1)^2}} \tag{12.42}$$

Assuming that the loop gain K_L is high and the filter bandwidth is narrow, such that $\Delta\omega_C \gg \omega_1$, Eq. (12.42) simplifies to

$$\left| F(j\Delta\omega_C) \right| \approx \frac{\omega_1}{\Delta\omega_C} \tag{12.43}$$

Substituting Eq. (12.43) into Eq. (12.41) and rearranging terms, one gets

$$\Delta\omega_C \Big|_{\text{lag filter}} \approx \sqrt{\Delta\omega_L \omega_1} = \sqrt{\frac{\Delta\omega_L}{R_1 C_1}} \tag{12.44}$$

where $R_1 C_1 = 1/\omega_1$ is the low-pass filter time constant. In using Eq. (12.44), one word of caution is in order. It is derived with the implicit assumption that $\Delta\omega_C \gg \omega_1$. Thus, it should be used only if the value of $\Delta\omega_C$ given by it indeed justifies this assumption.

12.4. APPLICATIONS OF PHASE-LOCKED LOOPS

The PLL is a very versatile building block suitable for a variety of frequency-selective signal demodulation, signal conditioning, synchronization, and frequency synthesis applications. In this section, some of these applications will be reviewed. Particular attention is given to applications which relate to monolithic PLL circuits.

In the applications illustrated in this section, the PLL is shown in its simplest form without an amplifier block within the loop. However, since such an amplifier can always be added into the PLL system when needed, leaving it out does not detract from the general nature of the conclusions.

FM Demodulation

If the PLL is locked on a frequency modulated signal, the VCO tracks the instantaneous frequency deviation of the input. Then the filtered error voltage $V_e(t)$, which constrains the VCO to maintain lock with the input signal, corresponds to the demodulated output.

Figure 12.10*a* shows the basic block diagram of a phase-locked loop FM demodulator. In this case, the linearity of the demodulated output characteristics is determined by the VCO voltage-to-frequency conversion characteristics, since the reciprocal of the VCO conversion gain $1/K_0$ determines the output voltage swing for a given input frequency change (see Figs. 12.3 and 12.4).

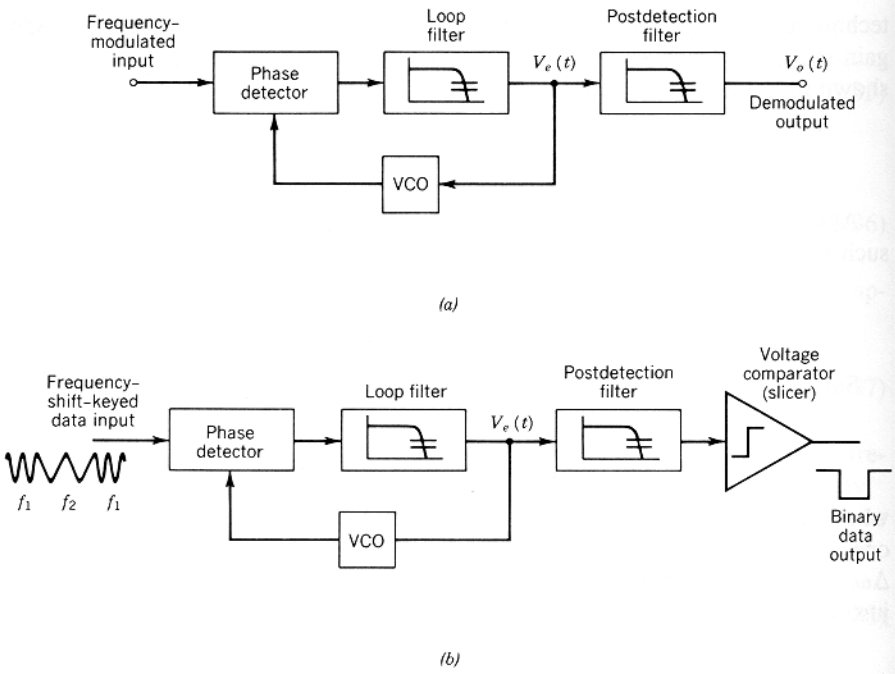


FIGURE 12.10. PLL as FM and FSK demodulator: (*a*) FM demodulator; (*b*) FSK demodulator (decoder).

In many applications, the demodulated signal $V_e(t)$ is filtered further by a so-called *postdetection filter* outside the PLL feedback loop. The function of the postdetection filter is to filter out any carrier feedthrough which may be present in the loop error voltage.

The PLL can be used to detect either wideband (high-deviation) or narrowband FM signals with a higher degree of linearity than that what can be obtained from other FM detection techniques. For this application, the linearity of the VCO control characteristics is critical since any nonlinearity in VCO conversion gain directly affects the distortion of the output signal.

In FM demodulation applications, the PLL loop gain and loop filter are chosen to provide a flat frequency response (i.e., $\zeta \geq 1/\sqrt{2}$), and both the loop lock and the capture range are made significantly larger than the input FM signal frequency deviation. In commercial FM detection, the main drawback of monolithic IC PLLs is the relatively poor signal-to-noise (S/N) ratio at the output due to the VCO phase noise associated with the multivibrator-type oscillators used. This limits the practical signal-to-noise ratio of demodulated output to approximately 65 dB for $\pm$ 1% deviation FM signals.[6]

Frequency-shift keying (FSK) is a special form of frequency modulation used in binary data transmission. The digital information is transmitted by switching the input frequency between two discrete frequencies called *mark* and *space* frequencies, which correspond to digital 1 and digital 0, respectively. Figure

12.10*b* shows the basic PLL system used as an FSK decoder. When the PLL is locked on the input FSK signal and follows the step changes of the input frequency, the error voltage $V_e(t)$ is in the form of discrete voltage steps corresponding to input frequency changes (see Fig. 12.8). These voltage steps correspond to the demodulated data output. In a conventional FSK detector system, as shown in Figure 12.10*b*, this output is filtered further by a postdetection filter to eliminate carrier feedthrough and then converted to logic-level swings by means of an output voltage comparator or *slicer*.

In optimizing a PLL's performance for FSK decoding, one normally chooses the VCO free-running frequency f_o to be midway between mark and space frequencies, that is,

$$f_o = \tfrac{1}{2}(f_{\text{mark}} + f_{\text{space}}) \tag{12.45}$$

so that the error voltage within the loop would change polarity when the input signal frequency makes a transition. Typically, the loop capture range is chosen to be well in excess of the input frequency step size, and the loop is made slightly underdamped ($\zeta \approx 0.5$) to obtain a rapid rise time of the error voltage, without excessive overshoots (see Fig. 12.8*c*).

Frequency Synchronization

Using the PLL system, the frequency of a relatively poor oscillator, such as an emitter-coupled multivibrator, can be phase locked to a low-level but highly stable frequency reference signal. This can be done by using the oscillator to be synchronized as the VCO portion of a PLL. Then the VCO output reproduces the input signal frequency at the same relative accuracy as the input reference, but at a much higher power level. In some applications, the synchronizing signal can be a low-duty-cycle tone burst at a specific frequency. The PLL can then be used to regenerate a coherent continuous-wave (CW) signal, synchronized to such a short tone burst. A typical example of such an application is the phase-locked chroma reference generator integrated circuit in color TV receivers. The horizontal *raster scan* and the vertical scan information in conventional color or black-and-white TV receivers are also synchronized using PLL systems in a similar manner.

In digital systems, the PLL can be used for a variety of data or clock synchronization functions. For example, two system clocks can be phase locked to each other so that one can function as a backup for the other, or it can be used for synchronizing disk or tape–drive mechanisms in information storage and retrieval systems.

Signal Conditioning

If the input signal spectrum contains several out-of-band signals, interfering channels, and noise, in addition to the desired signal frequency, the PLL system can be used to recreate or "condition" the desired signal and eliminate or

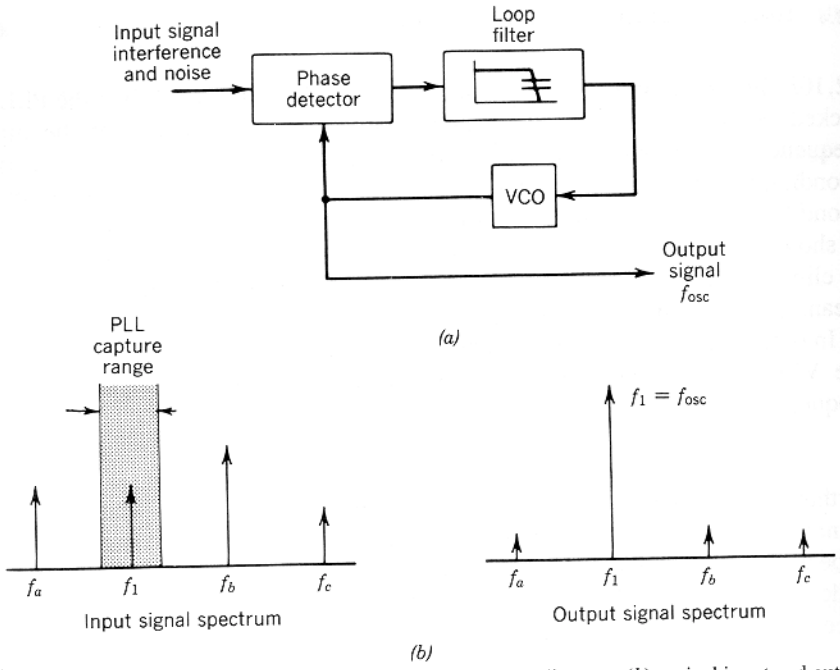


FIGURE 12.11. PLL as signal conditioner: (*a*) System block diagram; (*b*) typical input and output signal spectra. (*Note:* f_1 is the desired signal; f_a, f_b, and f_c represent out-of-band interference signals.)

attenuate the undesired signals. Figure 12.11 illustrates the use of a PLL system in such an application.

By proper choice of the VCO free-running frequency, loop gain, and loop filter function, the selectivity characteristics of the PLL can be centered around the desired signal frequency present at the input; the PLL can be made to lock onto that signal. This is illustrated in Figure 12.11*b* in terms of the desired input signal f_1, which is present at the input along with the undesired signals at frequencies f_a, f_b, and f_c. If the PLL is locked on f_1 and the loop bandwidth is maintained relatively narrow, then the VCO output in Figure 12.11(a) reproduces the frequency of the desired signal while greatly attenuating the out-of-band signals. Note that a small but finite amount of interfering signals still appear at the VCO output spectrum because the difference frequencies between these frequencies and the VCO frequency can still pass through the loop filter, causing a slight modulation or *jitter* of the VCO frequency.

If the loop bandwidth is sufficiently narrow, the signal-to-noise ratio of the VCO output can be much higher than that at the input. Thus, the PLL can be used as a noise filter to regenerate weak periodic signals buried in noise.

A typical signal-conditioning application for monolithic PLL systems is in pulse-code-modulation (PCM) telemetry and telephone systems where the distorted and dispersed pulse-code modulation data have to be accurately regenerated at periodic intervals by means of synchronous *repeater* systems. Often, these repeater systems involve a PLL to extract the synchronous clock signal and then regenerate or recondition the weak input signal into a binary data stream.

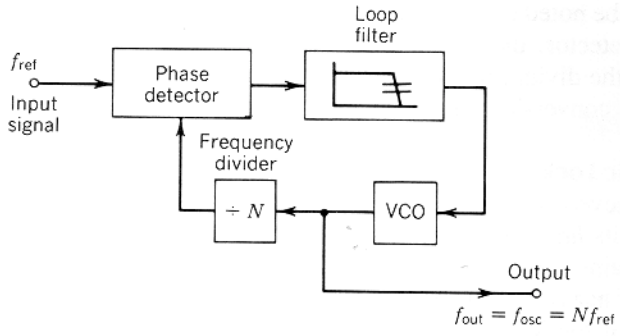
Frequency Synthesis

By inserting a frequency divider circuit into the feedback loop of a PLL, between the VCO output and the phase detector input, the PLL can be made to function as a frequency multiplier. A block diagram of this circuit configuration is shown in Figure 12.12*a*, where N is the frequency-divider modulus. Thus, the actual frequency signal supplied by the loop into the phase detector is $1/N$ times the oscillator frequency. When the PLL is locked on an external reference frequency, the two inputs of the phase detector are at the same frequency, or

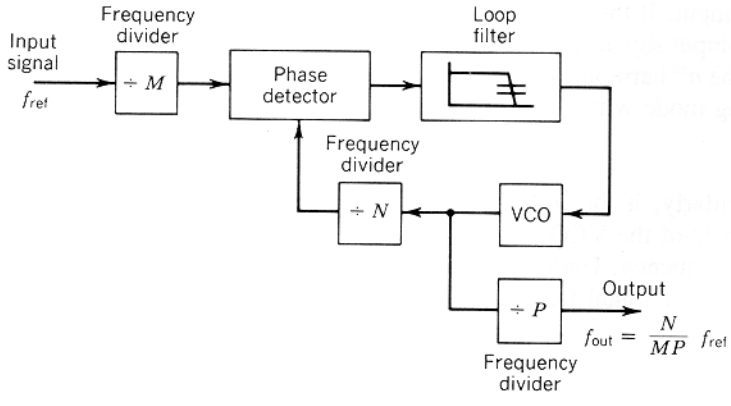
$$f_{\text{ref}} = \frac{f_{\text{osc}}}{N} \tag{12.46}$$

Then, taking the signal at the output of the VCO, one obtains

$$f_{\text{osc}} = Nf_{\text{ref}} \tag{12.47}$$



(a)



(b)

FIGURE 12.12 PLL as frequency synthesizer: (*a*) Basic frequency synthesizer; (*b*) synthesizer with pre- and post-scaling dividers.

By selectively changing the divider modulus N, one can obtain a multiplicity of frequencies which are integer multiples of the input reference frequency.

If a noninteger relationship is desired between the input and output frequencies, additional frequency dividers, such as those shown in Figure 12.12*b*, can be added into the system. In such a configuration, the divider with modulus M is called a *prescaler,* and the divider with modulus P is called a *postscaler*. By equating the frequency of the signals entering the phase detector, one can show that

$$f_{\text{out}} = \frac{N}{MP} f_{\text{ref}} \tag{12.48}$$

PLL frequency synthesizers are very widely used in transmitters, receivers, and transponders, as well as in laboratory instrumentation. The examples shown in Figure 12.12 are some of the simplest configurations. In practice, frequency synthesizer circuitry can get quite complex and often involves several interlocked PLL systems.[7]

It should be noted that when a frequency divider is used between the VCO and the phase detector, the effective conversion gain of the VCO becomes K_0/N, where N is the divider modulus. Since the loop gain K_L is directly proportional to the VCO conversion gain, it is also reduced by the factor $1/N$.

increasing C_1 and then correct for loop damping by adding R_2 in series with C_1 into the low-pass filter. With reference to the design equations (12.27) through (12.29), or those shown in Table 12.1, one proceeds as follows.

Step 1: Calculate C_1 to set a 3-dB bandwidth. From Eq. (12.29), the low-pass filter bandwidth ω_1 can be calculated as

$$\omega_1 = \frac{1}{(R_1 + R_2)C_1} \approx \frac{(\omega_{3\,\mathrm{dB}})^2}{4K_L} = 555 \text{ rad/sec} \tag{12.82}$$

Assuming $R_1 \gg R_2$,

$$C_1 = \frac{1}{(R_1 + R_2)\omega_1} \approx \frac{1}{R_1\omega_1} = 0.6\ \mu\text{F} \tag{12.83}$$

Step 2: Calculate the value of R_2 to keep $\zeta \approx 1/\sqrt{2}$. From Eq. (12.28), one gets

$$\omega_2 = \frac{1}{R_2C_1} \approx \sqrt{\frac{K_L\omega_1}{2}} = 6.66 \times 10^3 \text{ rad/sec} \tag{12.84}$$

or

$$R_2 = \frac{1}{\omega_2 C_1} = 250\ \Omega \tag{12.85}$$

Note that both the $R_1 \gg R_2$ assumption used in Eq. (12.83) and the $K_L \gg \omega_1$ assumption used in Eq. (12.28) are satisfied.

REFERENCES

1. F. M. Gardner, *Phaselock Techniques,* 2nd ed., Wiley, New York, 1979.
2. W. C. Lindsey and M. K. Simon, Eds. *Phase-Locked Loops and Their Applications,* IEEE Press, New York, 1978.
3. A. B. Grebene, and H. R. Camenzind, "Frequency-Selective Integrated Circuits Using Phase-Lock Techniques," *IEEE J. Solid-State Circuits* **SC-4,** 216–225 (August 1969).
4. A. B. Grebene, *Analog Integrated Circuit Design,* Van Nostrand Reinhold, New York, 1972, Chap. 9.
5. P. R. Gray and R.G. Meyer, *Analysis and Design of Analog Integrated Circuits,* Wiley, New York, 1977, Chap. 10.
6. *Phase-Locked Loop Data Book,* Exar Integrated Systems, Sunnyvale, CA, 1981.
7. W. F. Egan, *Frequency Synthesis by Phase-Lock,* Wiley Interscience, New York, 1981.
8. A. Blanchard, *Phase-Locked Loops: Application to Coherent Receiver Design,* Wiley, New York, 1976.
9. A. B. Grebene, "The Monolithic Phase-Locked Loop—A Versatile Building Block," *IEEE Spectrum,* 38–49 (March 1971).
10. *Phase-Locked Loop Data Book,* 2nd Ed., Motorola, Phoenix, AZ, August 1973.
11. D. K. Morgan and G. Steudel, "The RCA COS/MOS Phase-Locked Loop," App. Note ICAN-6101, RCA Corp., Somerville, NJ, October 1972.