EE155/155 Homework 2 Solutions

October 11, 2017

1 Problem 1

1.a

The energy dissipated in the FET during the turn-on is found via the voltage across the FET and the current through the FET. The power dissipated in the FET is the product of the two waveforms v_{M1} and i_{M1} shown in Figure 1. Let E_1 be the energy dissipated in t_1 and E_2 be the energy in t_2.

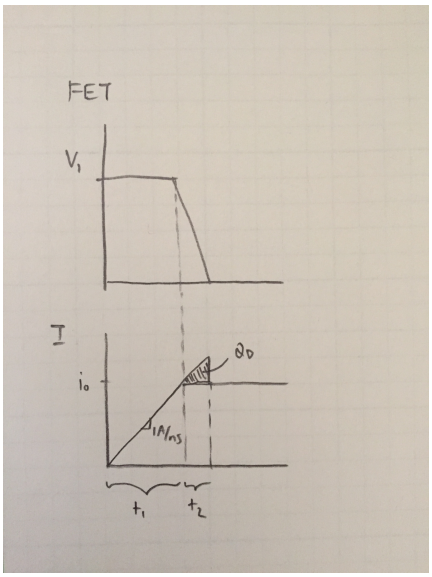

Figure 1: FET Voltage and Current over time

The energy dissipated in E_1 is due to the finite current ramp time of the FET. t_1 is the time that it takes for the FET's drain current to equal i allowing the diode to turn off.

$$t_1 = \frac{10A}{1A/ns} = 10ns$$

$$E_1 = \frac{1}{2}V_1 it = 0.5(400V)(10A)(10ns) = 20\mu J$$

After the diode has switched off, the drain capacitor must fully discharge before the drain node falls to 0V. We can assume the voltage falls linearly to zero over time t_2 as the current continues to linearly increase until the capacitor is fully discharged at which point the current drops immediately to 10A. Since we don't know the exact parasitics of the FET, other acceptable current waveforms can have the both a ramp up in current above 10A and a ramp down over time t_2.

We can assume that the current continues to linearly increase as the capacitor discharges through the FET at the same rate of $1A/ns$.

$$Q_D = C_{DS}V_1 = (70pF)(400V) = 28nC$$

$$t_2 = \sqrt{(\frac{2Q_D}{s})} = \sqrt{\frac{(2)(28nC)}{1A/ns}} = 7.48ns$$

We can now solve for the voltage slope, given by $\frac{\Delta V}{t_2}$, or $-53.47V/ns$. Given the voltage and current slope and times, we can now solve for E_2. Adding energies we get the total turn on energy.

$$E_2 = \int_0^{7.48ns} i_{ds}V_{ds}dt = \int_0^{7.48ns} (10A + \frac{1A}{ns}t)(400V - \frac{53.47V}{ns}t)dt = 18.69\mu J$$

$$E_{on} = E_1 + E_2 = 38.69\mu J$$

1.b

$$P_{sw} = 100kHz * E_{on} = 3.87W$$

1.c

Diode conduction lost is the average current through the diode times its voltage drop

$$P_{diode} = 0.5(1V)(10A) = 5W$$

FET conduction lost is the resistive loss from R_{on} while the FET is on times the average current through it.

$$P_{FET} = 0.5(I_D^2)(R_{on}) = 0.5(10A)^2(45m\Omega) = 2.25W$$

1.d

Doubling the current ramp should reduce the switching energy and P_{sw} in parts a and b. Specifically t_1 is halved to $5ns$, E_1 is halved to $10\mu J$, t_2 reduced to $5.29ns$, and E_2 reduced to $12.45\mu J$. For part b, switching power is reduced to $2.245W$

2 Problem 2

The minimum time that is required before the drain can reach 0V is dictated by the amount of charge the gate driver must remove from the capacitor to set the drain voltage at 0. Note that there is a change of 400V despite there being only 395V across the capacitor, and the likewise the capacitor will have a final voltage of -5V across it.

$$Q_{DG} = V_1 C_{DG} = (400V)(75pF) = 30nC$$

$$t_{min} = \frac{30nC}{2A/ns} = 15ns$$